Microelectronics: Devices to Circuits
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Lecture – 29
CMOS CG/CD Amplifier Configuration

Hello everybody and welcome to the NPTEL Online Certification Course on Microelectronics: Devices to Circuits. Today's lecture will be primarily concerned with common Gate and common drain amplifier configuration. In our previous schedule, we had looked into common source amplifier with source degeneration resistance as well as without source degeneration resistance. We also saw the advantages of having an source degeneration resistance.

And the advantage primarily was to do with enhanced bandwidth but a reduced gain and more stability. What we will do today is have a look at common gate configuration and common drain. But, please take into consideration that most of the time common source configuration is used as an amplifier because of its relatively high gain which depends upon the value of transconductance of the MOS device under study.

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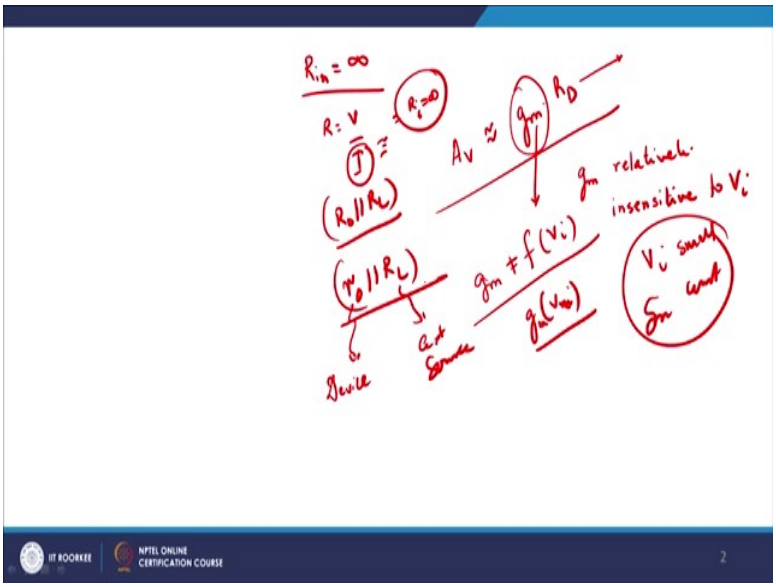

So, higher the transconductance, we remember yesterday in our previous discussion, if you look very carefully, what we did, what we saw was the gain in general is considered to be equals to g_m times R_D. This we have already learnt where g_m is the transconductance of the device and R_D is the drain resistance. Now, this g_m we have already discussed this point that is you need to be relatively insensitive to V_i. Right.

Which means that to input voltage. Which means that gm should not be a function of V_i. In reality, it is not true and therefore, g_m happens to be a function of input voltage. But if your g_m or V_i is relatively a small signal then my g_m is considered to be constant right. Under that condition, we say that my linearity is sustained and I am in a saturation region. We have also seen in the previous interactions and discussions that the input impedance of MOS device is always infinity.

R_{in} is typically infinitely large because you are actually feeding your signal to the gate side. And since the gate side has got oxide layer inbuilt into it you will not have any current and therefore, your resistance which is voltage by current, since your current is approximately equals to 0 you get R equals to infinity. And that is what typical input resistance of the amplifier is all about.

Output impedance will depend upon many factors but typically it is R_o parallel to R_L, where R_o is the resistance offered by the device itself. r_o should be small parallel to R_L or R_D, where R_o is basically the resistance offered by the device itself and R_L is the resistance offered by the external source. So, with this basic logic or with this basic understanding, let us now undergo what is known as a Common Gate Amplifier.

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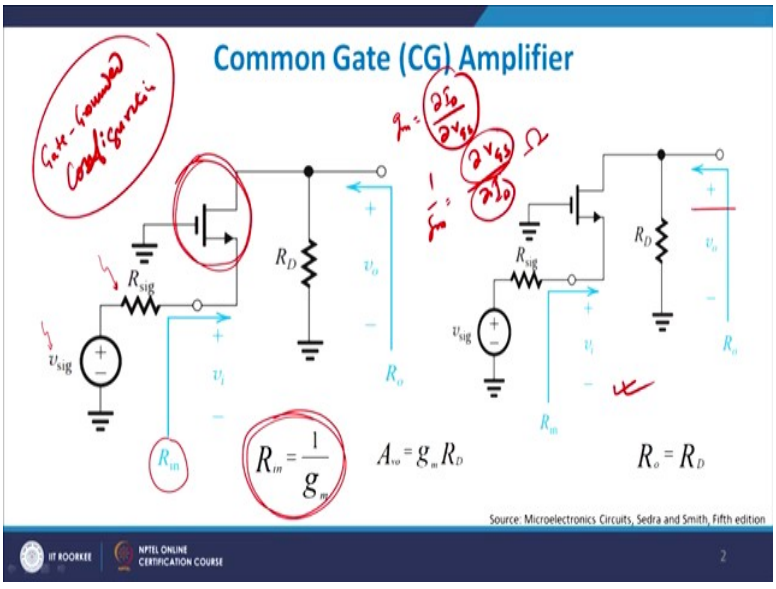

In the Common Gate Amplifier you need to therefore ground your Gate. So, if you look at this diagram here, this is your NPN transistor which you see or sorry it is an N channel MOSFET which you see and its gate is basically grounded here which means this is also referred to as Gate Grounded Configuration. Right. So, this is Gate Grounded Configuration and this is also referred to as Gate Grounded Configuration and the Gate is grounded.

Now, please understand, therefore you are inserting a signal to the source end of my gate and you are extracting the signal from the drain side. So, this is your V_{sig} is my input signal and R_{sig} is my resistance offered by this voltage source. Resistance has a series to it, typically relatively very small and R_{in} is basically the resistance offered by the device looking from the source side.

So understand, looking from the gate side it was infinitely large because there was an oxide layer. But, looking from the source side it is not infinitely large but typical value is 1 by g_m. Right. So, I will not derive it here but a source, from the source side if you want to look in a MOS device the resistance offered by it is 1 by g_m, right. So, higher the trans conductance of the device, lower will be your R_{in}.

And intuitively you can understand why is it like that. If you remember, g_m was equals to ∂I_D by ∂V_{GS}, right. So, if you take 1 by g_m it is just the reciprocal of this one and you get ∂V_{GS} by ∂I_D, which means that for how much change in I_D I should get for a typical change in V_{GS}. And if you look at this dimensions it is basically in ohms.

So, this is the resistance offered by the device when you are looking from the source end of its operation. On the right hand side which you see here, which is this one, if you look at this one, we are assuming that the diagram is exactly the same which you see on your left and right. But, here I am assuming that my impedance looking from the drain side is actually equals to R_o.

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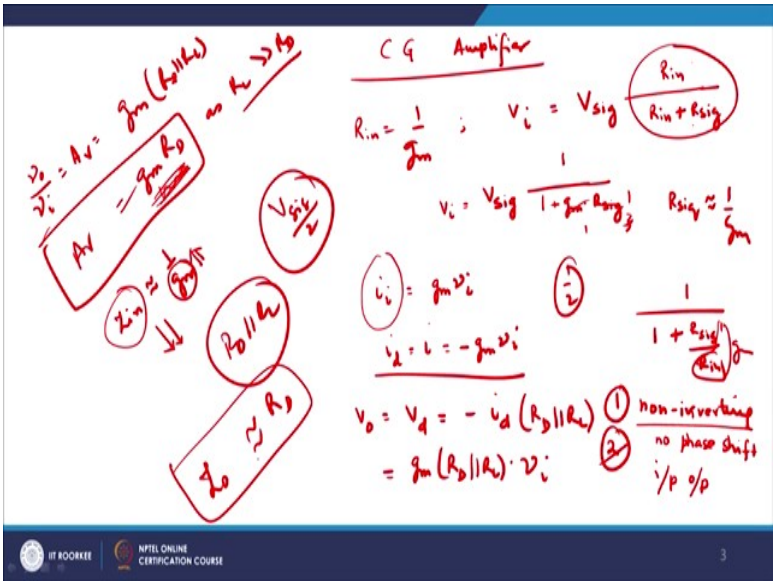

With this knowledge let me just do a small derivation, a brief interaction of CG amplifier. So, this is basically your common gate amplifier, right. If you solve it, I get R_{in} equals to 1 by g_m, this we have already seen just now. I can say V_i equals to V_{sig} into R_{in} upon R_{in} plus R_{sig}. R_{in} is the input voltage, input resistance which you see and V_{sig} is the voltage of the signal which you see. Therefore, I can right down V_i equals to V_{sig} signal divided by 1 upon 1 plus g_m times R_{sig}. How do I get it?

So, how do I get it, if you divide numerator and denominator here by R_{in}. So, if you divide this whole by R_{in}, numerator and denominator, I get 1 in the numerator, I get 1 in the denominator plus R_{sig} by R_{in}. But 1 by R_{in} is nothing but g_m. Therefore, I get g_m times R_{sig}. Therefore, I get input current ii equals to gm times V_i. Please understand here, why are you getting an input current because you are feeding the voltage through the source terminal of the MOS device. That is the reason you are having an input current, right.

This would not have been there provided you are actually doing on the gate side, right, and that is the reason it is g_m times V_i. So, therefore the drain current which you get is also therefore equals to g_m times V_i, but it will be with a negative sign. So, this will be minus gm times V_i, negative, why, because there is a phase shift between there. Sorry, because the current direction will be just reversed as that of the source side.

Therefore, I get V_o which is output voltage also referred to as V_d equals to minus i_d times R_D parallel to R_L. If you solve it, I get g_m times R_D parallel to R_L multiplied by V_i. So, V_o by V_i is nothing but, therefore V_o by V_i is nothing but A_v and that is equals to g_m times R_D parallel R_L, right. Therefore, I can safely right down this to be equals to g_m times R_D as R_L is much larger as compared to R_D. Therefore, I get A_v to be equals to g_m times R_D. You see here, right.

So, your Common Gate Amplifier is basically g_m times R_D you see here A_v gain, right it is g_m times R_D. So, what I get from here is that it can act as a unity drain device provided R_{sig} is approximately equals to 1 by g_m. So, if it is 1 by g_m that cancels out I get 1, so 1 by 2 half. So, what I get half here, I can have V_i to be equals to V_{sig} by half, right. So, half the V_{sig} is available to you in the input side of your device and therefore your gain will also reduce in that sense.

One thing is there, on the second part of it is that, it is one characteristics is that it is noninverting in nature. So, it is noninverting, which means that, the phase, there is no phase change between input and output, right. Because you are feeding from the source side and not

from drain side. There would have been a phase change provided you had taken it from Gate side and taken from the drain side, output would have been from the drain side.

But, in this case you are feeding from the source side and you are taking it from this drain side. Therefore, it is also refer to as non-inverting design with no phase shift between input and output, first thing. Second thing is, if you look very carefully the input impedance of this device is approximately equals to 1 by g_m which we already understood.

Now, this is relatively very low. Because g_m is relatively very high, right. And therefore, Z_{in} is typically low, so the input impedance of the device in the Common Gate Amplifier is relatively low, right. So, that we have understood that it should be low and output impedance can be found out as R_D parallel to R_L and if R_L is typically large it is approximately equals to R_D which you get Z_o output impedance, right, for a Common Gate Amplifier.

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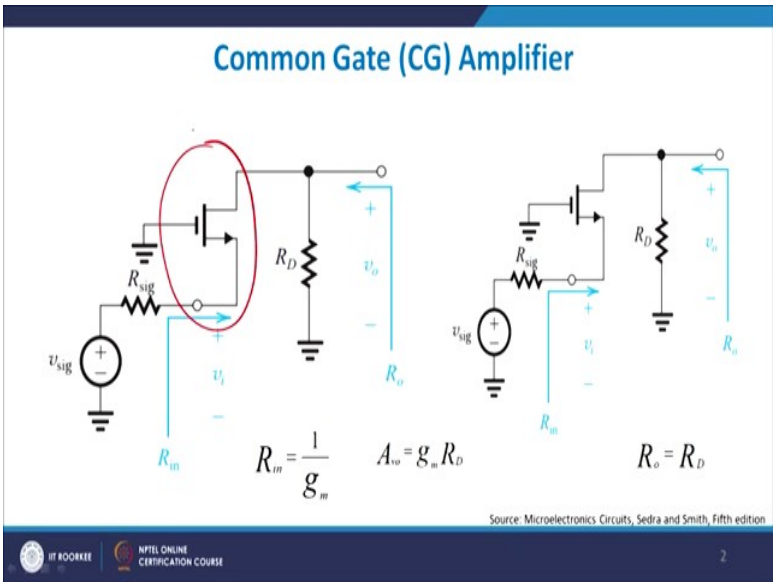

One small thing, which I just wanted to point out to you here is, that that if you look, for example, if you look from this side, this diagram here and just concentrate on this particular point then let us see what is the problem.

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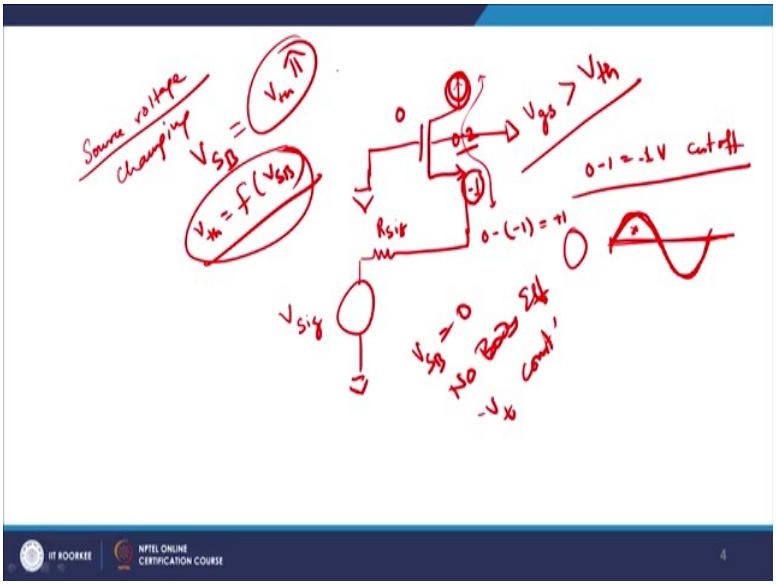

One small problem area of Common Gate. So, please understand, you are feeding the signal from this R_{sig} right, V_{sig} right and this is R_{sig} and you are feeding on to the source terminal of the battery. And the gate is grounded, right. If you look very carefully, when this, so for the device to be on, gate to source voltage should be larger than the threshold voltage of the device. That is the basic concept we have been learning for, we know very well.

Now, if gate is 0 volt and let us suppose my source voltage is positive and let us say it is 1 volt then 0 minus 1 will be equals to minus 1 volt and therefore my device will be in cut off, right. And that is the problem area that whenever my device goes to negative or the positive. Let us suppose, I have a positive and a negative cycle, then for the positive cycle you will automatically have this problem.

In the negative cycle, let us suppose this is minus 1, then what is get is 0 minus of minus 1 which is equals to plus 1. And let us suppose the threshold voltage is point 2 then obviously my device is in the on state, right. So, the negative half cycle it works fine but the positive half cycle you do have a problem that your device might be in the cut off state. And that is the one of the problem areas of Common Gate as such but we will discuss no further than this in this case.

Secondly, why there is no phase difference between Drain and source because you will see, if you look very carefully, whatever potential you are giving here the same potential will appear at this edge, right. Because, the same current has to flow between these two points and therefore it is not out of phase it is perfectly in phase. And therefore, basically it is a non-

inverting. Common Gate is basically non-inverting amplifier and the second thing is Z_{in} is very low and Z_{out} is relatively high.

With this, Okay, One more thing which maybe I can discuss with you is, one more problem area is that, now you see very effectively your source voltage is changing, right. Source voltage is always changing, right. Why it is changing? Because we applied a V_{sig} here. The signal voltage will change and therefore this voltage will go on changing, right. Once this change, obviously V_{SB}, let us suppose our base is grounded, then V_{SB} will also change source to bulk and therefore my threshold voltage, which you remember will be function of V_{SB}.

In the previous, all my examples, since my source was grounded and even if it is not grounded provided in a MOS device, I am able to plug my bulk to the most negative part of the potential. Then my V_{SB} will be approximately equals to 0 and therefore, I will get automatically no body effect. So, under the condition that your V_{SB} is equals to 0, you will never have and there will be no body effect and your V_t will be effectively constant, right.

But, in this case specifically when you are doing a Common Gate structure, you end up a variation in the voltage of the source side and therefore source to bulk voltage goes on varying and therefore threshold voltage becomes the strong function of the source to bulk voltage. And therefore, threshold voltage will vary. And therefore, we are not sure whether the device will be on or off at particular point of time. So, this is one of the problem areas which people face when you are doing a Common Gate translation.

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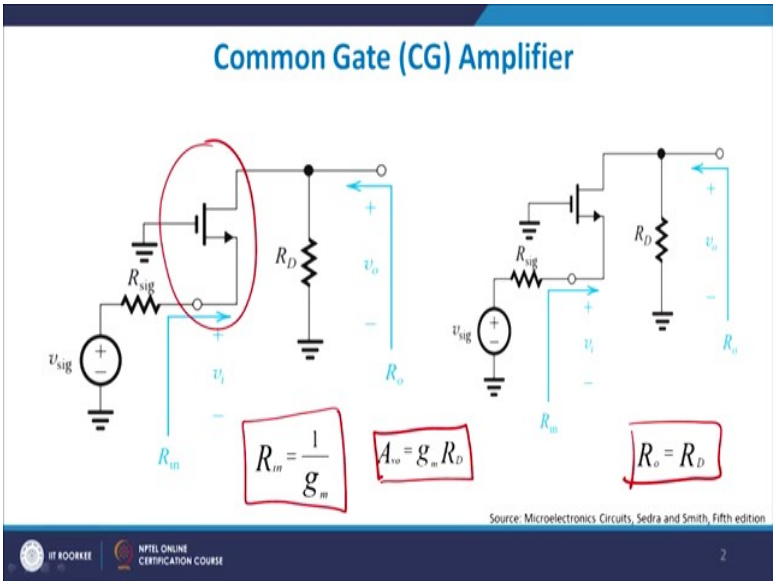

We come to the next part and that is basically, just a minute, so Common Gate we have finished, we have seen that A_{vo} is g_m times R_D and output impedance is approximately equals to R_D and input impedance is 1 by g_m, right. So, it is just Common Gate Configuration which you see.

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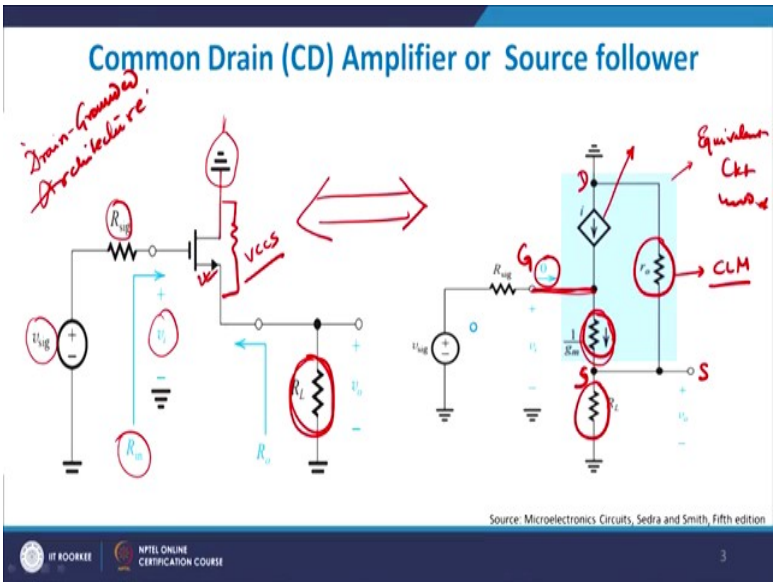

Let me come to Common Drain architecture, Common drain as I told you there are termed as a Common Drain, your drain will be grounded and therefore it is also referred to as Drain Grounded Architecture. It is referred to as a Drain Grounded Architecture. This Drain Grounded Architecture which you see, is primarily means that the drain has been grounded, obviously to the 0 potential here and applying at signal back to the gate side, right.

So, only in one condition which is CG which is Common Gate is the point where you apply the signal through the source side. For all other conditions, for all other amplifier configuration you apply the signal voltage on to the gate side. So, I am applying a V_{sig} here through an R_{sig} here applying to this. V_i is the available input voltage and R_{in} is the input impedance.

So, V_i is the available input voltage out of, so V_{sig} was your total voltage given to the device out of which V_i appears as the input voltage to the Gate side of this device and you get something like this. And then you have R_L here which is the load impedance and there will be a output voltage will be seen from this side. So, if you do a short channel. Sorry, small signal analysis and maybe replace it by a T model then let us see how it works out. So, if you see very carefully, this blue box is my Equivalent Circuit Model. I will explain to you how we got it.

First of all see, this ro is between this point and this point and this primarily comes out because of CLM. So, Channel Length Modulation remember, I am assuming that my output impedance will be infinitely large, not true, there will be a finite impedance available between the drain. So, this is your drain end and this is your source end and this is your drain end. So, you will automatically have a impedance or a resistance between Drain and Source, which you see in front of you, this one. And therefore, this is your source actually and therefore you get this thing.

What is 1 by g_m? 1 by g_m is nothing but this device itself. Because, remember this is basically a VCCS (Voltage Control Current Source). So, I can safely write down the resistance offered by the device is 1 by g_m looking from the source end. We discussed this point earlier also, right. This is the point. And this R_L is basically resistance offered by external load. So, R_L is external load which you see in front of you. And This is the MOSFET current source.

So, I am assuming this to be an ideal current source, right. So, its output impedance is infinitely large and then what I am trying to do is, its corresponding resistance looking through the source side is given by this. Now, why I am applying, why I am adding this here, the reason is very simple, that since no current is flowing through this point because it is a gate terminal.

No current, I can safely join the Gate terminal to this particular point, without violating any Kirchhoff's law. Because, there is no current flowing through these two arms. So, what is the net equivalent circuit, I have r_0 here 1 by g_m R_L and a current here which is basically an ideal current source and I get V_{sig} at this particular point, right.

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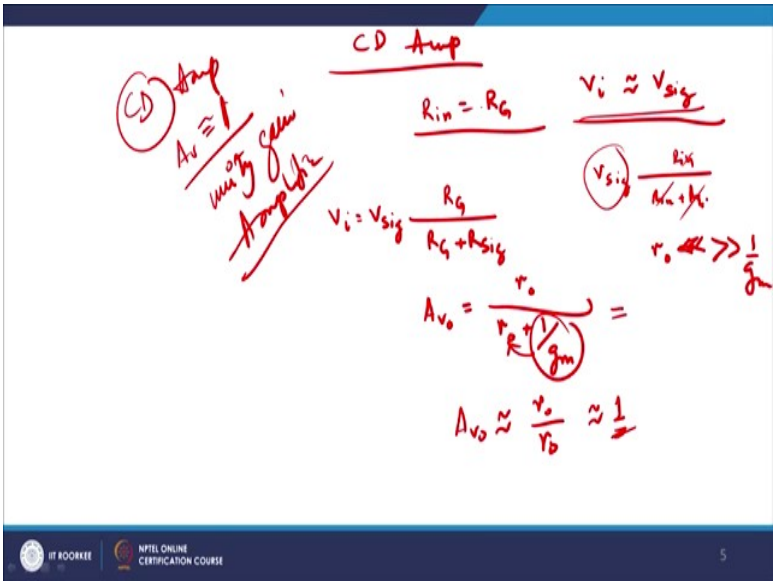

Now, let me explain to you the CD (Common Drain Amplifier), what you get is R_{in} equals to R_G the gate voltage, of course, and Vi therefore will be approximately equals to V_{sig}, and the reason is that, if you remember the concept was that your, if you remember in previous term or previous discussion, we saw that V_{sig} was actually getting divided by R_{in} and R_{in} plus R_G. Now, if R_{in} is relatively very large this cancels off and therefore I get V_i equals to V_{sig}.

So, under the condition that your repeat impedance is relatively very high, I automatically get my V_i equals to V_{sig}. So, whatever V_{sig} you are giving, say you are giving a 2 volt supply, 2 volt will apply at the Gate side of MOS device. With this knowledge, I can write down V_i equals to V_{sig}, right, R_G upon R_G plus R_{sig}, right. So, if you solve it I get A_{v0} to be equals to r_0 divided by r_0 plus 1 by g_m. And therefore, if you see, sorry it is very-very large as compared to 1 by g_m, right.

This r0 which is primarily because of the CLM phenomena is very-very large compared to 1 by gm. So, I can safely write down that Av0 will be approximately equals to r0 by r0 because this will be very small as compared to r0. And therefore, I can safely write down this to be equals to 1. Therefore, I can safely say that the CD amplifier (Common Drain Amplifier) is having a Gain of unity which is basically a Unity Gain Amplifier. This is basically a Unity Gain Amplifier, right. This is Unity Gain Amplifier which you see. So, it is basically uses a buffer, right.

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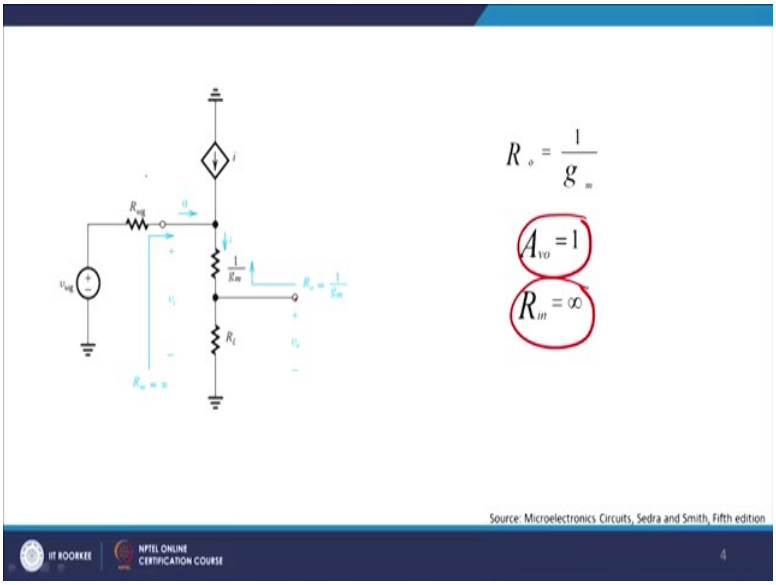

Now, if you come here therefore, you see A_{v0} is 1, R_{in} is infinity for reasons which you have already understood by now because, R_{in} is infinity why? Because you are actually seeing from the Gate side. So, as I discussed with you infinity. R_o is basically the impedance looking from the drain side onto the device.

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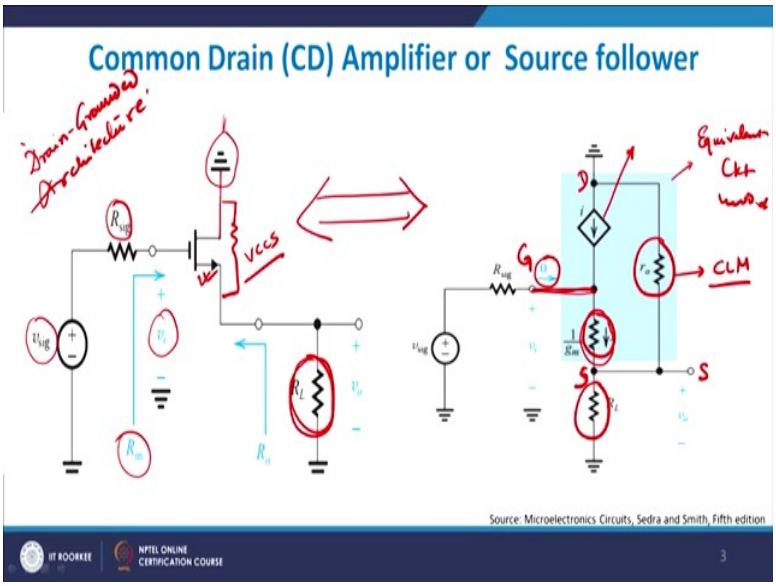

So, if you come back here, you are looking from the Drain side onto the device, means you are looking from this side onto this side which is nothing but 1 by g_m as we discussed earlier.

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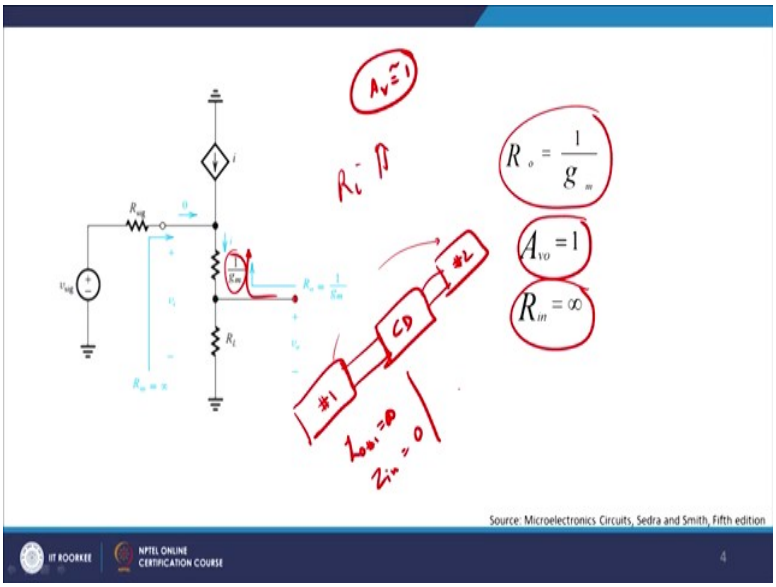

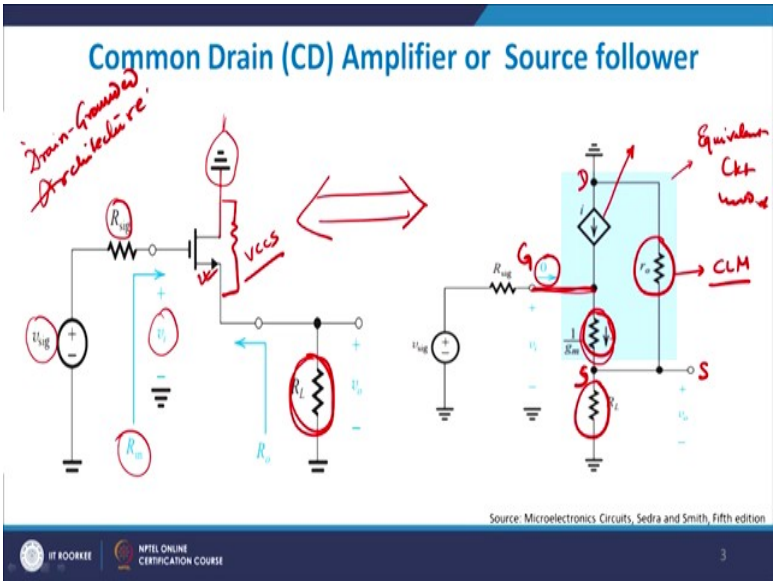

If you are looking at the output here the equivalent Circuit model, If you are looking from this, then this is my output and then looking into this region, right, from the Gain side, not from the drain side, sorry. I will just explain to you, this is my output right, so you are looking from this side. Looking from this side is basically looking from the source end of the device. Source end of the device means 1 by g_m. So, I get R_0 equals to 1 by g_m, right. So, if you want to use it as a impedance matching purposes, you can do that, provided so this will be somewhere sitting in the buffer of IU design, right. It can be used as a buffer.

Why? Because since its A_v is approximately equals to 1, it does not give you any Gain. But, what it does is, its input impedance is relatively very high, R_i is relatively very high, so if I have one block here and another block, this is my, I have another block here. So, this is my CD right, since it is input impedance is infinite, the output impedance of previous stage, so

this is stage number 1 and this is stage number 2 and you want to have the maximum signal to be transferred from stage 1 to stage 2.

Then, if the output impedance of stage 1, Z_{out} of stage 1 is infinitely large, then you connect this to this very easily because, input impedance of CD is infinitely large. And if I can connect to the, like this, then CD drives stage 2 whose input impedance is 0. And therefore, I can have a maximum power being transferred from 1 to 2. And therefore, reliability is not a major question provided you have a CD gap in between them, right.

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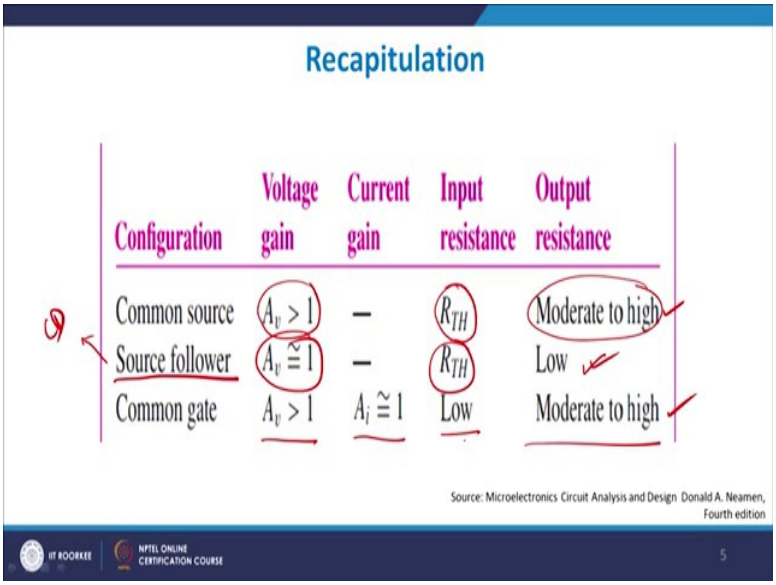

With this knowledge, we have almost done the most part of the design functionality of the Common Gate, Common Drain. Let me just recapitulate therefore all the 3 configuration to you. The first is Common Source, as I discussed with you, obviously its A_v is much larger than 1, right. Input impedance is the Thevenin equivalent of the total resistance offered by the device. Output resistance is moderate to high. We just now saw source, Common gate A_v is greater than 1, current gain is approximately 1, input resistance is low and moderate to high. Ok, Common Drain this is also referred to as CD, Common Drain is basically a source follower.

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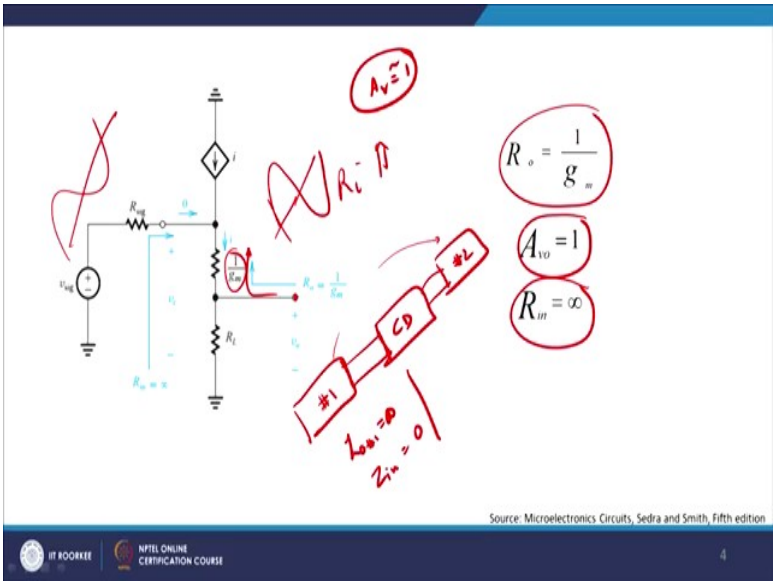

I will explain to you, why it is source follower. Just a minute! Source follower primarily mean that, whatever voltage you give on the source side, right. Exactly same appears across the output. So, source follower means whatever input you are giving in the source side, right. Exactly same thing appears in the output side without any gain or loss, because your Av equals to 1. Therefore, this is also referred to as a source follower.

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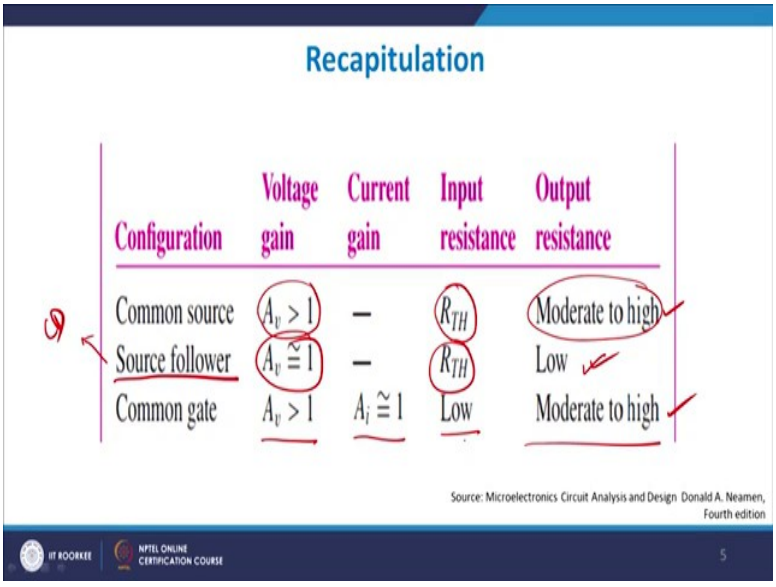

Configuration	Voltage gain	Current gain	Input resistance	Output resistance
Common source	$A_v > 1$	–	R_{TH}	Moderate to high
Source follower	$A_v \cong 1$	–	R_{TH}	Low
Common gate	$A_v > 1$	$A_i \cong 1$	Low	Moderate to high

How do you define a source follower? Source follower is that the signal on the source side of a device will be exactly equals to the input signal and therefore it is also referred to as a source follower with A_v approximately equals to one, right. Gain is approximately equals to.

So, Common source, Common gate, both are very high Gain out of which Common source has got much higher Gain.

Output impedance is relatively high for both of them. But, for Source follower the output impedance is low because it is 1 by gm and input impedance is also relatively small which you see in front of you. So, what we have done till now therefore is that, we have finished with configurations of Common gate, Common source and we have also seen into the fact of Z_{in} and Z_{out}. Therefore, we are now in a position to use these MOS devices under various configurations.

So, if I want a high gain fix it to Common source. I don't want a high gain, I want only the impedance matching, do Common drain or Source follower. If I want to go for moderate, low input impedance, go for Common gate structure, right. And therefore, you will be able to handle all of them independently in order to design it. With these words, I thank you for your patience hearing. Thank you!!!