Microelectronics: Devices to Circuits
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Lecture - 28
CMOS CS/CG/CD Amplifier Configuration

Hello and welcome to the NPTEL online course on Microelectronics: Devices to Circuits. In our previous file or previous have understood what is known as the small signal model of the MOS device; wherein he also understood as π; hybrid π model and what is a T model.

So for both MOS device why was it important? Reason was that whenever you encounter a MOS device in a circuit you can replace it by the equivalent circuit model and then calculation of various gains and output gain, current, impedances becomes much easier. We have also seen that in a previous example of the previous slide that your MOS device is basically a voltage control current source, right. And therefore by using an external voltage source, which is gate to source my drain current flowing through the device can be changed, right.

What we will see today is basically the various configurations of amplifier and therefore the name of the topic of today's discussion is basically CS CG CD amplifier configuration, CS primarily means common source, CG means common gate and CD means common drain. They are also known as source grounded, gate grounded and drain grounded amplifier configuration. So these are all actually amplifier, which is, which is there with us.

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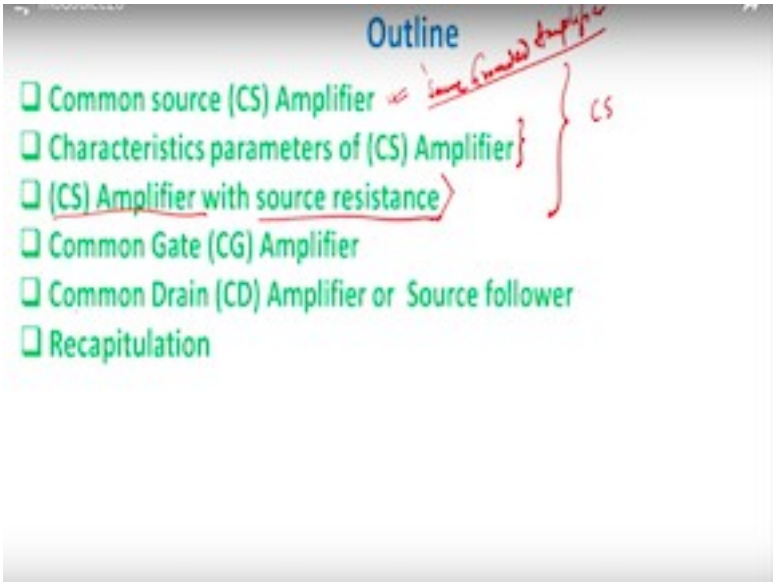

So let us see the first what will be the outline of my talk. The first thing, which we will be starting basically my common source amplifier, which is basically also known as source grounded. This is the most commonly used amplifier design across the world and for reasons we will discuss later on. We will see the various characteristics of this amplifier, which means we will be looking into the various output characteristics of this amplifier. As we have seen in our previous discussion if we apply a source resistance, right, source resistance, how does my CS amplifier change or how does its output characteristics change.

After we have understood these three important points regarding CS we go to common gate and then source follower or common drain, right. Common drain also referred as source follower and there are certain reasons, why we study CG and CD, but the most commonly used amplifier is basically the common source amplifier, right.

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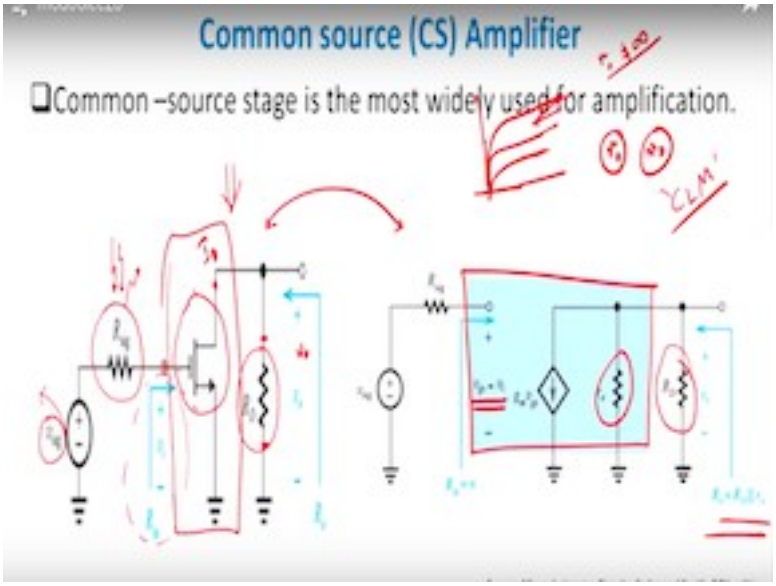

Common source amplifier is this, this is the diagram of a common source amplifier, right. This is the diagram of a common source. You see here you have a NMOS device which is this one active device, this is your output resistance of the input signals source, so this is the signal source which is there with me, right.

So assuming that I have already DC biased it, which means that I have already fed these devices with an external V_{DD} supply and source supply and biased it at saturation region so that its works as amplifier. This V signal is a small signal input voltage, which I am giving to the MOS device and R signal is basically my resistance offered by the voltage source. So a voltage sources please understand output impedance is very low, but in reality you might get some amount of resistance offered by it and that is given by R signal, right. So R signal therefore comes in series to V signal and V signal is the input voltage, which you give.

Then this r_D is the load resistance on external voltage resistance, which you see on the external world. So you see the effective V_{in} showed in this blue diagram in this blue curve is basically the V_{in} is the input voltage. So you see depending on the value of your R_{sig}, right, and this resistance r_G or r_D some part of V_{sig} will appear as V_i so not all of V_{sig} will appear as V_i or it might appear, but you will have a voltage divider network and therefore, we will see later on a part of V_{sig} will appear as V_i, so that is nothing but V_{gs} because source is grounded and whatever gate voltage you give will be basically your gate to source voltage. That will generator a current I_D, that current

I_D multiplied by this r_D is basically the voltage drop V_0, which you get and therefore that will be the output voltage, which you see, fine.

With this knowledge you have gained till now let me therefore do a matching of one to one matching between the actual circuit and the equivalent circuit model. So, what I do? I replace this MOS device here, this device here by its equivalent circuit which you see is this one. Please understand this is very very important to how you are replacing it. You are replacing it, why? Because please understand that $G_m V_{gs}$, this one is nothing but the current source, its the drain current of this MOS device. So I have the MOS device whose applied input voltage is approximately equals to V_{gs}, why? Because input voltage I am giving here, gate to source voltage input voltage and therefore I get $g_m V_{gs}$ is the drain current.

We have also understood in the previous, when we were discussing the small signal was that I will always have a r_o which is the output impedance of the device by virtue of the fact that your output will be slightly CLM. You will have always a channel in modulation phenomena and therefore at this point, at this point if you want to find out ∂I_D you will always have r_0 which is not equal to infinity, but typically a relatively a large value will be there, right, and that is what is r_0 is here.

So this r_0 primarily comes out because of CLM, which means that assuming that my device, which is a MOS device here is behaving like a non-ideal current source and therefore I will have this r_0. This r_D is the applied drain resistance in the output side or the load resistance whatever you see. So the effective resistance seen by the output world is nothing but r_D parallel to r_0, fine. This is r_D parallel to r_0, which you see and therefore this r_D parallel to r_0.

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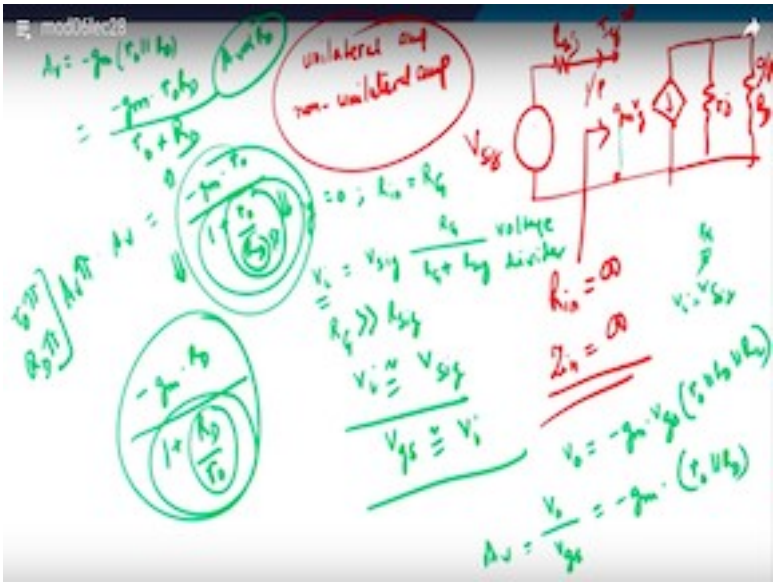

So let me just discuss with you that how will I look into the same facts, so let me draw for you this diagram, this diagram if you look very carefully then I will have signal here, right. I will have R signal here, right, and then I will have $G_m V_{gs}$, right, as a current source and then I will have r_0 and then I will obviously have r_D, with us right. This is what we have learnt till now and this is what you get, so this is your V_{sig}, this is your R_{sig}.

Please understand therefore your input impedance is actually infinity, why? Because your gate current will be 0, why gate current will be 0? Because see, where you are inserting your current or you are inserting it on the gate side of your MOS device, the gate is separated from the channel by a oxide layer or a thick oxide layer, right. This oxide layer is primarily if you look very carefully is a dielectric material of course and therefore I would not expect to see any current flowing through the MOS device as a gate current.

And therefore, looking from the gate side which is the input side your impedance will be very large so you are Z_{in} will be typically infinity, ideally it will be infinity so that, therefore, I keep it open input side is kept open, right. The input side is kept open this is the input side and this is my output side. Input side is kept open.

With this knowledge let me define what is, there is a term what is, known as unilateral and then you have another type of amplifier which is non-unilateral. The meaning of unilateral is that if there is no feedback between output and input, which means that

the effect of output impedance, right, does not load your input impedance and vice versa then we define that to be as a unilateral.

If there is a feedback loop which tells me that, no if I start loading the output, loading means I increase the value or decrease the value of your load resistance then your impedance; input impedance also changes, we define that to be as a non-unilateral amplifier, right.

So we have two types of amplifier typically, amplifier and this is one is unilateral amplifier and we have a non-unilateral amplifier. So if have a non-unilateral amplifier it means that if I change the output I would expect to see a change in the input by some closed loop control, right, whereas unilateral amplifier; both are totally different.

So as you can see since my input impedance is infinitely large actually my input does not talk with the output direct and as a result you will actually see that there is no change in the value of your input impedance because of the change in the output impedance.

Now with this knowledge let me therefore start doing the derivation for the gain for the, for the CS stage design and let us see how it works out. We discuss just now that of course your gate current will be 0 and therefore your input resistance will be approximately equal to the gate resistance, which means that whatever your input resistance is there will be equal to gate resistance therefore I can safely write down V_i equals to V_{sig}, right. R_G upon R_G plus R_{sig}, why?

Because R_G is a resistance which is the gate resistance which you see here, I am assuming it to be infinity but let us assume that it is not infinity at this stage it is having a finite value then we define V_i to be equals to, so you see if R_G is infinite value, right, if it is infinite value then this denominator will be at actually equals to just, if you look the denominator will be just R_G by R_G. So R_G R_G will cancel and V_i will be equals to V_{sig}, right and that is true also.

That means if your ideally, if your device, MOS device would have shown you an infinite resistance my input signal and my actual signal given by the voltage source will be exactly equal to each other, but since they are not I will have a voltage divider,

voltage divider network here and therefore gives me a value V_i here, right, but since my R_G is much larger as compared to R_{sig}, I will automatically get that V_i is approximately equals to V_{sig}, right, and therefore we can safely write down V_{gs} is approximately equals to V_i, right. So whatever you give the V_i that will be equals to V_{gs} as such, right.

With this knowledge we have already if you remember from my previous discussion that A_V voltage gain was equal to G_M times r_D, with that knowledge let me see how it works out, let me suppose I want to find out V_o, output voltage, it will be minus gm times, right. V_{gs} times R_o parallel to R_D parallel to R_L, R_L is the load resistance, there must be some load resistance in the output side and let me suppose this is there.

So, if you want to find out gain so it will be V_0 by V_{gs} will be nothing but g_m r_D, so g_m times r_0 parallel to r_D assuming that R_L is very very large, load resistance is very very large as compared to both of them. This into consideration, this is nothing but A_V, voltage gain, right. So I get voltage gain therefore A_V for common source amplifier is g_m times, right r_o parallel to r_D and therefore if you solve it, I get minus g_m times r_o R_D divided by r_o plus R_D, is it clear?

So if you want to find out the effect of R_D for example then just simply divide the numerator and denominator by R_D and you get what, you get minus g_m times r_o divided by 1 plus r_o by R_D. So if you increase the value of R_D, right, this quantity will decrease and therefore this quantity will decrease and therefore this whole quantity will do what? It will increase and therefore your gain will become larger, so therefore, gain is directly proportional to R_D as we have already learnt. Similarly gain is also proportional to the value of g_m.

Let us see what happens to r_o, right, again the same concept will come, if you divide r_o, I get g_m times R_D divided by 1 plus R_D by r_o. So if R_D increases, this decreases, this decreases, this increases. So even if r_o increases or R_D increases I will automatically get a higher gain with me, fine. So this is what we get overall gain, which you see.

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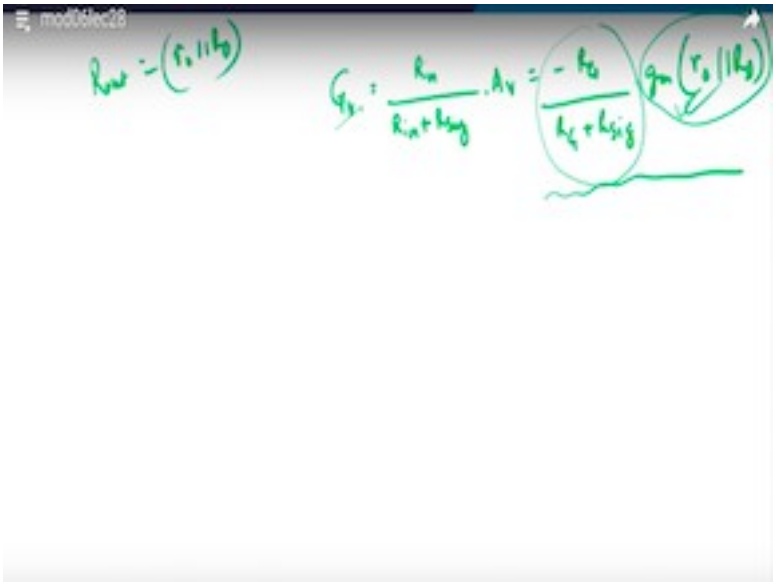

Now, if you want to find out the overall gain, total gain of the system, then we write down G_v, which is the total gain to be equals to R_{in} upon R_{in} plus R signal into A_v which is equals to minus R_G times R_G plus R_{sig} into g_m times r_o parallel to R_D, right and therefore this is this gives you the value of your overall gain system. So this is the gain due to the device itself and this is the gain due to the circuit itself and therefore I get this, but as I discussed with you overall, since R_G is very very large this will cancel off with each other and I will get over all gain to be equal to gm times, R_D with a negative sign, negative sign because you will get 180 degree phase shift between the drain and the gain of your device, right.

What is your R_{out} in this in this case, R_{out} will be therefore equals to r_o parallel to R_D, right, and that is what we get. So with this information let me see what we have understood until now.

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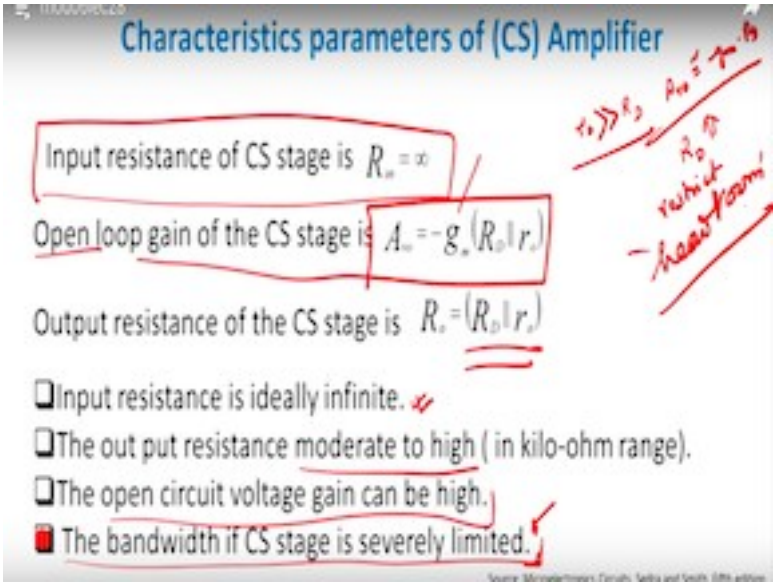

We have understood that the input resistance, right, in the CS stage is always equals to infinity right very important point, but it is infinity. Why is it infinity? And we have discussed point just now, why it is infinity? It is infinity because that you are applying to the gate side, right, you are applying to the gate side, once you have applied to the gate side, gate is open circuited; when gate is open circuited you automatically get input impedance to be infinitely large.

Now, how do you define the open loop gain? So what I am trying to tell you is that the gain, forget about open loop let us just discuss the gain here, the gain of a CS stage is given as minus g_m times R_D parallel to R_o and output impedance is given as R_D parallel to R_o, right. So as I discussed with you is ideally infinite, input impedance is infinite or the output impedance is moderate to high and the open circuit gain can be also be high depending on the value of g_m and the bandwidth of the CS stage is severely limited. We will not this discuss this at this stage but this for information so you can write down a term known as bandwidth of the CS stage is severally limited capacity.

We will discuss this when we discuss the switching behaviour, means we will go to frequency modeling of MOS devices. At this stage you can just keep this in mind that it is restricted. This will be, this last point which is here, which is this one the last point will dealt, when we discuss with you the modeling of the device for frequency

modeling; high frequency, moderate frequency and low frequency and there we try to find out the bandwidth of the MOS device.

But three things take away from all these discussion; infinite input impedance, moderately high output impedance, very large gain A_V and so on and so forth.

Now, as you can see therefore the price again the same thing discussed earlier also that let us suppose your R_D is suppose your r_o, right is very very large as compared to R_D then I can safely write down A_{V0} to be equals to approximately equals to minus g_m times R_D because they are in parallel and therefore again by the previous discussion if I increase R_D I restrict my head room, right, and therefore I am playing with there will be a chance of large order of discontinuity it the output side, ok.

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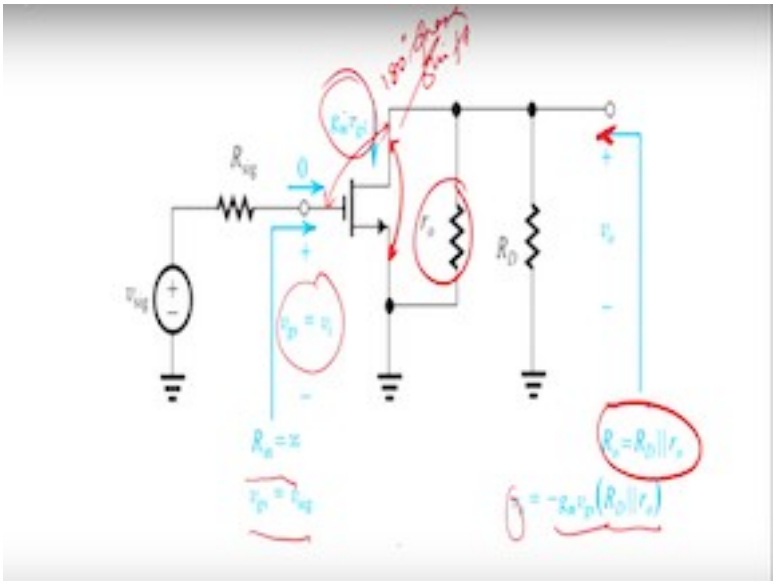

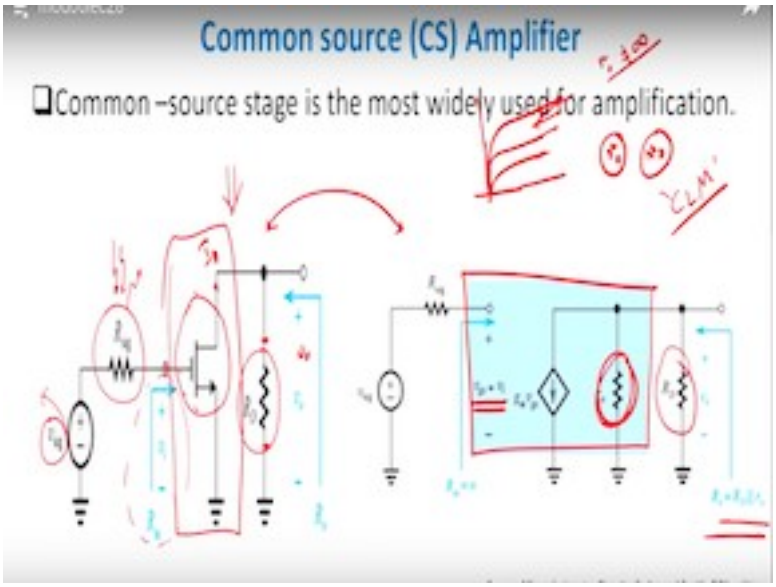

So this is how the CS amplifier looks like and let me come to the next stage also referred to as, so this is what I was talking about so you have, so you have your, just let me just come to the point, let me come, discuss the previous point as well as I was discussing with you, so you see V_{gs} is equals to V_i, so R_{in} equals to infinity and therefore since R_{in} equals to infinity and V_{gs} equals to V signal, drain current is nothing but g_m times V_{gs}, this is the output voltage which you see, which is equal to nothing but g_m V_{gs} multiplied by R_o, right, that is what is because current multiplied by output impedance will be the output voltage and therefore you get g_m times V_{gs} multiplied by R_D parallel to R_o is equal to V_o negative sign because gate and drain of a MOS device between these two, you will always have a 180 degree phase shift, right. Phase shift you will always have that is perfectly possible.

Now this also circuit takes into account the r_0 turn right it was not there in the previous discussion as you can see this was there in the previous one if you look at the previous one discussion this was grounded whereas this was also grounded but we have connected to the source showing that it is between these two nodes exactly which is happening, right. Now, so this is what we get a common source configuration.

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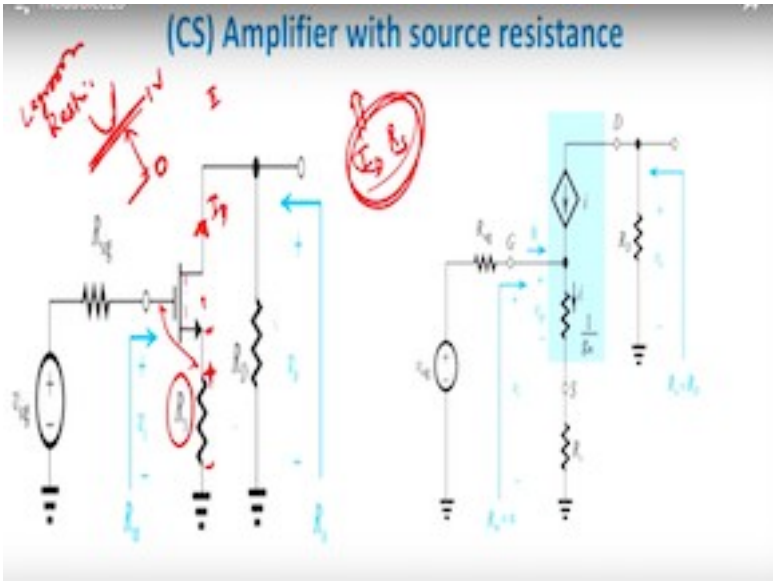

Now let me come to the common source amplifier with source degeneration resistance. So member what change we are doing, what change we are doing is we are replacing the source side which was initially grounded by a source resistance R_S. So this is source resistance R_S which is in series to the MOS device, right, so I have a MOS device here and I will put a series resistance here. I have discussed already with you why this is important in terms of application.

See it is important because as you make your R_S large or you make your source degeneration resistance large you end up having the voltage drop across this larger and larger, fine, because let us suppose current I_D is flowing, sorry I_D is flowing, when once the I_D is flowing through the circuit I_D multiplied by R_S is basically the voltage drop across R_S. So if your I_D increases, right, I_D R_S increases and therefore this voltage increases which in fact means that you are able to reverse bias this gate to source junction, fine.

Why? Because it is MOS device, n channel MOS device, so this is basically N and this is basically P, you have an N region here and since on the N side you are giving a positive bias you are reverse biasing it. Once you are reverse biasing it your current is falling down, so whatever current increase you got by virtue of some problem you will be able to reduce it by giving a negative feedback, right. So this is also a negative feedback.

Now, now so therefore, but therefore the problem what is the cost you pay for it is something like this. The cost you pay for it is now your leg room is restricted, leg room is restricted, why? Because out of the negative say you want to go to 0, you actually went to 0 at one point of time. I_D R_S is 1 volt, so out of 0 your 1 volt is already taken care of by I_D R_S, so your 1 volt here, so you can only go up to this much point. You cannot go below this much point. If you go you will have, you will have clipping, you will have wave-shipping problem so on and so forth.

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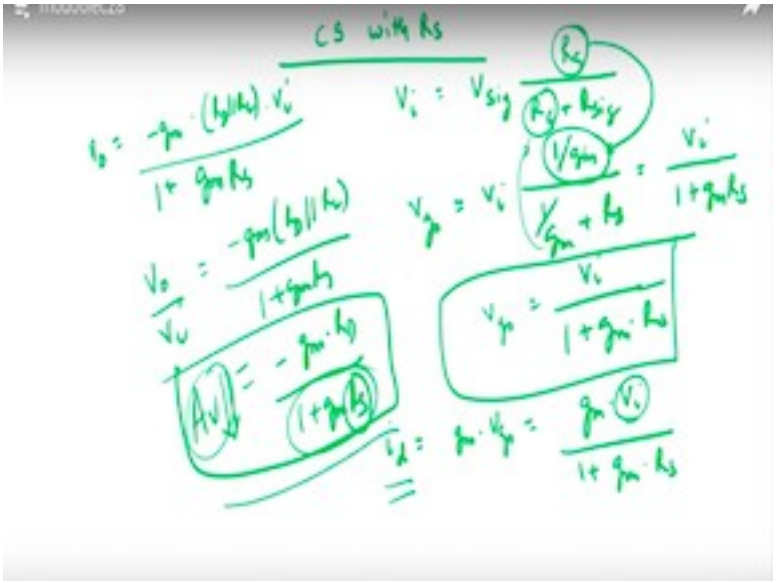

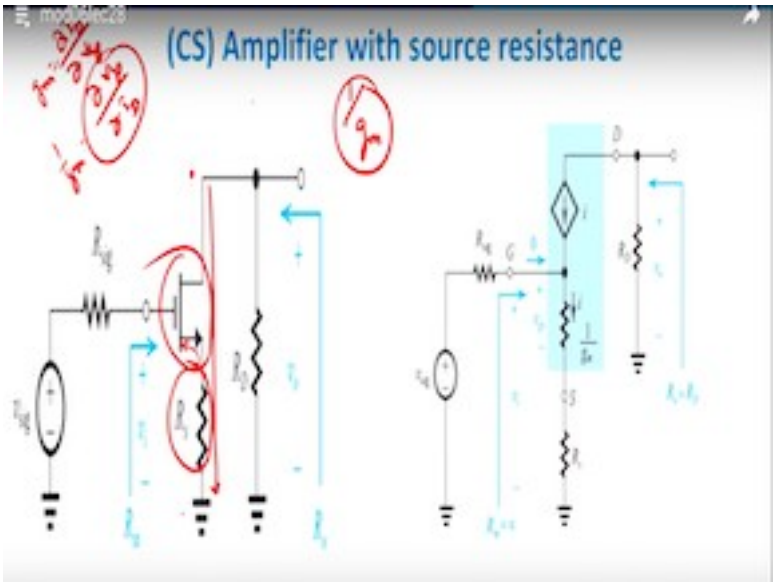

So this is a source degeneration resistance, which you see and I told you what is that advantage of source degeneration resistance, right. Let me therefore show you source degeneration, so CS stage with R_S; let me just do some small derivation here, CS

mean a common source with source degeneration resistance. Now let me write down V_i therefore again same thing, V_{sig} signal into R_G upon R_G plus R_{sig}, right.

As I discussed with you therefore V_{gs} is equals to V_i and this is quite interesting 1 by g_m upon 1 by g_m plus R_S. Now, this is quite interesting I will just explain to you from this discussion. See now the idea is that if you go from this point to this point. From this point to ground, right, you are encountering two resistances. One is R_S, right, another is the resistance offered by this device, right, and that offer is that looking from the source side the resistance offered is basically 1 by gm. Remember g_m was equals to g_m was $\partial I_D \partial V_{gs}$, right, so if you do 1 by g_m, it is ∂V_{gs} by ∂I_D, right.

So ∂V_{gs} ∂I_D primarily means that for the same change in the value of V_{gs}, how much I_D is changing? That can only be done provided you know what is the resistance offered so this is basically the resistance. So 1 by g_m is the resistance offered by the MOS device.

So therefore this is very very important you can solve it yourself and get the principle get this clear that obviously therefore I can replace this R_G by 1 by g_m, R_G by 1 by g_m so I am replacing this R_G by 1 by g_m which I was assuming to be infinite in the previous case I am assuming it to be 1 by g_m; yes and 1 by g_m will be relatively small quantity and therefore R_S will be there here and I will get something like this.

Now, from here this could be written as or this could be written as this could be written as V_i upon 1 plus g_m times R_S because if you cross multiply this will be 1 plus g_m R_S, this g_m will go in the numerator, right, and this g_m will cancel with this g_m and you will remain with this. So I get what? V_{gs} equals to V_i upon 1 plus g_m times R_S, right, this is the gate to source voltage.

Therefore, I can write down i_d, which is the drain current flowing to the device to be g_m times V_{gs}, V_{gs} is nothing but for this quantity g_m times V_i upon 1 plus g_m into R_S, right. This is what I get and therefore if I want to find out the value of V_0 output voltage I just have to multiply I_D with R_D; R_D parallel to R_L. So what I get I get minus g_m, right into R_D parallel to R_L output resistance multiplied by V_i, this V_i divided by 1 plus g_m times R_S, right.

And therefore, I can write down this V_0 to be equal to minus g_m times, right R_D parallel to R_L, so V_0 by V_i, 1 plus g_m R_S, so if you solve it I get minus g_m times R_D assuming that R_L is very very large quantity as compared to R_D I get 1 plus g_m R_S. This is your voltage gain, its minus g_m R_D upon 1 plus g_m R_S.

So you see as compared to CS stage without source degeneration resistance, with source degeneration resistance your gain is actually fallen by a factor 1 plus g_m R_S, right, and that is quite an interesting observation or quite an interesting idea, that what has happened therefore is that once your, once you are increasing the value of a source degeneration resistance because you wanted to be more stable and you do not wanted to be going beyond a particular limit or you do not want to clip out output device what happens is that this increasing R_S will result in a reduced value of A_v or the gain will reduce, right and that is the price you pay for a reduced gain with higher R_S. So what we have learned therefore is that A_V will be given as minus g_m R_D upon 1 plus g_m R_S, right.

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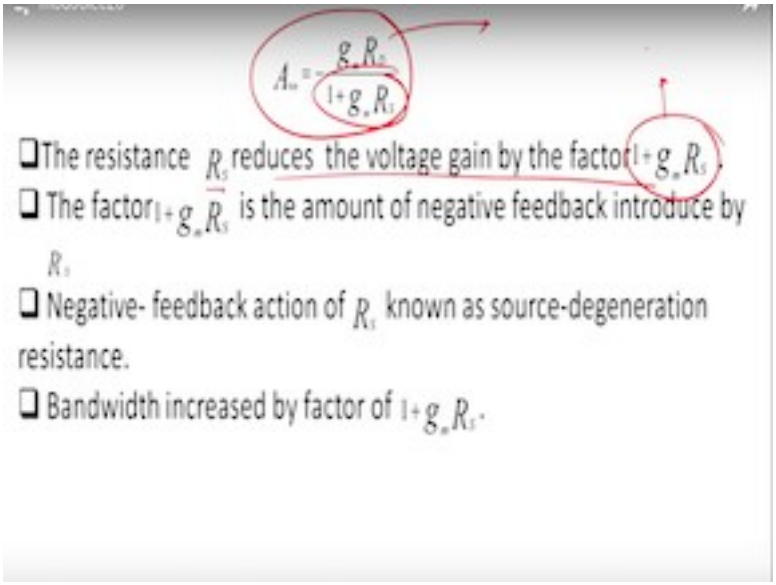

So let me come to this point and this is what I was talking about. So A_{V0} is equal to minus g_m R_D upon 1 plus g_m R_S and therefore, the resistance R_S reduces a voltage gain by a factor of 1 plus g_m R_S, this is the reduction. Initially we had g_m R_D now reduces by factor 1 plus g_m R_S.

So therefore, we define 1 plus g_m R_S is the amount of negative feedback which is introduced by R_S, right, so you have R_S resistance, the voltage drop across it will be

negative bias reverse biasing your source to channel contact, or source to gate contact and as a result you will have negative feedback, this negative feedback will result in what? Will result in a reduced gain. So what happens is that if the negative feedback is also known as, this R_S is known as source degeneration resistance, right, and the bandwidth increases by the factor of 1 plus $g_m R_S$. We will come to this later on in our discussion of frequency response. So this is what we get from common emitter or sorry common gate, sorry common source with source degeneration resistance.

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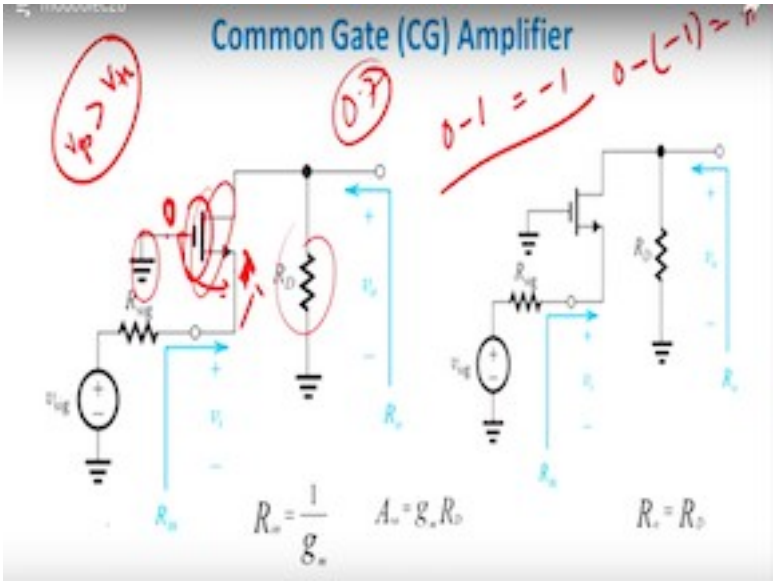

Now, let me come to common gate configuration, in common gate configuration again as I discussed with you the gate will be actually grounded so it is also known as gate grounded configuration, right. So I have a gate grounded configuration what is it means, that my gate is basically grounded which means that the gate is grounded here as you can see and therefore when get is grounded we automatically have a device and if it is an NMOS device it will be basically in a cut-off mode as such.

And therefore if you apply any signal here, right, what was the idea that V_{gs} should be great than V_{th} for the device to be your, but you see your gate is giving you 0 voltage here, so if your source voltage is positive, right, if its positive gate voltage which you are giving then gate to source voltage will always be negative, right.

Because let us suppose this is 2 volt here, and maybe 1 volt here, so 0 minus 1 will be equal to minus 1 volt, right, and therefore you need to switch it on to give, but in the

negative cycle suppose this is 1 volt here and sorry this is minus 1 volt here, 0 minus of minus 1 will be equal to +1 and this is larger than the given threshold voltage. Let us supposed threshold to be 0.7 in that case it will switch on and there will be current flow, right, and so therefore I have R_D and so and so forth.

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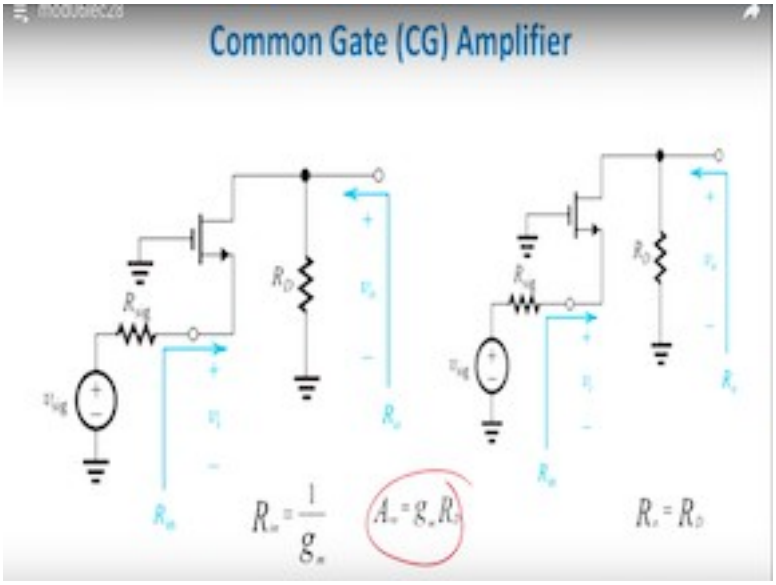

So let me therefore delete this option here or remove all the, remove all the inks here and you see for a common gate, if I have a common gate option or we, I will prove it maybe next time that in this case also I get $g_m R_D$ as my output resistance, but in this case quite interestingly you do not have a phase change of 180 degree. So the output will be exactly in phase with input side unlike in the CS stage or in the CD stage here you will not get the same profiling or the same this thing in this case, right.

So with this let me stop here today and explain what we have done, let me just recapitulate; we have done common source, we have done common source with source degeneration, we will take up common gate in the next turn and common drain in the next turn and that will finish the amplification action of a MOS device.

Since MOS devices is actually a device which is, which is, VCCS or a voltage controlled current source, we, output impedance of the device will be typically low but the input impedance will be typically very high, right, and therefore I can use it in the MOS device provided I am able to fix it in the saturation region of operational device. So with this let me thank you for your patient hearing until we meet next time. Goodbye!!!!