Microelectronics: Devices to Circuits
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Lecture - 27
Biasing of MOS Amplifier and its Behavior as Analog Switch – III

Hello and welcome to the NPTEL online course on Microelectronic: Devices to Circuits. In our previous interactions, we have seen that in order to amplify an input analog signal, we required to bias the MOS transistor in the saturation region of operation, which primarily means, that if you want that the amplification should be linear, which again means, that your amplification is independent of the input voltage, then we need to bias the MOS device, in the saturation region. And it should be well in the middle of saturation region, so that, even with the application of an input voltage, your output voltage does not make your Q-point, either go into the triode region or in the cut-off region, right? Otherwise, there will be a distortion in the output side.

We also saw one important point that your input signal should be as small as possible. So, that linearity is sustained for the I/O characteristics. We also kept this into mind, that while doing so, we require an external DC biasing and superimposed on the external DC biasing, we will have the input's AC signal, right? That is what we have learnt. And there are many types of biasing available to us, which we have already yesterday learned. For example, direct gate biasing. We have a feedback, drain gate feedback biasing, we have a source degeneration biasing and so on and so forth.

The best one option available to us was the source degeneration biasing, which if you, we, if we discussed in the previous turn, we saw that though your gain was reducing, but I had stabilized operation. There was a negative feedback, and therefore, whatever increase in the current was there will be reduced by virtue of a negative feedback, by virtue of the larger I_D available to you. So, this was what we have learned in our previous section.

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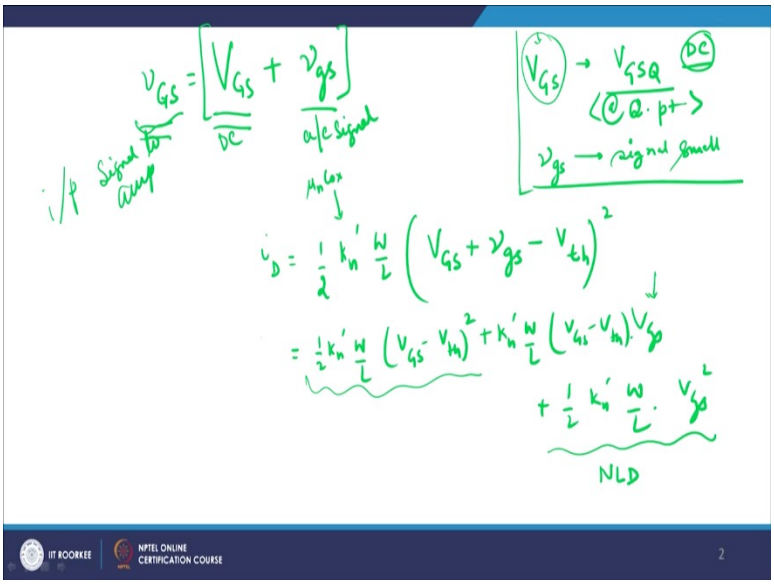

What we will learn today, is again the same continuation of my previous lecture and we will take up one important point. That now, let us suppose, we do have DC bias, which is fixing my MOS device into the saturation region, right. And let us suppose, that my saturation region, in the saturation region, let us suppose, that you do have, in the saturation region, the gate voltage is suppose V_{GS}, right. This is the, also defined as V_{GSQ}, let us suppose, which means that gate to source voltage at Q-point. So, this is at Q-point, right, at Q-point. So this is that Q-point.

Now, superimposed on that, so this is basically a DC bias, given by an external world, right. You already have the blocking capacitors or bypass capacitor, but this gives you a DC bias, which is basically V_{GS} right, gate to source voltage. Superimposed on that we will have, a small v_{gs}, which basically is the signal. So, this is your small signal, small signal voltage, which superimposes on the DC bias of v_{gs}, right. So, this is what, what we try to do. And therefore, we can safely write down V_{GS} is equals to V_{GS} plus v_{gs}, which means that, this is actually applied signal to the amplifier, is composed of one DC bias right, this is the DC bias component and this is the AC signal which you are giving. This is the actual signal, signal to the amplifier, to amplifier right, amplifier input signal, this amplifier.

Now, what I should do is, I just need to feed this value, into our drain current equation assuming that it is already in the saturation. So, I can write down Id to be equals to, 1 by 2, K'_n, which is μ_n C oxide, into W by. So, this is basically your μ_n C oxide, W by L, right. And then, we write down in place of v_{gs} minus v_{gs}, V_{th}, we write down, V_{GS} plus v_{gs} minus V_{th} whole square. If, you break it open, because it is a, it is basically, if you want to break it open, I will get something this to be equals to half, K'_n W by L, V_{GS} minus V_{th} whole square, right, plus K'_n W by L V_{GS} minus V_{th}, into V_{gs} plus and then half K'_n W by L into V_{gs} square.

Now, if you look at the first term, well, there is no problem because in any case, it is the term of the current which you will get in the saturation, saturate case, which means if the device is in saturated case, this amount of the current will surely flow, you cannot remove this. The second term, current is a linear function of v_{gs}, so, also, we do not have any problem. But, third term is where the problem is.

We have a heavy non-linear distortion. And the reason being, that now your input (volt) current is a square function of your gate voltage, which means that, a small change in the input gate voltage will give rise to a large change in the value of output drain current. Now, therefore, your define this to be as, a one of the major non-linear distortions, distortions available to you, right.

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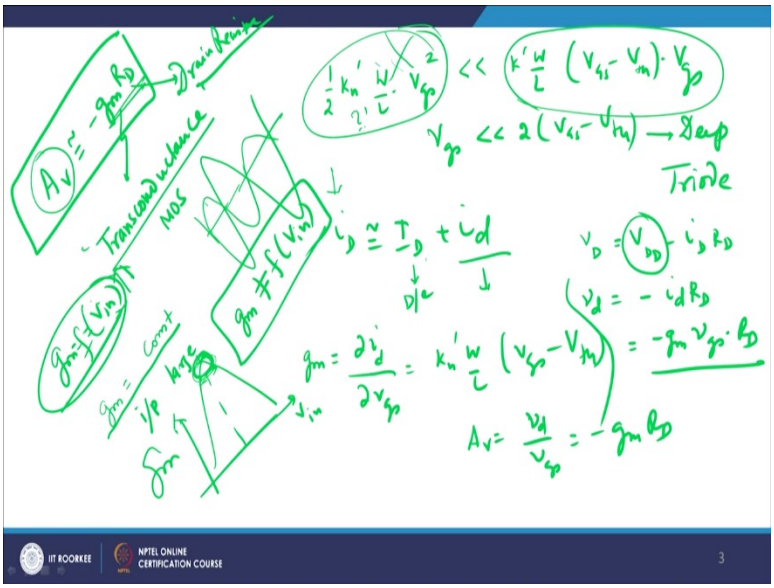

So, with this knowledge or with this idea, if I assume that half K'$_n$ right, W by L V_{gs} whole square is much smaller than K'$_n$, W by L, V_{GS} minus V_{th} into V_{gs}, which is the second term, and then, we can write down therefore, that v_{gs} is much smaller than 2 V_{GS} minus V_{th}. So, this is known as deep triode region, deep triode.

Then, I get i_d, is approximately equals to I_D plus i_d. So, this i_D is the actual output current which you see, from the amplifier. This I_D is the DC bias, DC current and this i_d is the current, due to the signal, input signal. So, if you find out g_m, which is the transconductance, then it is basically ∂i_d, right, ∂ v_{gs}. If, you solve it, I get K'$_n$, W by L, v_{gs} minus V_{th}, right. So, this is nothing, no problem because you need to just differentiate this problem.

This is gone because this is very, very small. See, see where are you operating? You are operating at very, very low value of v_{gs}, right. And therefore, when you squared it, this term can be negligible, can be neglected, can be removed. And therefore, this term comes out to be K'$_n$, W by L, v_{gs} minus V_{th}, right. Similarly, you all, we have already seen that V_D is equal to V_{DD} minus i_d R_d. And therefore, v_d can be written as minus i_d times R_d. Why? Very simple because what are you doing is that, you are replacing V_{DD} by output voltage, shorting it.

And therefore, I can right down this to be as minus g_m times v_{gs} times R_d, right. This equals to v_d. So, what is our gain? Gain is equals to v_d by v_{gs}, source to drain, is equal to minus g_m times R_d. So, this is what we get from all this discussion. That the overall gain for any amplifier is approximately equals to g_m times R_d, where gm is basically known as the transconductance, right, transconductance of the device, which device? The MOS device. And R_d is the drain resistance.

So, A_v, the minus sign, shows you that it is basically a, it is basically a 180 degrees phase shifted. So, if your input is something like this, your output will be something like this, right. And therefore, this is known as 180 degree phase shifted, as long as this is a small signal model, anyway.

Now, this assumption that, A_v equals to minus g_m times R_d, holds good when your g_m is typically, is considered to be independent of the value of V_{in}. In reality, you will see that, the transconductance g_m is again, in second order, we are not dealing it here. Second order, g_m is actually a strong function of V_{in}. We will learn that later on.

So, whenever you do a large signal modeling, so whenever you do a large signal modeling, your g_m actually increases or decreases, depending on the value of V_{in} which you are choosing, which means that, this transconductance value, which we have assumed to be constant, and therefore, g_m into R_d which is assumed to be constant, equals to A_v, will not hold good, when, when, when your input signal is having a large signal, right. Your g_m then starts to be a function of V_{in}.

Till now, we were assuming that g_m, is not a function of V_{in}, right. But in reality, we will see later on that, if you are having, if your V_{in} variation is very large, then gm becomes a function of V_{in}. Typically, if you plot, g_m versus V_{in}, it is something like this, right, something like this. If you plot, g_m versus V_{in}, right, very small region it is peaking and then it is dropping down drastically. We try to keep our input voltage in this range and therefore, we get the maximum gm available with us, right.

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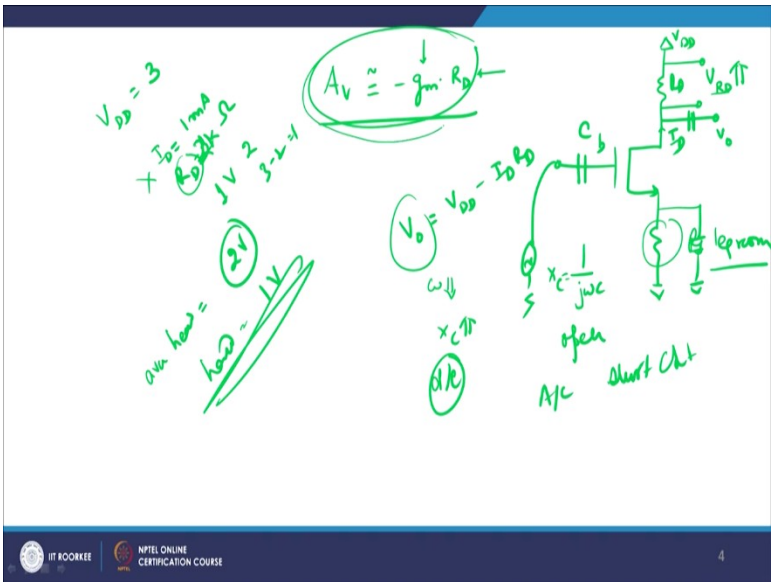

So, with this knowledge, we therefore, know that, for any amplification to occur, or to any amplification to be available to me, I will have, the voltage gain A_v to be approximately equals to g_m times R_d, where R_d is applied drain voltage, resistance. So, there are two ways of increasing the amplification of CA stage or any stage amplifier using MOS device. You either increase the value of gm or increase the value of R_d, right. But, let us see the cost; you will pay for, increasing the value of R_d.

Let us suppose, so your R_d was this one, right, and this is your MOS device, which is there and let us suppose you have source resistance at this point and this was V_{DD}, right. So, as I discussed with you, V zero, which is this one will be nothing but V_{DD} - I_D R_D, where R_D is this one and drain current I_D is flowing in this manner.

Now, the point is, therefore, the V zero is given. Now you see, if you, if you would increase the value of R_D, because you want a higher gain, you then, ensure that the drop across R_D, which is let us suppose V_{RD} is therefore, will increase. And therefore, the available headroom to you will reduce, right. So, let us suppose, your V_{DD} is say, 3 volts, right. And your I_D, I_D R_D is, I_D is 1 milliapm and R_D is 1 kilo ohms, right. Then, I get this; if you multiply these two, I will get 1, so you will get 1 volt, and therefore, 3 minus 1 volt is 2 volt.

So, available headroom to you is, available headroom is, headroom is 2 volt. If you increase R_d to say 3 ohms or maybe 2.5 ohms, 2 ohms, then, you will get, 2 into 1 is 2 and therefore, 3 minus 2 equals to 1, and I will get only 1 volt as a headroom. So, I can do only manipulations up to 1 volt so, my headroom gets reduced.

Similarly, if you go on increasing R_s, your leg rooms, leg rooms gets reduced. So, the cost you pay, for a higher gain is offset by a reduction in your head rooms, for an analog design. So, please understand, this very interesting and important property that do not think, by simply increasing the value of R_D, you will be able to achieve a larger gain, always. You will be able to achieve, but the cost you will pay, will be too much. So, therefore, it is always advisable to restrict yourself to very small signals of inputs, right, very small signals of input, right, this one.

Now, second thing, as I discussed with you yesterday, that this, I have a blocking, I have a blocking capacitor here, right, also I had a coupling capacitor. I had blocking capacitor here as well, right. Coupling or blocking, whatever you want to name it, you can name it. But, you can remember yesterday's talk, last part of the talk was that X_c or the trans, X_c means, reactive capacitance, of this one will be 1 by jwc.

So, when, w is very, very low, X_c is very, very large, which means that for a DC bias, this acts as a open circuit and, for AC bias, right, this act as a short circuit, capacitances. So, whenever, we are doing AC analysis, short, that is the reason, we say that, when we do AC analysis, please short all your capacitances, right. When you do a DC analysis, please open all your capacitances, so that it acts as an open circuit.

Now, with this idea or with this, we have therefore, recapitulated one point, that gain is this one. But, then gain depends also on g_m as well as R_D. Higher the value of R_D, more is the gain, but less is the headroom available to you to work with,

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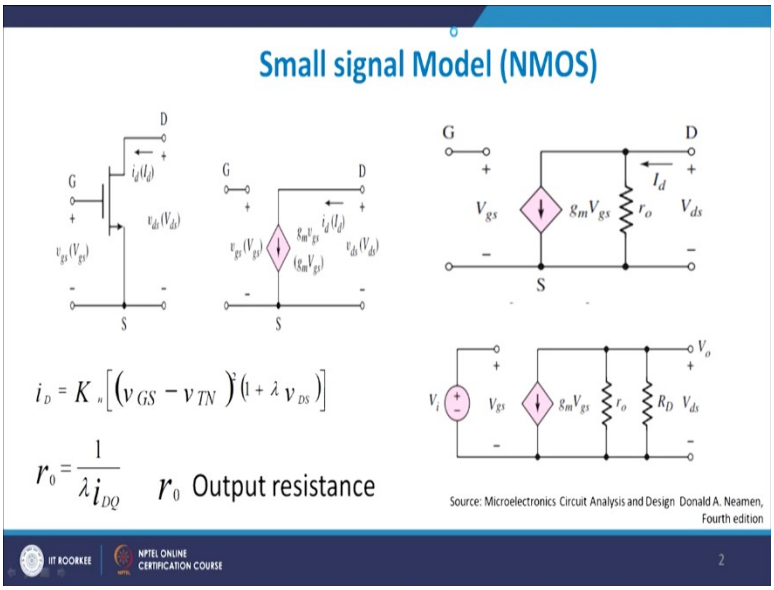

With this knowledge, let me come to, very important topic that is known as a small signal model of a device. So, we have understood NMOS, NMOSFET and let us, therefore, take the NMOSFET and see, if we can do small signal model, means by the input voltage is varying by very small.

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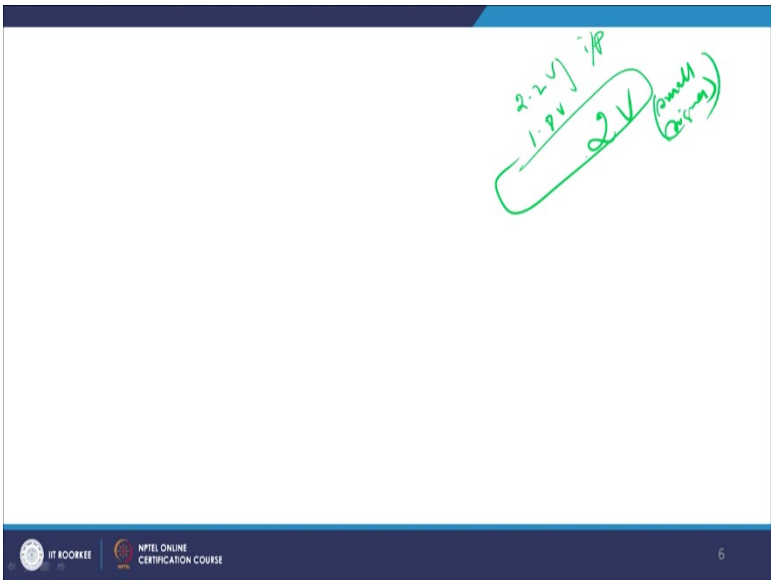

Typically, when we say small signal, there is no quantitative analysis as such, but typically what people expect is that, a plus minus, 10 percent, from Q-point, from Q-

point. That is will be defined as a small signal. So, if your Q-point is somewhere around 2 volts, suppose it is 2 volts, 2 volts, then it will be 2.2 to 1.8 volt will be the input swing. Then, we will define this to be as a, 2.2 will be defined as small signal. So, this will be defined as a small signal, right. So, I will have small signal, available with me, provided, this is true or this functionality is true.

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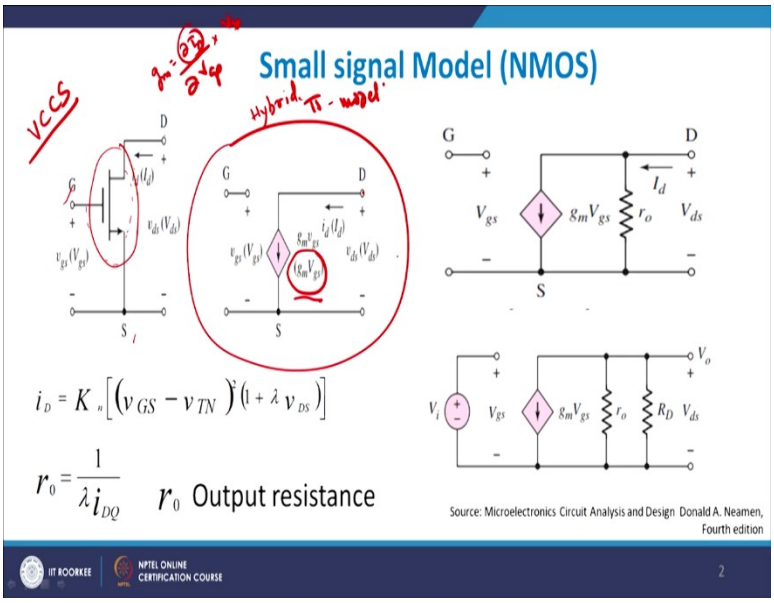

Now, let me come to you, the small signal model of the FET device. If you look here carefully, this is the N-MOSFET, which is in front of you, right. I have a current flowing which is a drain current. V_{ds}, is the drain to source voltage, which you see here. And you have a gate to source voltage, which is available at this particular point. So, it is basically a three terminal device gate, drain and source.

And therefore, as you can see, it is basically a voltage controlled current source. So, it is basically a V_{CCS}, right, it is basically a voltage controlled current source. Who is controlling, controlling this current, I_d, is v_{gs}. So, therefore, this is also referred to as a voltage controlled current source, right.

Now, so what we can do, simply is, I can, I can, make this transistor or this MOS device, as a ideal current source. And therefore, I can simply write down this to be as, a current source with $g_m V_{gs}$ as the current value, because, that is what we know. G_m was referred to

as ∂I_d ∂V_{gs}, remember, right. So, If, you multiply this with V_{gs}, I get simply, I_d, and therefore, this gives you the drain current.

And, therefore, on the drain side, I refer to this as g_m times V_{gs} and the gate is open. Why the gate is open, shown as open? Because please understand, it is basically a voltage source. A voltage source, in its equivalent form will always be open circuit because, a voltage source by definition, means that, its output impedance is zero, right. Its output impedance is zero, and will give you the same voltage, even if you draw any, any current, right.

So, therefore, a voltage source is always shown by an open circuited and a current source is, its equivalent form, if you want to find out, will be always shorted right; whenever you want to find out its equivalent form. So, I get this, so, this was my, this was my model. This is also referred to as a hybrid, hybrid π model, right. This reason, for the hybrid π, why, it is known as hybrid π model. But it is also referred to as a hybrid π model. So, we have understood why.

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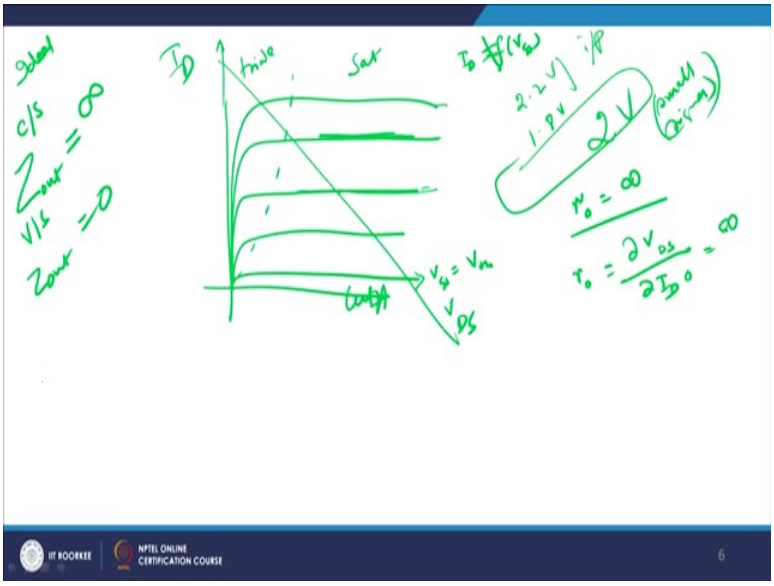

Now, let us understand, this was with the assumption, that my I-V characteristic of the MOS device is perfectly straight in the saturation region, which means that, it is absolutely, a perfect current source, in the saturation region. So, this was the saturation,

by definition this is saturation, this is triode and then if you go, like this, this is V_{gs} equals to V_{th}; this is cut-off.

So, you are biasing your device somewhere in the middle, by drawing the load lime, you are biasing somewhere here. But, then I am assuming that, this saturation current source is basically, a fully straight line. So, this is I_d versus V_{ds}. So, when this is a perfectly a straight line, I assume that, therefore, Id is not a function of V_{gs}, right. It is not a function of V_{gs}; it is a constant current source. If, that is so, what happens to your output impedance, will be infinitely large. Because, r_o or output impedance, will be referred to as ∂ V, V_{ds} by ∂ I_d.

Now, if you travel from this point to this point, even if you are varying in V_{ds}, your I_d is still, ∂ I_d is still zero. So, this is zero, R zero will be infinity large, right. So, therefore, a current source, therefore, let me write down a current source, an ideal current source will have, its Z_{out}, which is output impedance, to be infinitely large. A voltage source, a ideal voltage source, Z_{out}, will be equals to zero.

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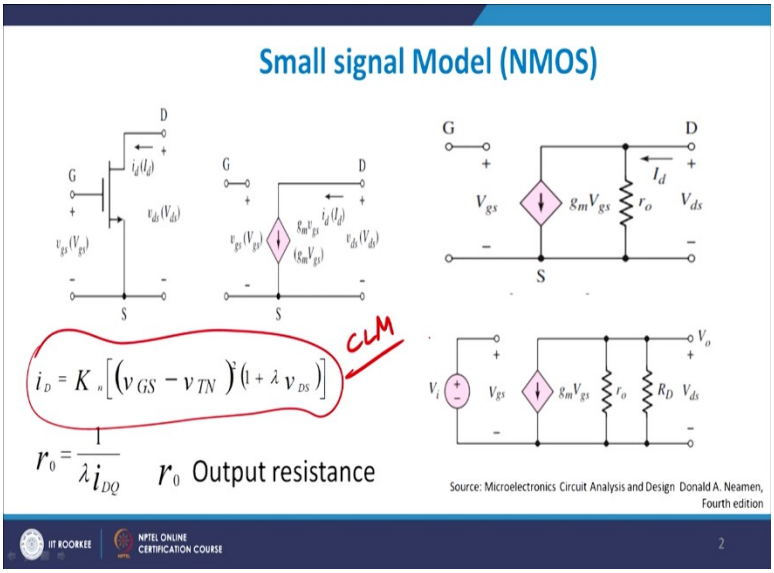

But, in reality as we have discussed in our previous turn or in our previous understanding, that I_d is actually depending on the value of V_{ds}, in the saturation, also, known as Channel

Length Modulation phenomena, right. We have discussed this point, when we were discussing MOS device physics as such.

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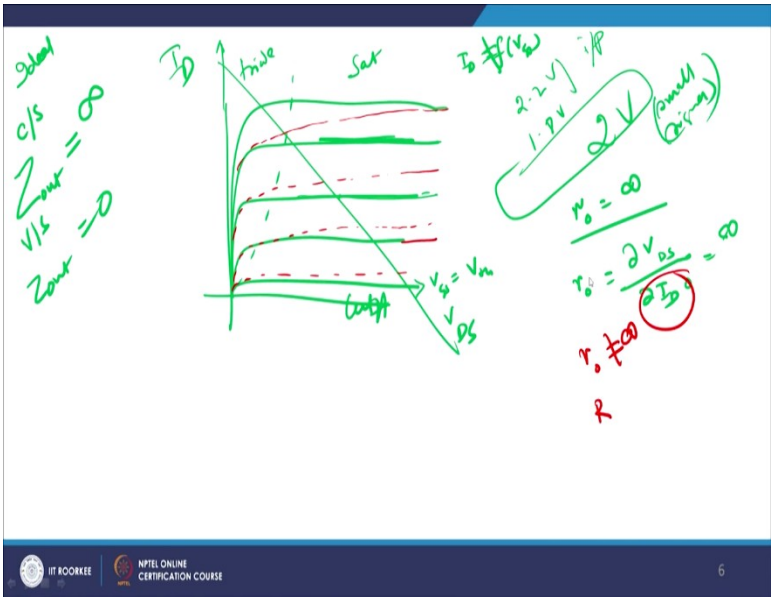

And therefore, due to Channel Length Modulation phenomena, what happens therefore is, that rather than this remaining, like perfectly, perfectly straight or perfectly constant, I actually start getting a small rise in the current, with increase. So, with increasing the value of V_d, V_{gs}, right, V_{ds}, I start getting a more and more current with me, right. So, this is higher values of V_{gs}, which means that now; since this is not a straight line and you do have a finite ∂, you do have a finite ∂I_d, I_d, therefore, r_0 will be, not, will not be equals to infinity, but will have a value, right, but will have a value; which in this case, we have considered to be r_0.

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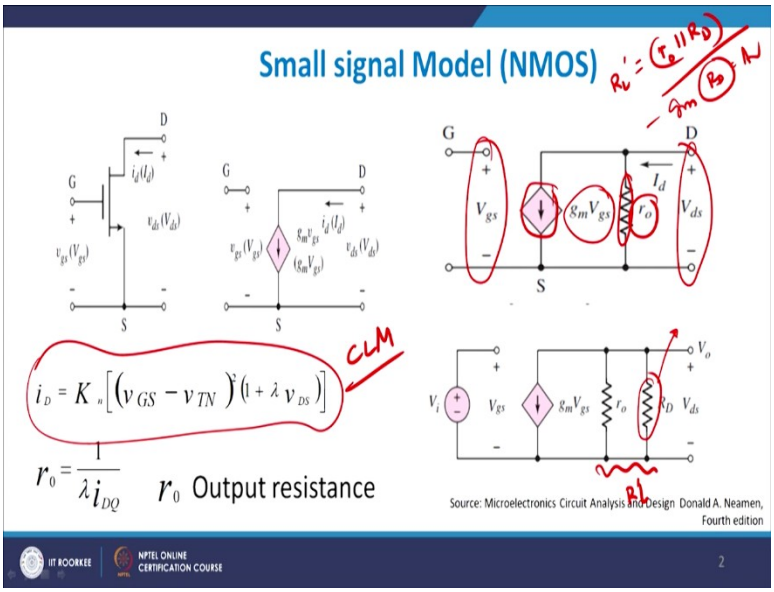

So, I just take r_0, in parallel to the current source here, where, r_0 is basically, the resistance offered by the device, when the device is operating in the saturation region, fine. And therefore, there will be a current I_d flowing here, there will be V_{ds} flowing here, and this $g_m V_{gs}$ is current.

So, if you, if you treat, gate, drain and source as three terminal gate, will be obviously open circuited, as we discussed. Drain, will be open circuited, but the drain will be terminating on to a current source, whose value is $g_m (V_h) V_{gs}$, followed by a resistance, which is in parallel to the current source, to prove that Channel Length Modulation phenomena is taking place, right.

Apart from this, you will also, automatically, have the drain current resistance, drain resistance, right. Why drain resistance? Any external resistance which you will be putting will be defined as drain resistance and you will always have the drain resistance, in the output path, right. And, this will give rise to a, change in the value of your, if your, output impedances. And this is what we learned from; we will discuss this in detail.

We will see that, since therefore, I can safely say, R'_L, let us suppose R'_L is basically this, R'_L, right, R'_L. Then R'_L is R_O parallel to R_D, right. And therefore, only less than the least resistance will, will appear with us, right. And therefore, only R_D will appear, because R_0 is typically very large, R_D will appear. And again, g_m times R_D, will be your A_v value, which you get for a small signal model, right.

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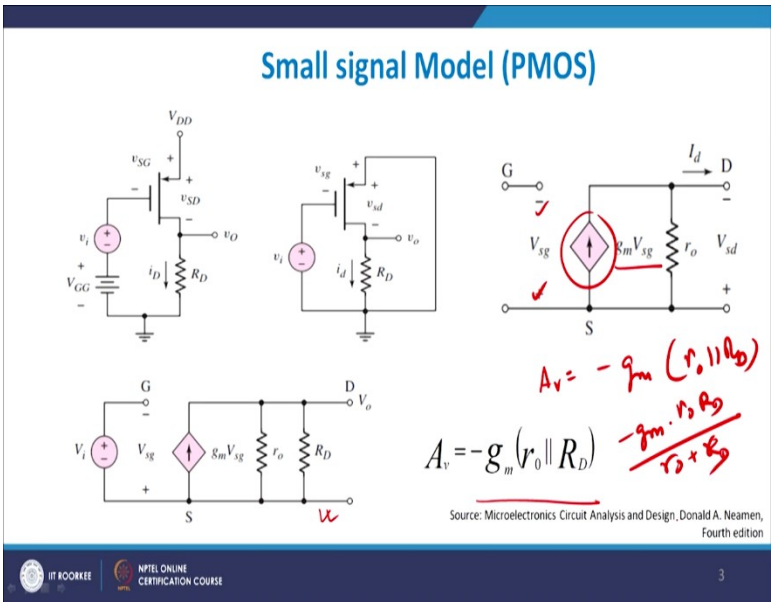

Let me explain to you for the PMOS model. The same thing, the same thing; though, just let me remove this, is exactly the same thing, but you have to see, that the current direction is just switched. So, you had a, sorry.

So, the current direction was initially this side, down and now if you look back, the current direction, is up. And, the gate to source voltage, also has changed between, positive and negative to, to negative and positive, right and therefore, we get V_{sd} to be equals to g_m times V_{sg} into r_0, you will get.

Similarly, if you put, a drain voltage outside, I get minus g_m times r_0 parallel to R_D. So, I get A_v to be equals to, minus g_m times r_0 parallel to R_D. So, if you solve it, I get minus g_m times r_0, R_d upon r_0 plus r_d, fine, you get this as your final value. So, I get, minus; so, I get what?

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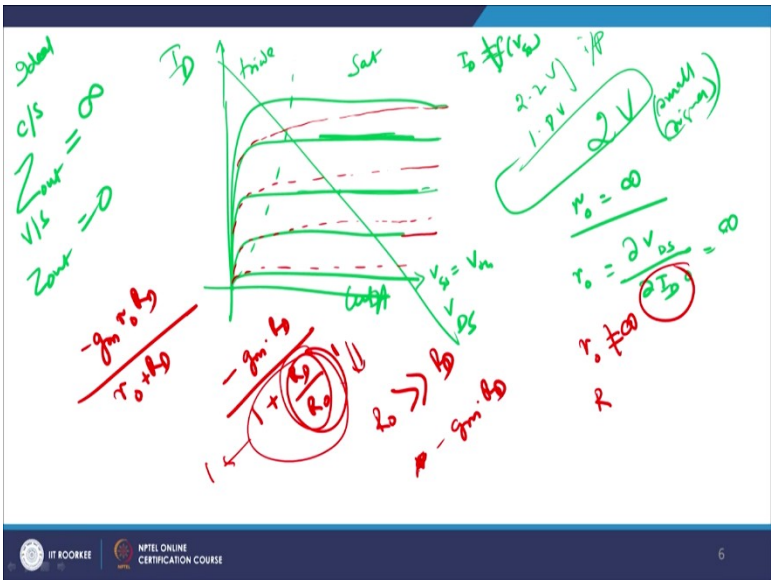

So, I get minus, minus g_m r $_0$, R_D divided by r $_0$ plus R_D. So, if you divide by say, R_D, numerator and denominator or r $_0$ by denominator and numerator, I get g_m R_D, divided by 1 plus R_D by R_O. Now, if your R_O is much, much (large), smaller as compared to R_D, then this, this whole quantity will be equal to 1, right, If, R_O is much, much larger as compared to R_D, then, this whole quantity will be much smaller, very low. And therefore, 1 plus very low quantity, will be approximately equals to 1. And therefore, I can safely write down this to be, equals to g_m times R_D with a negative sign, right.

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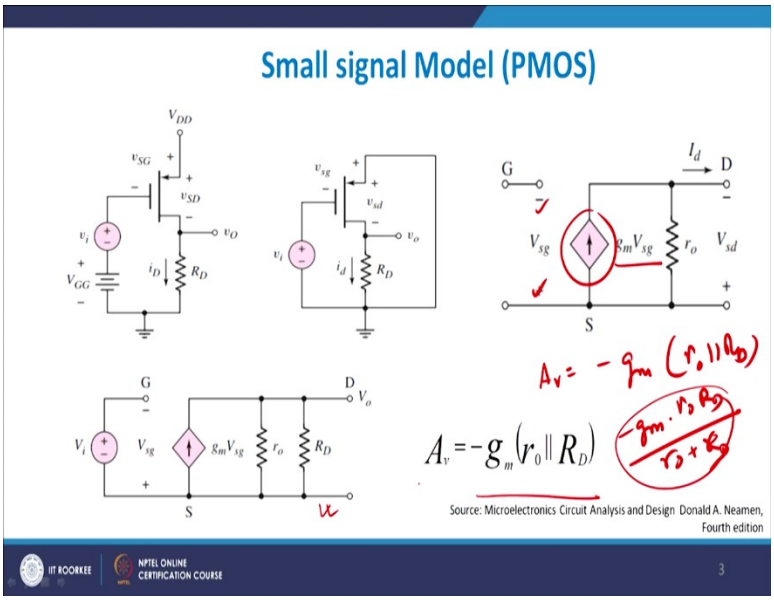

And, this is what we get here, that, A_v will be minus g_m times r_0 parallel R_D, where R_D is the applied drain resistance which you see.

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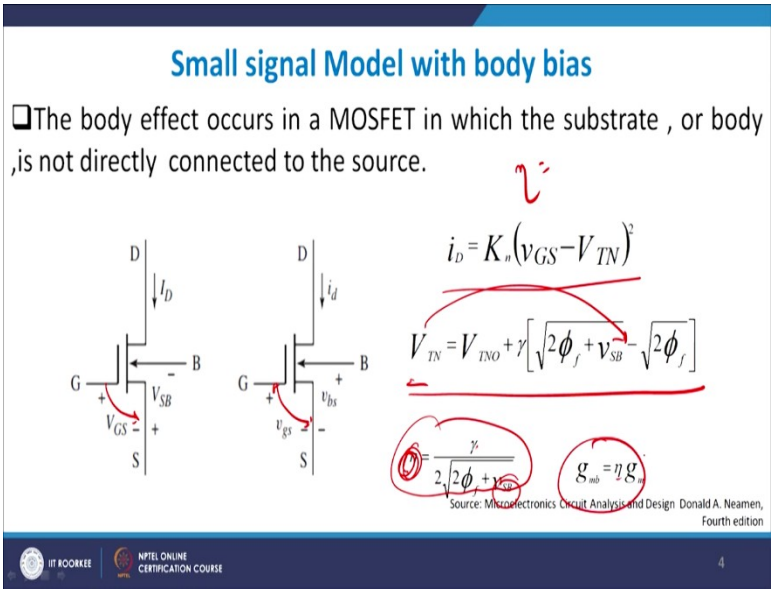

Now, let me also discuss with you, that if you remember, that a MOS transistor is not always, three terminal device. It is actually, a four terminal device, with substrate being the fourth terminal, right. This, we have already discussed earlier, that is known as body effect, right.

So, I had discussed with you, that i_D will be equal to K_n times v_{GSN} minus V_{TN}, v_{GS} gate to source of N device, gate to source of N device, this, minus V_{TN}, threshold voltage of N device. Now, threshold voltage of n-channel MOSFET is itself written in this manner, which means that it is a strong function of v_{sb}. And therefore, I can write a new term η to be equals to this; so there is a derivation, I am not doing it, in this interaction. But, I am doing a derivation, which tells me that η will be equals to γ upon 2phi F + v_{sb}.

So, if you vary v_{sb}, my η will change and as a result, you will expect to see g_{mb} to be n times, η times g_m. And therefore, on depending on the value of η, the g_{mb} means, transconductance with bulk, with bulk potential and g_m is transconductance only with the gate potential. So, I will see a change, in this case.

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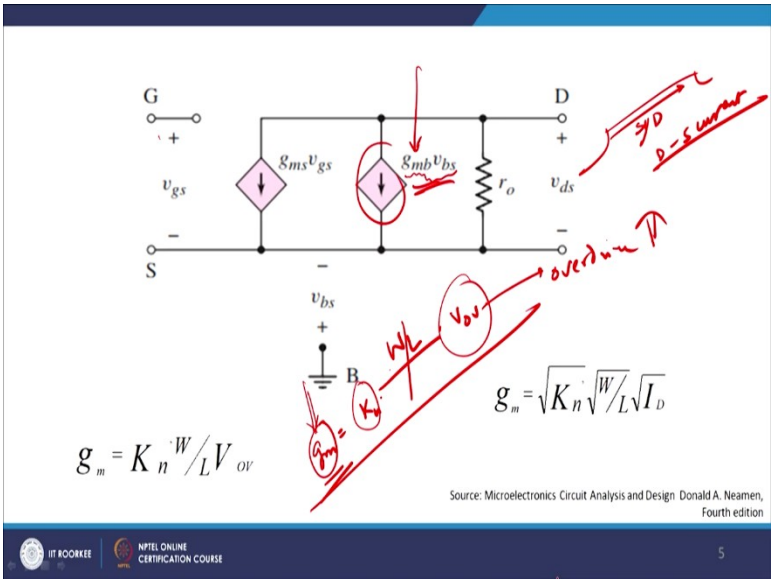

So, what I am done, therefore is, if you remember correctly in your precious discussions, my current is flowing in this direction, for source to drain, right, source to drain current is flowing, So this, so this is, the gate, drain and source. So, if you remember, this g_{mb} times v_{bs}, is nothing but the, again drain to source current, right, drain to source current. Because, there is no other way, the current can move.

Because, you are applying bias from the drain side, your source is grounded. So, all the charge particles generated, assuming, there is no bulk as such or the bulk potential is

relatively smaller or no change, then I will expect to see it, moving across source to bulk. That is what is happening here, I get g_{mb}.

So, g_{mb} is defined as a transconductance of the device, with substrate bias, right, substrate bias. Now, g_m, as I discussed with you will be referred to as K_n times WL, right, W by L into V overlap. So, K_n times W by L into V overlap, is actually equals to g_m, right. So, if you want to increase the value of g_m one is that straightforward, W by L ration, you make it higher. As you make my, W by L ratio higher, I get a larger current, and therefore, I get a larger gm for the same change in value of v_{sb}.

Second thing is, if you try to increase the overlap voltage, V overlap, right, or V, V over or even K_n, I should also get a larger value of g_m, right. So, your overdrive voltage is a large, I will expect to see g_m to be also very large, right. And, as a result, higher the overdrive, higher will be the transconductance of the devices itself.

So, let me take up MOS as analog switch, where we have already discussed, this point in detail, in our previous discussion. But, let me just; still reframe the whole network for you. As, I discussed with you, whenever my input is basically more than threshold voltage of the device, the device turns on, and, as a result, there is a direct path between V_{DD} and the capacitance. And, the capacitance gets to, starts to get charge and the charge, and the output voltage, goes from 0 to 1, right. Similarly, in the reverse bias, when your input voltage is negative, PMOS switches on, and output voltage, will therefore, go from 1, 0 to 1, because it is moving towards V_{DD}.

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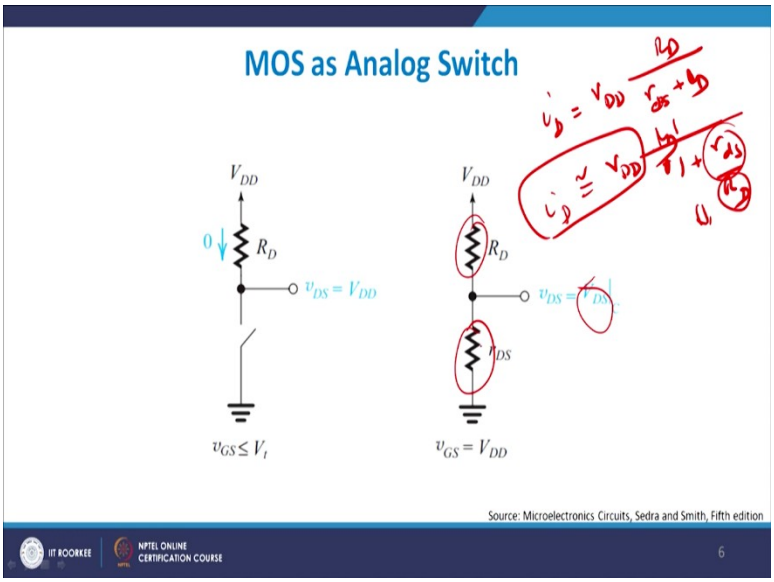

Now, assuming that, you are doing; assuming that you are having something like this here, then I can safely say that i_D, right, is basically equals to V_{DD} into R_D upon r_{ds} plus r_D, fine, voltage divider. So, V_{DD} divided by 1, if we divide by 1, 1 plus r_{ds} by R_D, right. If, your, R_D is very very small as compared to r_{ds}, right, this whole quantity can be neglected, and V_{DD}, i_D will be approximately equal to V_{DD}, approximately equals to V_{DD}, multiplied by R_D, multiplied by R_D.

So, if you see very carefully here, MOS is an analog switch, if you look very carefully, I have an R_D value and r_s value, coming into picture and therefore, v_{DS} drain to source voltage, is equals to V_{DS}, in the center frequency. And, r_{DS} is the resistance. So, it is basically known as two resistance model of a MOS device, right, and it depends upon the value of current flowing through this terminal, and value of voltage, at this particular point, because of this current, right.

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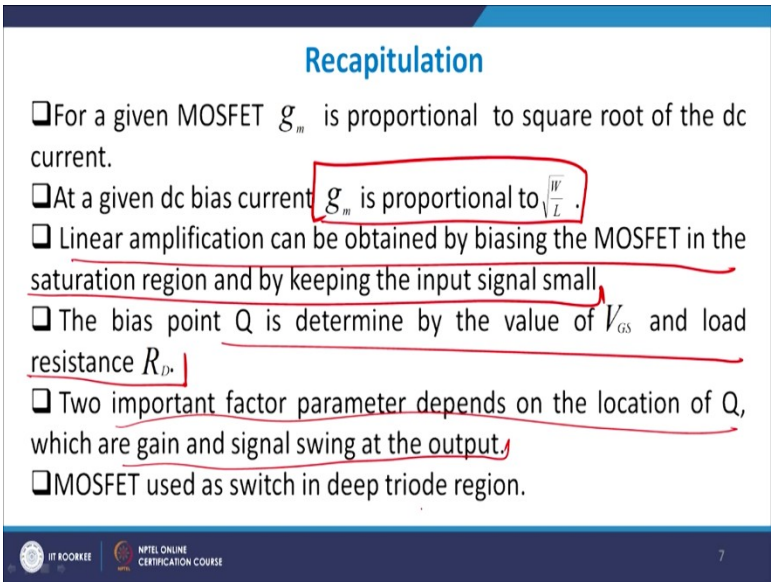

So, let me therefore, recapitulate what we have leaned till now, that transconductance is always proportional to square root of dc the current. This we get, in another means, but do not worry about it. But, transconductance primarily depends upon value of mobility W by L ratios and the square of the, square root of the dc current. Now, at any fixed dc value of current, g_m is always proportional to W by L root over, right, and this is an expected or an accepted fact across the world.

Linear amplification can be obtain by biasing the MOSFET in the saturation region and by keeping the input signal small. This, we have already discussed time and again, to remove the nonlinear distortions. Now, how you determined the value of Q-point? By using V_{GS} and R_D. R_D is the external parameter and V_{GS} is also the external parameter. But, how it switches on the MOS transistor, is basically the internal parameter. And, therefore the bias point Q, is determined by the value of V_{GS} and load resistance R_D, fine. And, it is the standard method of finding out the Q-point, technically.

Two important factors, decide the location of Q-point- what is the gain, what is the signal swing at the output, you got the point. Because, if your Q-point, is very close to the, either the saturation or cut-off, then even in the small change in the input voltage, I would expect to see, somewhere cut-off in your output voltage, And, as a result, it is not a good idea to have cut-off voltage available to you, right.

If, you want to use MOSFET as a switch, please bias it in the triode region. So, that is very, very important. You bias it, in deep triode, right, so, this will make you off, right. Is it alright? So, it will make you off and that gives you very good idea of the MOSFET can be actually used as an analog switch, right. And τ, as you all know, 0.69 R times C, is my typical, this thing, delay element for a switching diode, or a switching MOS device.

With this, let me finish, today's lecture and thank you, for your patient hearing. The next turn, we will look into the other facts, as far as this course is concerned. Thank you very much!!!!!!