Microelectronics: Devices to Circuits
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Lecture 26 - Biasing of Amplifier and its Behaviour as an analog switch-II

Hello everybody and welcome to the NPTEL online certification course on Microelectronics: Devices to Circuits.

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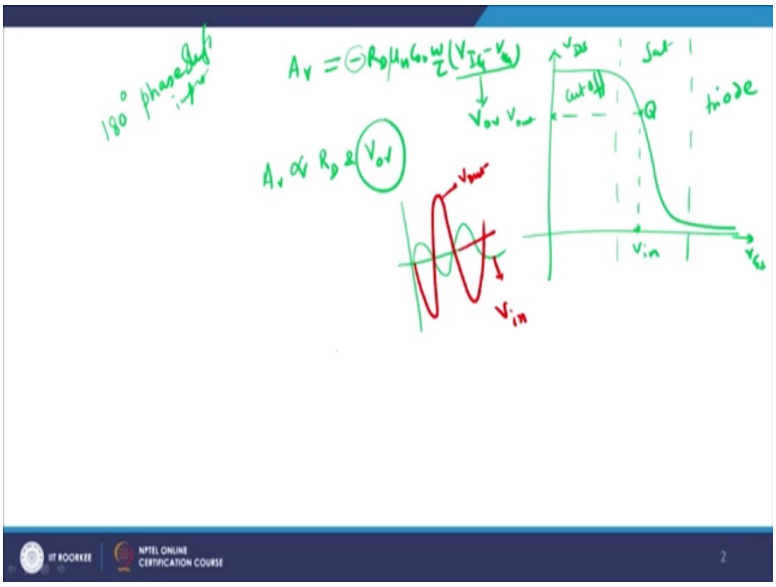

We will start from where we left in the previous turn, we had actually seen that the gain depends upon the overdrive and we saw from the previous turn that when the device is in saturation region, right when the device is actually in the saturation region then you do have a profile here and therefore if you look very carefully that this is the saturation region which we are talking about this one, this is the cut-off and this is your triode and this is the saturation. So if you bias your device somewhere here right, somewhere here with this to be as V_{in} and this is to be V_{out}, right this is your V_{in} right.

Then I will be able to achieve a gain which is given as A_V was equals to, if you remember correctly in your previous turn to be equals to minus R_D times μ_n C oxide W by L into V_{IQ} minus V_{TH}. V_{IQ} is nothing but the input at this point Q, right and this is therefore the nothing but the overdrive, V overdrive, right.

So A_V voltage gain is therefore proportional to R_D and also onto the overdrive V overdrive. So higher the overdrive more will be the gain and of course higher the R_D you will also get the gain, but you see you have minus sign here negative sign which tells me that a MOS device,

when you have a source grounded condition will always have the output 180 degree phase shifted right, phase shifted as compared to input, right.

So you will always have a 180 degree phase shift and therefore it will always be negative in nature. So if you have input something like this, right then the output will be the output if you want to find the output, the output will be something like this that it will be like this, it will go like this and then like this and this, so it is 180 phase shifted. This is the V_{out} right, and this the V_{in}, right and if you want to find out the gain it is basically V_{out} by V_{in} at any particular point.

So it is 180 degree phase shifted. Now let us come back to our original discussion and see how does this works in the triode region, right so what we will be doing is we will be now discussing what is happening in the triode region. So let me erase some part of it and just give you an idea about the basic functionality here that if you did have a triode region, we saw the gain in a saturation region is independent of the applied input voltage, it only depends on the value of R_D and it does not depend upon anything else, it depends upon the overdrive voltage as well.

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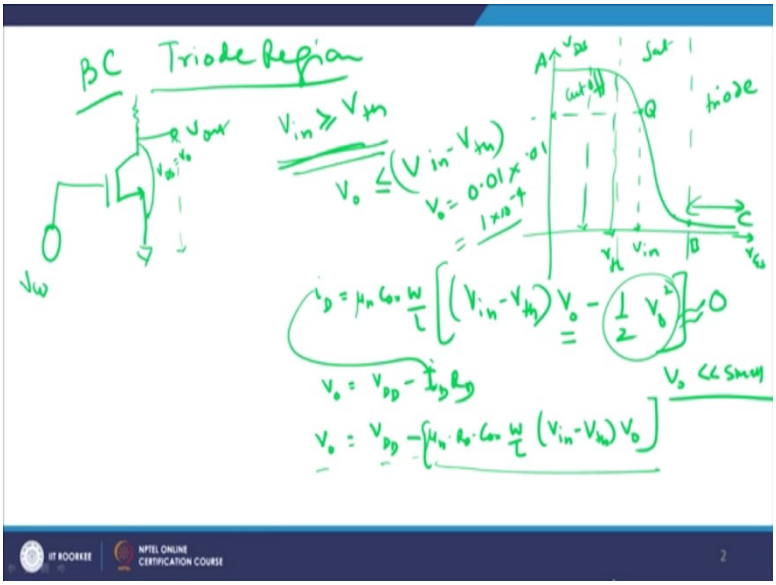

So with this discussion let me come to the region, let us suppose this is point B and this is C, this is A, right. Let me discuss about the point region BC which is this point, right. This is actually your triode region of operation, triode region. In the triode region if you see very carefully then input voltage is obviously larger than threshold voltage because already threshold voltage is somewhere here or somewhere here is the threshold voltage V_{TH}.

So your input voltage is obviously larger than threshold voltage but what has happened is that your V_{out} has actually fallen below V_{in} minus V_{TH} that is quite critical. That, your V_{out} has fallen below, so your idea was that V_{DS} should be greater equals to V_{GS} minus V_{TH} for saturation, but once your V_{out} falls below V_{in} minus V_{TH}, right then you are in a fix that now the condition for saturation will not be applicable.

Now the device will start behaving like a resistive network or resistive device and therefore I can write down in this case I_D to be equals to μ_n C oxide W by L, right and then we right down V_{in} minus V_{TH} into V_o, I will tell you why, into half V_o square. Why? Because if you remember the previous discussion which we were doing MOS device was something like this and you did have R_D here and this was your V_{GS} and this was grounded and you are taking the V_{out} from here. So if you take V_{out} from this to ground, it is exactly the same as drain to source because source is grounded. So therefore V_{DS} is equals to V_{out} and that is the reason we change from V_{DS} to V_0, right and V_0 is the V_{out} which you see from here.

Where V_0 is exactly equals to V_{DD} minus I_D R_D. So what I do, I just put the value of V_0 equals to V_{DD} minus I_D I just plug it from here and place it here and we write down to be equals to μ_n into R_D into C oxide into W by L into V_{in} minus V_{TH} into V_0 assuming that my V_0 is very very small.

So if V_0 is very very small, V_0 square will be negligibly small and this can be approximated to be equals to 0. For example V_0 is say 0.01 or so whatever then if you multiply it 0.01, I get 1 into 10 to the power minus 4 and so it is very very small as compared to this quantities here and therefore you can safely say that V_0 equals to V_{DD} minus this whole quantity into V_0.

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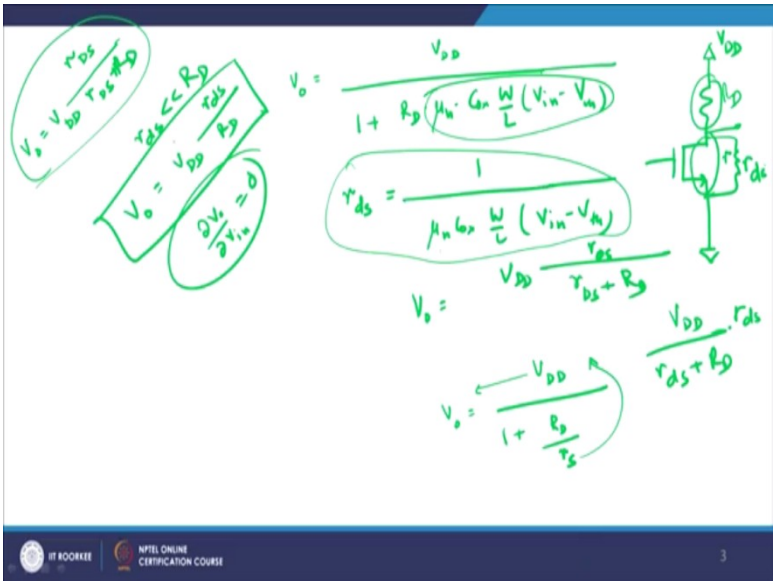

So we can write down therefore with this explanation, we can write down V_0 to be equals to V_{DD}, V_{DD} divided by 1 plus R_D times μ_n times C oxide into W by L into V_{in} minus V_{TH} and you get this. The effect was R_{DS} as the drain to source resistance as 1 by μ_n C oxide W by L V_{in} - V_{TH} and therefore I can write down V_0 to be equals to V_{DD} into R_{DS} into R_{DS} plus V_{DS} R_D.

How did I do that? See, simple if you look very carefully here if you take R_{DS} to be equal to this quantity because R_{DS} is 1 by this quantity, R_{DS} is the drain to source resistance of the MOS device in the on condition.

So once this is true if you place R_{DS} here, so this quantity can be written as 1 by R_{DS} remember, so I can write down V_0 to be equals to V_{DD} upon 1 plus R_D by R_S. So if you take LCM and do also some manipulation, V_{DD} comes outside, this denominator will come in the numerator and I will get R_S into so on and so forth. Finally, I get this thing:

So I will get V_0 equals to V_{DD} into R_{DS} upon R_{DS} plus R_D, R_D is the resistance on the drain side and if you look very carefully how it should like also, because when we were discussing just know if you look here carefully then this is V_{DD} and this V_{DD} is being broken into two parts as a voltage divider network and these two parts will be inversely proportional to the resistance offered by this as well as this. This is R_{DS}, so this is basically your R_{DS} and therefore R_D and since they are in series to each other, so the total current flowing through circuit will be nothing but V_{DD} by R_{DS} plus R_D.

This you multiply with R_{DS} to get the voltage at this particular point and that is what you are getting, V_{out} is equals to R_{DS} upon R_D plus, R_{DS} plus R_D. Typically what you get is that R_{DS} is

very very small as compared to capital R_D and therefore we write down V_0 to be equals to V_{DD} divided or R_{DS} right by R_D. This is your output voltage which depends upon V_{DD} into R_{DS}.

Now as you can see very carefully or interestingly that V_0 here is actually independent of V_{in}. So if you want to find out $\partial V_0 \partial V_{in}$, this will be actually equal to 0 because you do not get, you do not have any V_{in} on the right hand side but it depends upon the value of V_{DD}, R_{DS} and R_D, clear?

So as a result, I want to stress one important point here that in the triode region your gain will be fixed, will be almost 0 not only that your output voltage will also fixed and will not depend upon the input voltage and that is the reason as I explained to you. You will always get a constant value of the output voltage independent of the input voltage. This is one thing which I wanted to propose at this stage. So looking at the voltage transfer characteristics, I can only therefore safely say that I can only safely say that whenever my gate to drain whenever...

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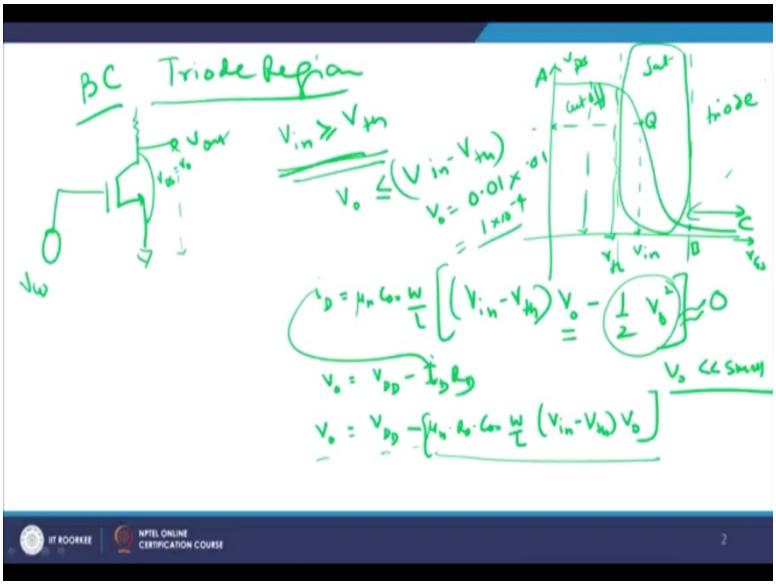

So if I want to bias the device as an amplifier it is always advisable to keep the device in the saturated region. This is the one take-away which you should do from this discussion. You place it here or here you are in a problem, you place it in a saturation region which is this, this region. You automatically get a very high gain which is available with you and this gain is typically very high, right, of the order of few 10 to the, even 10^2, 10^3 voltage by voltage by doing certain manipulation of course, and you can do it. Okay, with this let me explain it to you what do I get from here.

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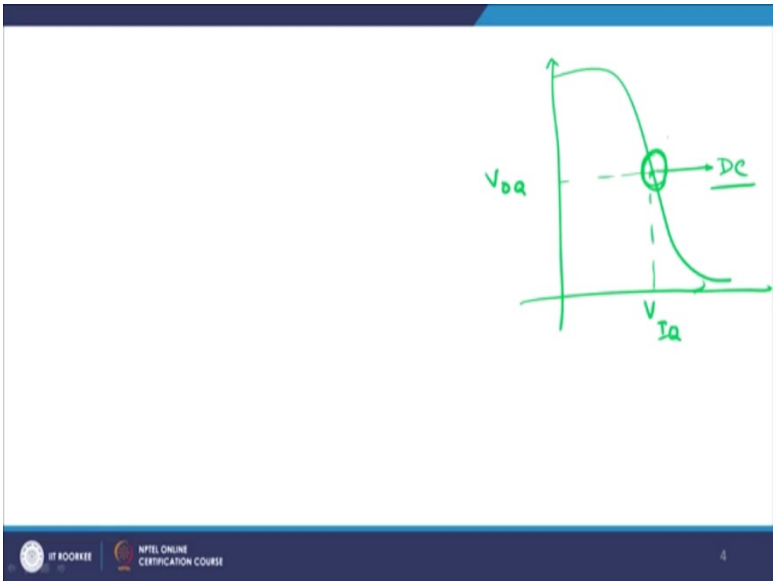

Now what I want to tell you is that since we have understood where to bias the device, say you have biased the device somewhere as expected, you have biased the device somewhere here. So almost in the middle of the region and this your V_{IQ} and this your V_{OQ}, so output Q input Q. So which means that you have to bias it by an external DC source, right so that initially even without an input signal it is placed somewhere in this region. Please be very careful, this is very very important that you need to first of all bias your device to sit in the saturation region before application of any input signal. That is what I was trying to tell you.

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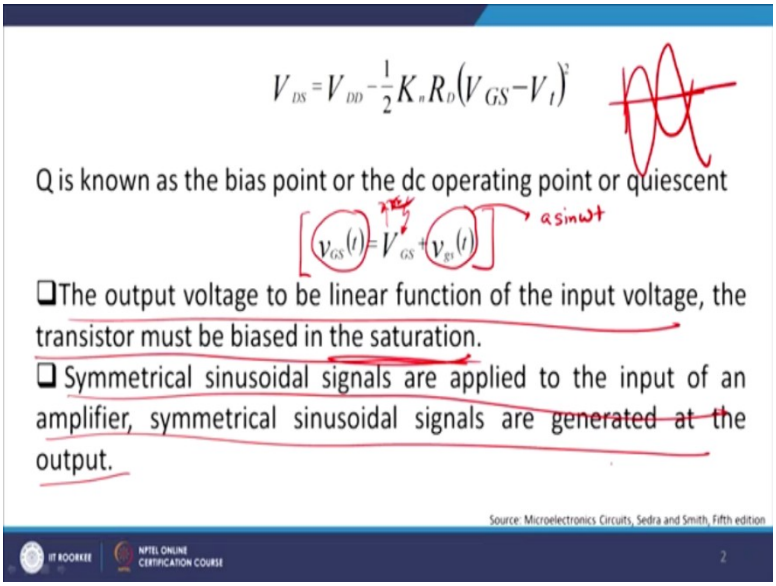

And therefore if you look very carefully this expression here, that my overall gate to source voltage which is a function of time will be the DC biased which you put V_{GS}, this is the DC

operating point and the input voltage. So this is my time varying input voltage, maybe an Asinw, sort of input voltage and you do have V_{GS} which is basically the DC bias which is fixed bias which is available.

Then you add simply to that and then you get this. So this basically a small signal output. Now the output voltage to be a linear function of the input voltage the transistor must be biased in saturation, this is the one single point which you should be very careful. Now what you do is that you apply a symmetrical sinusoidal signal to the input of an amplifier and we get a symmetrical sinusoidal output in the output side.

So you apply maybe a sine wave like this and you automatically get in the output side an amplified side wave in something like this, 180 degree phase shifted, fine. So this is one important point which you should be very carefully take care of in all due respects as far as this device is concerned, right.

Now let us see, as I discussed with you in our earlier discussion that the load line plays a very important role, why? Because the load line tells you those points within the IV characteristics of the BJT or the MOSFET where you should bias your device for proper application of amplification, right. So you should be very careful of the load line analysis or load line as such.

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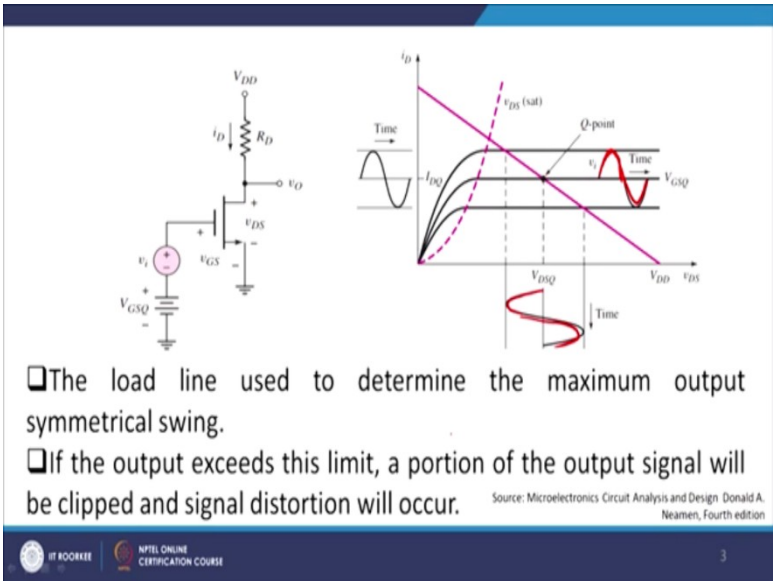

As I discussed with you this is the Q point, so this is your input and input goes from like this. And your output goes something like this in the time domain and you can get sorry, this is the input which you get and this is the output which you get from the this thing.

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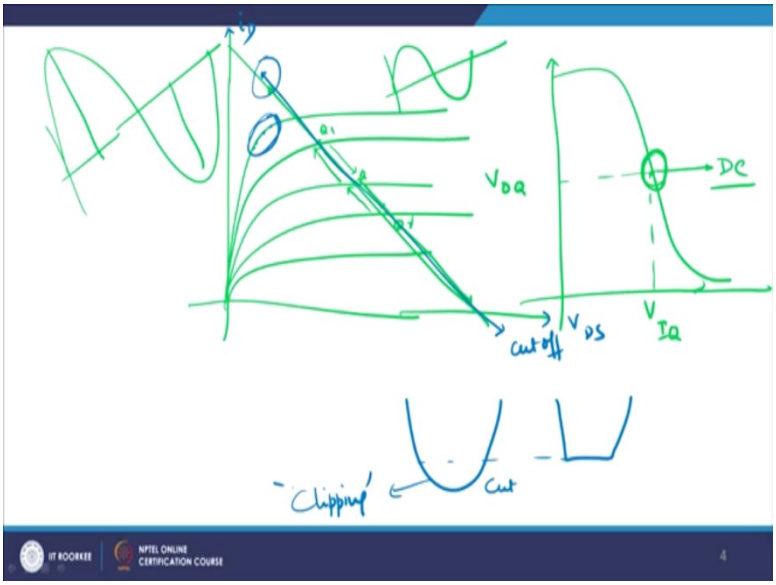

Now the idea here is that let us suppose I was discussing with you earlier point, let us suppose you had biased the device, this is my IV characteristics of my BJT, right. This is my IV characteristics, you had put the load line something like this and you biased it here, right. Once you biased it here, well, it is pretty simple then you apply an input signal, this Q point goes to this, suppose there are large number of curves here as well.

It goes to this point, so this your Q this your Q1 and this your Q2, right. So it goes to from here from here it goes to let me say it goes to Q1, right. Then from Q1 it goes to Q again and the Q to Q2 and then again Q2 to Q. So one single transition of input wave cycle will make my Q point traverse 1, 2, 3, 4, agreed? But if this signal itself is a very large signal which is this much big peak to peak right, then rather than going to Q1 it might actually go to this place or even go to this place, fine, are you getting my point? And therefore it is quite interesting or important to add that your input signal should be as small as possible or really small in nature, otherwise you force the Q point to go to the in this case into the triode region and this case if you go down into the cut-off region, in cut-off.

Which means that once you go to triode or cut-off, triode will ensure that your gain is a nonlinear amplification is there which means gain becomes a function of your voltage, please remember you can see that. See, this is current and this is I_D versus V_G V_{DS}.

If you see here, the resistance is varying if the resistance is varying obviously your gain will vary and as result if you force your device to be triode region you end up having a nonlinear amplification. Whereas if you force the device to go into cut-off, your output voltage will be

clipped, so your output should have gone something like this but what happens is that because of cut-off this goes like this.

You have cut-off here, this is cut-off. So this is also known as clipping, so you have clipping taking place. So you need to ensure that your device biasing is very proper, right and that is what is the next topic which I want to come to?

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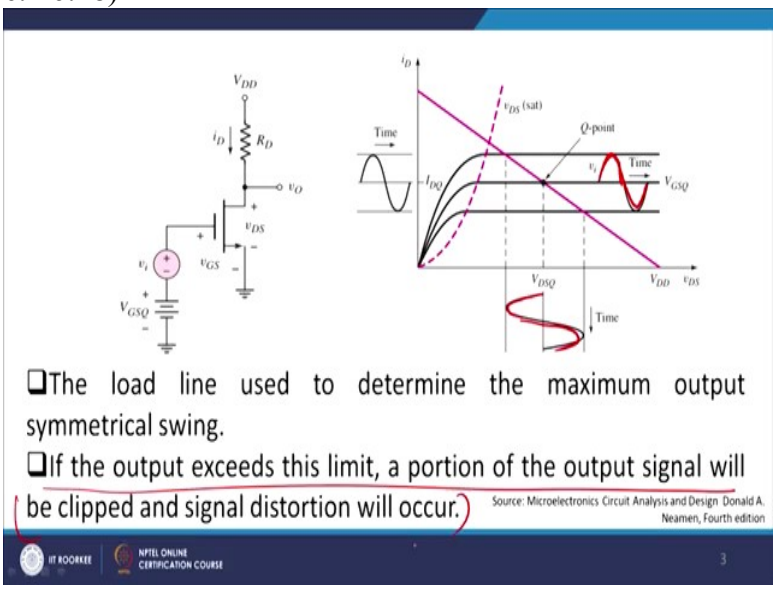

And therefore I was saying that if the input, output exceeds this limit a portion of the output signal will be clipped and the signal distortion will take place. Now this explanation of this idea which I was discussing with you, let me explain to you the various biasing techniques which are available to us as far as MOS device is concerned.

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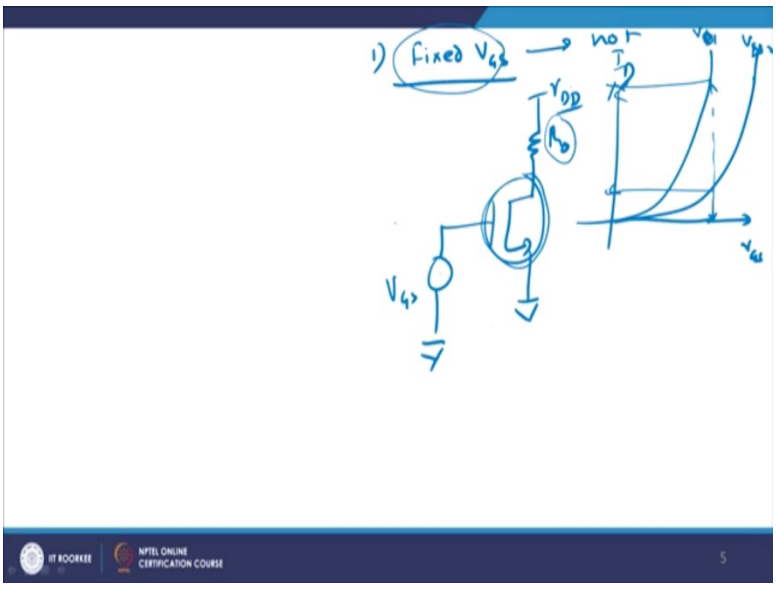

The first biasing technique which people used to follow much earlier, obviously not a very good biasing technique is what is known as a fixed, first is the fixed V_{GS} technique or a fixed gate to source voltage. It is not very of course, not good which means that in fixed V_{GS} what you do that you have got a drain source voltage, you do like this and then you fix up a gate voltage here and you fix up V_{GS} and I was discussing.

So this is basically a grounded source application with R_D here and V_{DD} here, this you have been learning it till now. But this way but the way it has been done is that you fix the value of V_{GS} in saturation region but the problem is that if you suppose replace this BJT by other BJT, if you replace this R_D or V_{DD} then chances are that the Q point will shift, so what might happen is something like this. So you have one device, so if you plot I_D versus V_{GS} let us suppose and then if you plot it then this will be this and maybe this.

So this is for $V_{GS\ 1}$ let us suppose and this for V_{GS}, $V_{DS\ 1}$ and V_{DS2}. So even if your drain to source voltage varies for the same values of V_{GS}, two devices may be so different from each other that the current obtained will be so large, so different from each other. It might also happen that for one calculation you have done properly for other one when you fix at the MOS device it forces it go in saturation region or in the nonlinear region. So fixed V_{GS} technique is not a very good technique and has been often like we do not assume it to be a very good technique.

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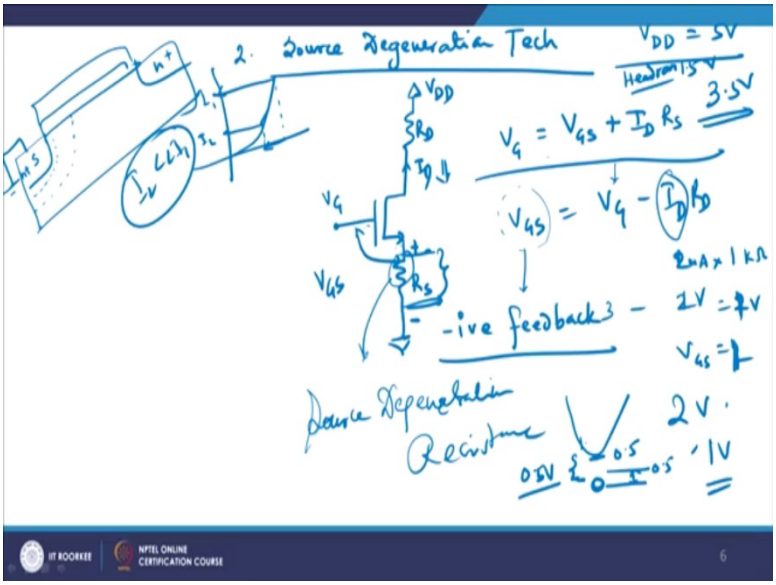

The second one which people follow is defined as source degeneration technique. This is source degeneration technique of biasing, so what I am trying do, I am trying to bias it from an external source using a DC bias, I am doing it on external source and trying to find out. Let me draw for you how it is different.

It is exactly the same as the first case, the only thing is that here we are adding an extra source resistance in series to your R_D and V_{DD}. So I have a V_{GS} of course available here. If you write it, so this is the value of V_G, so if you write it V_G, this will be nothing but V_{GS} plus I_D times R_S, this is the value of V_{GS} here. This is V_{GS} and this is V_{GS} plus I_D is the current which is flowing here, so I_D into R_S is the voltage drop across these two points. You add this voltage drop with this V_{GS} and you get the total gate current.

So the total gate current is therefore made up of V_G minus V_{GS}, therefore since V_{GS} is almost fixed I can safely write down that V_{GS} will be equal to V_G minus $I_D R_D$. Now what happens is that say if you assume that my V_{GS} has to vary for a fixed value of V_{GS} even if I_D varies even if I_D varies because of some reason or other then my V_{GS} will also vary in the opposite direction in order to compensate for the variation.

I will just show you how it works out. Say I_D was say 1 milliamp, so 1 milliamp multiplied by R_D say 1 kilo ohms, so if you multiply these two I get 1 volt, say V_G was equals to 3 volt, so 3 minus 1 is 2 volts, so V_{GS} was equals to 2 volts, right.

Now, let us suppose this becomes 2 milliamp, so 2 into 1 is 2 and I get this to be as 1 millivolt and therefore V_{GS} from 2 volts it becomes 1 volt. V_{GS} becomes 1 volt. Which means

that with increase in current, the gate to source voltage reduces and therefore it helps you to reduce the current. So, this is basically a negative feedback control, I will explain it to you just now, how?

Say current is flowing, so this is basically at higher potential as compared to this, of course. As a result this will reverse bias my source gate junction or the source, so it is something like this, on the source side it is source side and this is N^+ let us suppose and this is N^+ drain side, I have a gate here and then I have a metal function here and then I have got something like this.

Now what I do, on the source side, I apply a positive bias now, so what happens? The depletion thickness will be much larger here, if we did not apply any bias, it will be something like this. If you now apply the bias which is basically R_D into, I_D into R_S, the depletion thickness will become more stronger and therefore your current will drop down. So what happened? You increase the current right and decrease in V_{GS} force the current to go down, so something like this. If you plot I_D plus V_{DS}, your current increased, so what happens was your V_{GS} was large you get a large I_D. You force the V_{GS} to go low and it forces the current to go low here and therefore the current becomes something like this.

So you had I1, I2, I2 is much smaller as compared to I1 and automatically you get a much more stabilized system. This resistance is known as a source degeneration resistance. This is known as source degeneration resistance. Higher the value, better the control is, right. Let us also understand the cost you pay for it, the cost you pay for it is that as the voltage drops here, and this voltage drop can never be recovered, right and therefore the overall, so you have a headroom and a legroom. Headroom is basically, say you are you have applied V_{DD} say 5 volts, right?

Now whatever you do, the output voltage cannot go beyond 5 volts, then otherwise you will be violating Kirchhoff's law and there will be clipping, right? Let us suppose the due to amplification the output voltage peak voltage goes to say 3.5 volts, then the headroom available to you is defined as 1.5 volt, this is known as headroom, fine.

Also we define the legroom, legroom is when you go to the bottom side, so if you have a current flowing through the device and your bottom should be actually grounded but you are going to a value say equals to (1 point) say, your maximum value you are going to say, the value you are going like this, this value is say 0.5, then the legroom available to you is 0.5 volts and you can play with it.

Now if you already have I_D into R_S drop with you then this rather than 0, this will look something like 0.5 already, so you have actually eaten away into the legroom of the device. So the price you pay for it is that you peak to peak swings are therefore restricted now for a source degeneration technique based biasing, right. So you will be very careful about this technique that though you gain something you also lose something. Two things before we move forward, okay.

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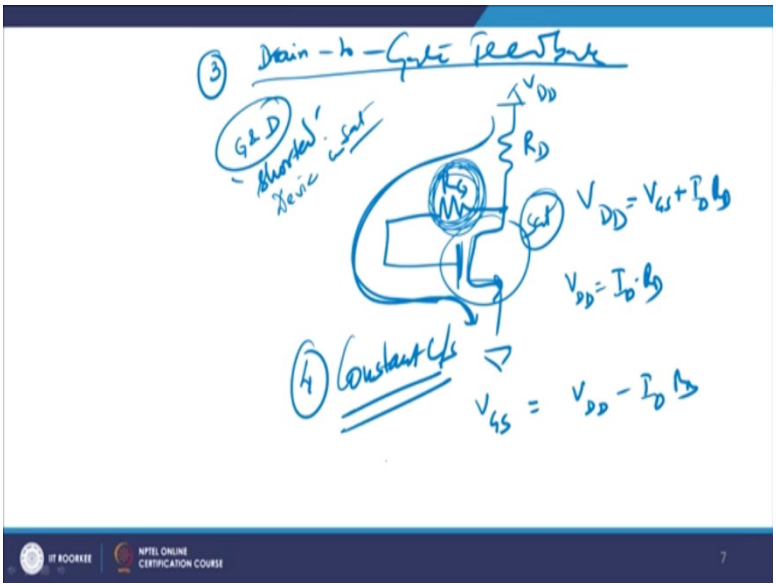

So let me go to third one, third technique for biasing is basically your drain to gate feedback technique, drain to gate feedback. It is basically drain to gate feedback. So let me draw for you how it looks like, it is something like this and you have a this, so R_D, R_G, this is V_{DD} and so on and so forth. So I get V_{DD} equals to V_{GS} plus I_D R_D of course. But if you go by this technique or from this path, I guess V_{DD} equals to I_D times R_D, is it okay? And you will also get I_G times R_G but I_G is very very small, you do not have any gate current available with you. So I get therefore, even if you follow this path the voltage drop across this will be negligibly small, right and you will get a more sort of idealistic situation.

I will get therefore V_{GS} to be equals to V_{DD} minus I_D R_D, what is the advantage of having a feedback loop here which connects the gate to the drain ends? That typically now your gate and drain are bond by this R_G. Since I_G equals to 0, the voltage drop across this thing will be negligibly small, so I could expect the gate voltage to be approximately equals to drain voltage and therefore this device will always be in saturation whatever be the input.

This is a quite interesting phenomena which takes place that since your gate and drain are shorted, then what happens is that you force the device to be in saturation for all values of

V_{GS}. And this is what you get. The fourth technique, I will not discuss it here is known as constant current source technique and it has been used quite often across the board but this is the constant current source technique.

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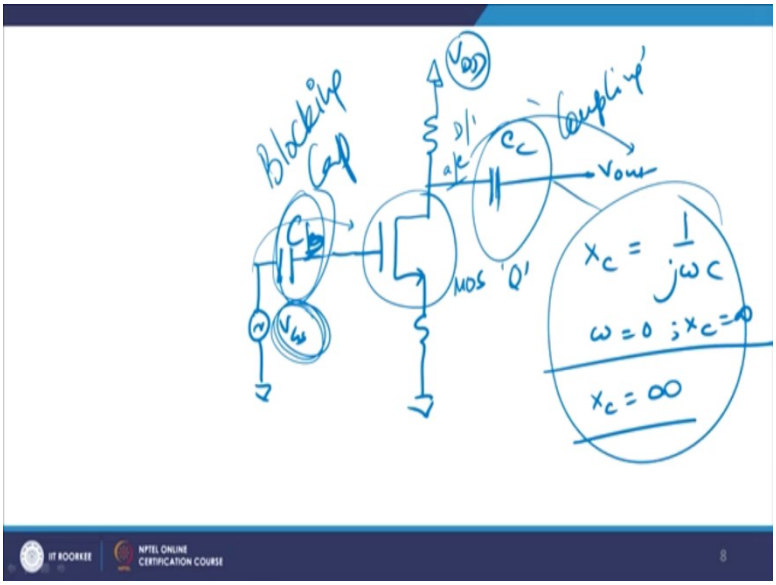

Please understand one more important point before we move forward is that whenever suppose we draw may be a source degeneration resistance based design, right, then if this is the gate voltage which you see, this is the output here, so we have a gate voltage we apply here that the input is given here and we have a gate voltage here V_{GS}, CC, CB we write down and then CC and this is V_{DD}. We have got two types of capacitors here, and these capacitors are also known as blocking capacitors CB, this is known as blocking cap or blocking capacitor and this one is known as a coupling capacitor, So, please understand that once we have this BJT biased at the saturation region, I do not want it to move away from the saturation region by external DC source.

Now any power supply in this case V_{GS} is a power supply, any V_{GS} which is power supply will always have some DC component superimposed on the AC component, it will not be pure AC which you will get. Now that DC component should not change the Q point of this MOS device. This MOS device Q point should not be changed by that DC input of this V_{GS}. So what people do, people put a capacitor here. Once you out a capacitor here remember the reactive impedance of the capacitor is 1 upon jwC.

So your w when it is 0 exceeds infinity and therefore for a DC bias which is omega equals to 0 the reactive impedance is 0 and the capacitive impendence is infinity sorry and therefore it does not allow any DC source to go here and it looks very good. Similarly, when you have a

coupling capacitor then I would like to see that all the AC signal which is available here should go to this next point and all this DC bias coming from V_{DD} should be stopped.

So you put a coupling capacitor, same principle you apply here as well and your V_{out} therefore will pure AC and there will be no DC bias available with you. So these are the blocking and coupling capacitors which we seldom use while DC while biasing of circuitry. So please be careful when we discuss the basing of the circuitry for all practical purposes.

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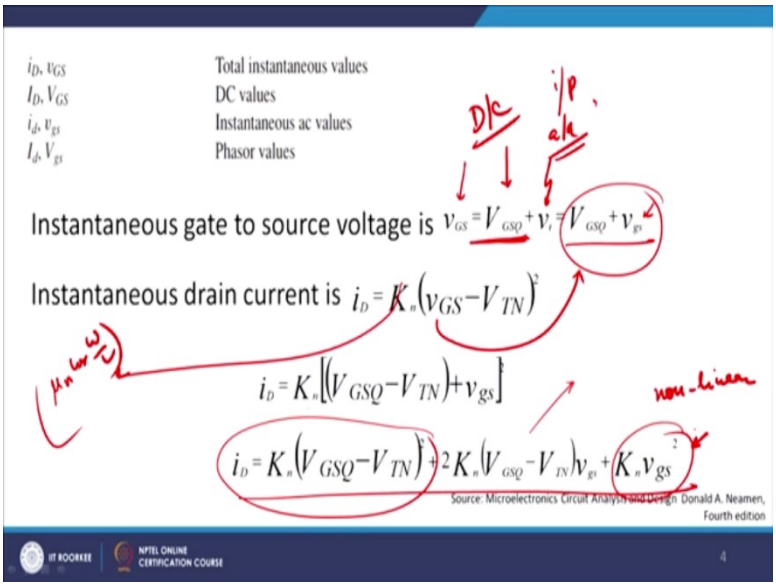

With this let me discuss with you that okay, so what happened was, so let me see therefore what happens, that now I have a V_{GS}, I have a V_{GSQ}, I have a DC bias which is somewhere in the middle. I have a DC bias here and DC bias I am overwriting the input voltage VI, this is my AC bias which I am giving and this is my total current or total voltage is sum of the DC voltage here plus the input AC.

So I get V_{GSQ} because it is at Q point plus V_{GS} gate to source voltage. So instantaneous drain current K_n is nothing but μ_n C oxide W by L. So this is the K_n value, this is K_n. So I_D equals to K_n V_{GS} minus threshold voltage whole square in the saturation region and therefore I_D is equal to K_n, in place of V_{GS} minus V_{TN} you just have to put this value now. So I get V_{GSQ} minus V_{TN} plus V_{GS} whole square, you got the point? Because just in place of this I place this and I get. Now if you expand it I get something like this, this is no problem because this is we have been talking about quite a lot time. So V_{GSQ} minus V_{TN} whole square the current in the saturation region, no problem. This is also a no problem because current is a linear function of V_{GS}. Where you have a problem is the last part where the current is parabolic function of V_{GS} which means that if V_{GS} increases by ∂V_{GS} amount that current will be parabolically

increasing. So there will be heavy nonlinearity provided you do not, you have this component of the current available with you and that makes the life difficult for overall picture.

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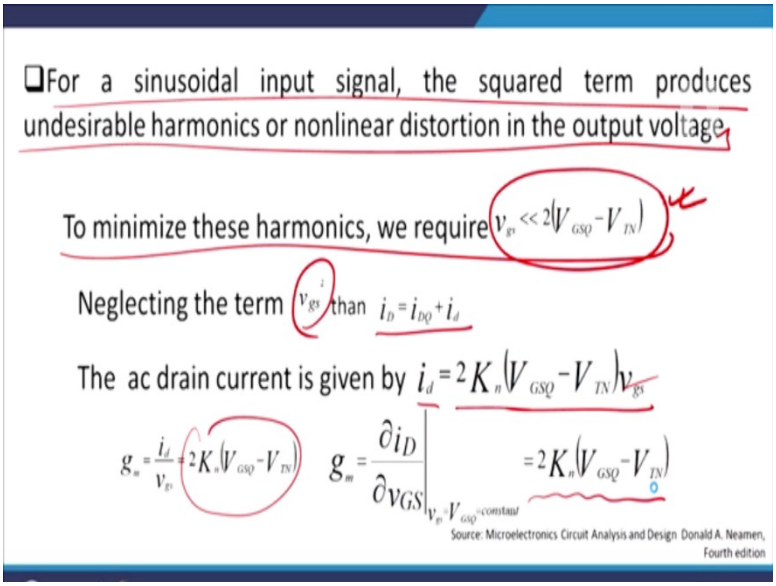

So for a sinusoidal, input signal what I am saying….for a sinusoidal signal input signal, the square term produces undesirable harmonics or nonlinear distortion in the output side. So to minimize this distortion we require that V_{GS} should be as small as possible, how small? Much smaller than 2 V_{GSQ} minus V_{TN}. So you are into deep triode region now. So therefore if you neglect therefore in such a scenario if you left at V_{GS} square I get I_D equals to I_{DQ} plus I_D. The AC drain current is given by this quantity we have already discussed this point and therefore I get G_M is defined as rate of change of drain current with gate voltage which is nothing but this, because if you differentiate with respect to gate voltage this vanishes off and you get this. So G_M we get two times K times V_{GSQ} minus V_{TN} and this is what the value of transconductance which you get. So this is what you get from the basic fundamental principle, so let me stop here because of the want of time. What we have understood today is given a MOS device where can I place the MOS device to obtain the most linear and the best saturation, first thing and the second thing is how to bias it using a DC source from an external world. From the next turn onwards we will look at the small signal model of MOS device and then we will look into the various modes of operation of MOS device, common source, common gate and common drain.

That will take care of our almost the analog part of the MOS device, amplification part at least, right? Thank you for your patient hearing. Thank you!!!