Microelectronics Devices to Circuits

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Module 05
Lecture 25

Biasing of Amplifier and its Behavior as an Analogue Switch-I

Hello everybody and welcome to NPTEL online course on Microelectronics: Devices to Circuits. Till now we have actually done more of devices in perspective which means we have learned, understood the concept of BJT, MOSFET, various operation modes of the MOSFET. We have also understood how a BJT works and how does a MOSFET works, what are the various domains of its working principle. We have also seen in our previous discussions, how fabrication can be done in terms of MOS devices which means that I do have MOS device with me, I need to fabricate it on silicon so what are the procedures one needs to follow.

Our last Module dealt with basically the principle of fabrication as well as packaging, so that we know that what is the final goal of the whole course. So finally we need to have a device which is basically integrable onto silicon and then can be packaged properly and delivered as an entity. With this previous about 4 to 4 and half weeks of lecture we were able to finish therefore the basic device concepts. Now let me come to the circuit aspect of it, and the next about 8 to 9 weeks or say 7 to 8 weeks we will be devoting much on Circuits and understanding the circuit aspect. To do that we will be starting with today's lecture and that is basically the biasing of MOS amplifier and its behaviour as an analog switch so that is the topic of today's lecture “Biasing of MOS amplifier and then behaviour as Analog switch.

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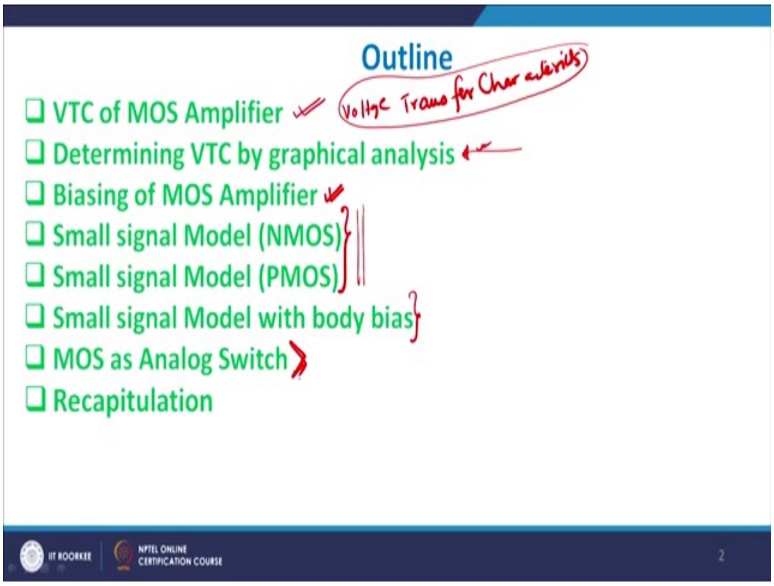

So what we will be doing in the first module of this course is we will be looking into the VTC of the MOS device, right. So I have a MOS amplifier, let me look at the basic simple MOSFET and then in a simple MOSFET let me draw for you the Voltage Transfer Characteristics, so VTC is basically your Voltage Transfer Characteristics. Using this we will be understanding certain things and certain areas of operation of the device. After this when we know VTC, we should actually graphically know can do the graphical analysis of this VTC right. So you have VTC available with you and you want to do a graphical analysis, then we actually how to go about doing it is basically my second point.

The third point is, we will learn about MOS amplifier how to bias it, now that is pretty interesting and important and the reason is if you remember very carefully that MOS can operate in triode region, in saturation region or in the cut-off region. In the triode region it works as a resistor, in the deep triode region it can work as a voltage variable resistor we have already discussed with you, in the saturation region it works as a current source and in Cut-off it is basically switched off. So whenever you want to use MOS device as a switch, you just have to shift it from saturation to the cut-off and vice versa, you just have to go from saturation to cut-off and Cut-off to saturation right that is known as switching right, so you know how to bias it.

But then if you want to use MOS device as an amplifier, you should know where the initial biasing of the device should be so that I get linear amplification with me, which means that the amplification A_V or voltage amplification voltage by voltage is not a function of the input voltage. So even if you are varying the input voltage drastically, my gain should remain constant and should be very high right. So you should know therefore how you bias your amplifier that is the reason this third one is important one right. We will be therefore looking at the small signal circuit models for NMOS and PMOS, obviously reasons asked is why will you require it?

Well, we require it because finally we have to use those MOS devices in a circuit environment and therefore if you are able to predict how does a circuit behaves or if you can predict how does a MOS device behaves, we can just take its equivalent model and place it in those places where MOSFETs have been there. This makes our calculation and understanding very easy from circuit perspective that is the reason we generally do small signal modelling here right. We again therefore look at small signal model with body biased and this I will come to this later on as we have discussed that body bias are important point and then we finally end our module by explaining how MOS works as an analog switch right, and we will see how it works as an analog Switch overall.

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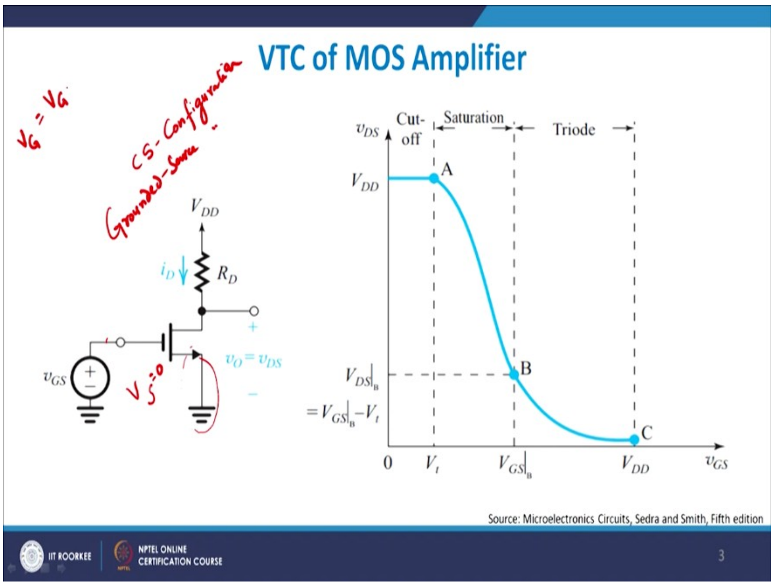

Now, I will just give you a brief insight into the voltage transfer characteristic of MOS amplifier. Now if you look very carefully, this is also known as common source configuration, if you look in front of you is basically a Common Source Configuration also known as Grounded Source Configuration right Grounded Source Configuration, and the reason being your source is basically grounded right. So source voltage is always held at equals to 0, so whatever gate voltage you give here is actually equals to gate to source voltage so your gate voltage V_G in this case is always equal to V_{GS} fine that this you should be very careful about this point. I again want to re-stress some important point which is you should be always careful to be handle about notation.

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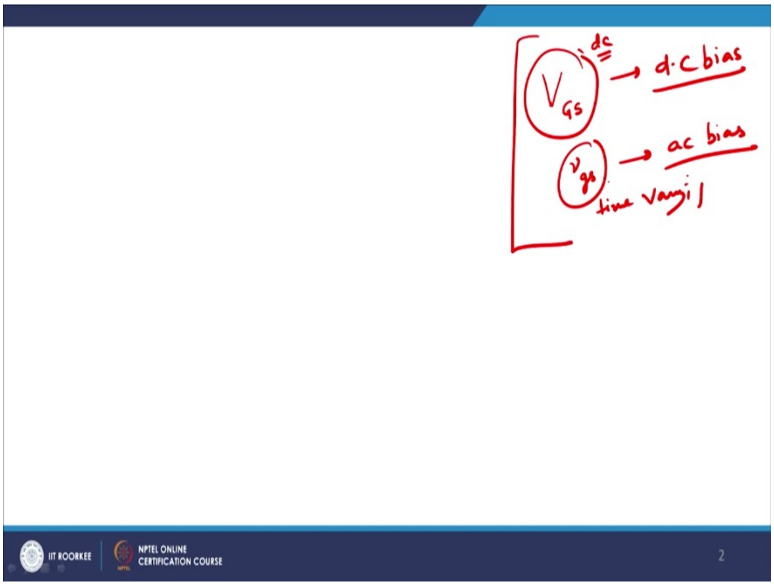

Notation is that if it is capital V_{GS} we have right, you can have small v gs right, so capital V_{GS} is basically the meaning of DC bias, DC biased primarily means that you have given a fixed value of gate voltage with respect to source voltage and it is basically a DC and therefore it is defined like this, v gs is basically your AC bias right or AC signal which means that it is a time varying signal so this is basically your time varying signal which you see time varying which you see. So you should be able to distinguish between capital V_{GS} and small v_{gs} and what does it stands for right at this stage.

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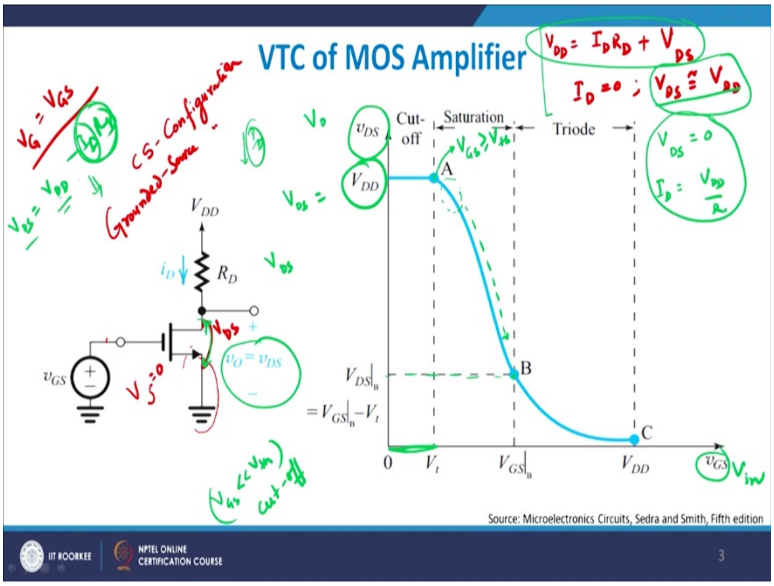

Now if you look carefully at this graph this profile, you will see I can simply write down for this case that V_{DD} equals to I_D R_D plus V_{DS} drain to source voltage right fine. Now which means that if your I_D is equal to 0, right, I_D is equal to 0, then V_{DS} is approximately equal to V_{DD} right. And when your I_D is not 0, I_D is typically a large value or V_{DS} is equal to 0 let me just tell you that you have V_{DS} is equal to 0 which means that so your V_{DS} is equal to 0 implies that your I_D will be equal to V_{DD} by R_D fine. If you therefore see very carefully that under the condition that you drain current is 0 and your device is cut-off, the output voltage will be dragged to V_{DS}. So as you can see here, V_O is equal to V_{DS}, right. And similarly, when your drain to source voltage is equal to $V_{DS,}$ your I_D is equal to 0 cut-off. And whenever my drain to source voltage is 0, I have a finite value of I_D flowing into it and that is what this with me.

Now understand that if I plot V_{DS} which is drain to source voltage versus V_{GS} right which is the input voltage, so this is my output voltage and this is my input voltage right. So I have an input voltage which is V_{GS} and output voltage which is V_{DS}. When my V_{GS} is below threshold voltage of the device, my device as I discussed earlier is in Cut-off mode right. Cut-off means this is cut-off so there is no current flowing through you, I_D is equal to 0 and as you can see V_{DS} is equal to V_{DD} see so this V_{DS} is equal to V_{DD} fine till a point you reach A, at A your MOS device turns ON, because your, at this point at node A, I get that V_{GS} is just greater than equal to V_{TH} threshold voltage of the device and as a result the device switches ON and the current starts to flow, I_D starts to flow.

I_D is initially low and then it increases, when it is initially low then if you can find out from this equation, from this equation if you find out V_{DS} therefore will be equal to V_{DD} - I_D R_D.

So even I_D is low, this quantity is small and therefore V_{DS} is almost close to V_{DS} which is this region. As I_D starts to increase, this quantity becomes larger and larger and therefore V_D minus that quantity starts to fall down and this is what is happening, your falling down, so the output voltage is falling down till you reach point B right. Point B is the point where you reach to a point where your V_{DS} drain to source voltage V_{out} has actually fallen so low that you have driven this almost into the edge of the triode region fine.

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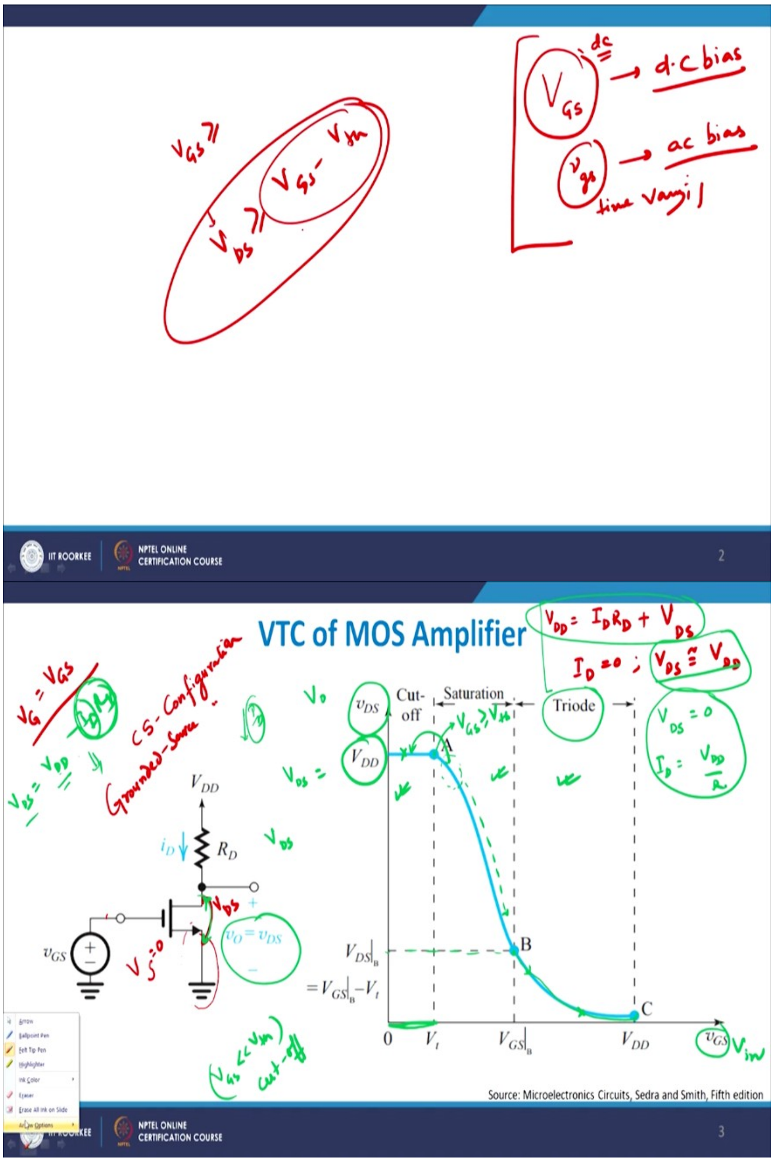

So you remember that if V $_{DS}$ was high right, you were into saturation if V $_{GS}$ was larger than, so the condition for saturation was that V $_{DS}$ should be great than or equal to V $_{GS}$ minus V $_{TH}$ this is one condition and that is the reason V $_{DS}$ should be quite large because this is quite large and therefore V $_{DS}$ should be quite large. So if V $_{DS}$ falls below a particularly limit which is happening here right and output voltage is falling below a particular limit you enter into triode region and that is the reason you see this is triode region.

And in the triode region, the current is the nonlinear function of the input voltage, and you see as the current increases the voltage further rises till you reach point C, and at point C the V $_{DS}$ is so small that there is no current flow and therefore your voltage transfer characteristic stops at this particular point. So we have therefore understood the VTC of MOS amplifier is divided into 3 parts; one is the cut-off, another is saturation, another is triode region right. So if you want to use it as a switch, you need to move from cut-off to saturation and from saturation to cut-off very fast, right.

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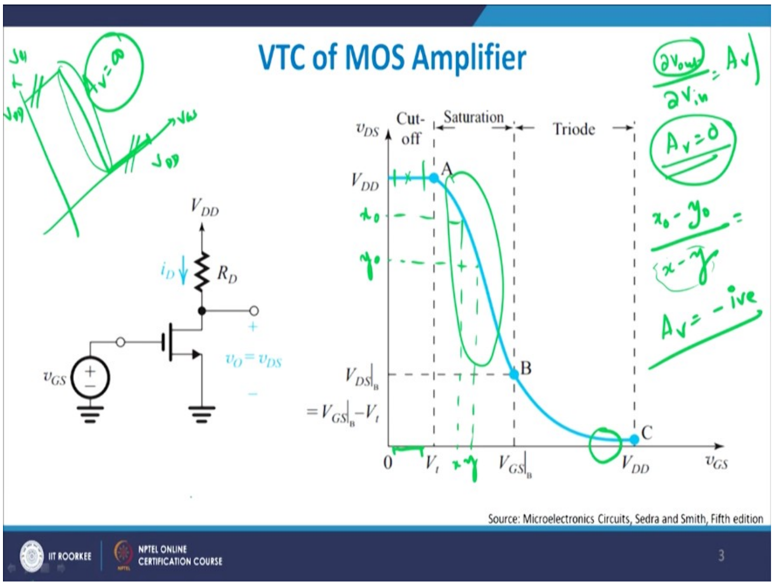

If you want to use it for example if you are biasing here or here which means at the cut-off triode region then you can safely see or you can actually see that if you are biasing somewhere here let us suppose right. And we try to find out output ∂V_{out} right and ∂V_{in} which is basically my voltage gain right peak to peak. Then you will see that even if I shift my input voltage by some amount, my output voltage still remains fixed which means that A_v is equal to 0 because ∂V_{out} is 0, which means that as you go on shifting your input voltage, your output voltage does not change and your voltage gain fix to 0, same thing will happen somewhere here where it is almost flat right.

So where the gain will be there? Gain will be there in the saturation region, where V_{out} is drastically varying even for a small change of V_{in}. So even if your V_{in} has changed from this point say to this point because of heavy nonlinearity, the output has actually changed from so if this is your input X and output Y, then this will be X_O Y_O and therefore we can define the gain to be equal to X_O minus Y_O divided by Y minus X or X minus Y. So it will be X minus Y actually but what we do is we write something like this, we write this to be as X minus Y so therefore this will be negative in dimensions because X is smaller than Y and therefore this gain A_v will be actually a negative quantity but will be a large quantity. So more steep is the slope, more will be the drain current, more will be the source.

So ideally VTC looks like this ideal, right, this is actually equals to V_{DD} here and this is also equal to V_{DD} here, this is V_{GS}, this is V_{DS}, right. And if you bias your device somewhere here I should ideally get A_v to be equals to infinity voltage gain to be equal to infinite. At this point the output latches to 1, at this point is latched to 0 so it is almost working as a digital switch, right, so by application of external bias I am able to switch it off from this side to this side. So with this let me therefore come to you how do I do it by graphical method.

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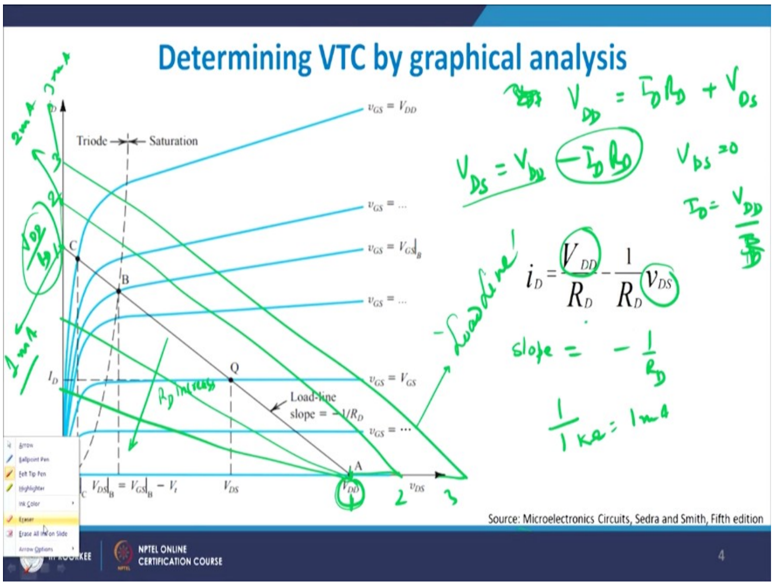

See as I was discussing with you that if you plot I_D versus V_{DS} right, I will get one point in I_D axis which is equal to V_{DS} so as I was discussing with you V_{DD} if you go back to the previous slide, V_{DD} equals to I_D R_D plus V_{DS}, right. So what I can write down safely is that V_{DS} equals to V_{DD} minus I_D R_D. Now when in this case, so if you look at the X axis, it is I_D which means that V_{DS} equals to 0. V_{DS} 0 means I_D will be equal to V_{DD} by I_D so this point is basically your V_{DD} sorry, R_D that will be this point. And what about this point? This is the point where your I_D is equal to 0. So when I_D is equal to 0, this quantity equals to 0 and therefore V_{DS} is equal to V_{DD} that is the reason this is V_{DD} fine. So I have a line which connects one point on the Y axis as V_{DD} by R_D to another point on Y axis which is basically equals to V_{DD} fine.

And therefore if you drop this line, the slope of this line is given so if you actually plot this line from this equation, I get I_D equal to V_{DD} by R_D minus 1 V_{DS} by R_D, V_{DD} is a DC bias and V_{DS} is the applied variable bias. So as you can see, the slope of this curve is equal to minus 1 by R_D so higher the value of R_D less is the slope available to you. So if you make R_D

large then what happens is that this quantity will drop down and this will not change, this will be V_{DD} and therefore if you increase your R_D it shifts to this, this is the increase in R_D, R_D increases right. Whereas, if you would have increased V_{DD} then this would have shifted to this point and this could have also shifted by the same amount to this point and therefore I will get a set of parallel lines when I increase V_{DD}.

So let us suppose your V_{DD} was say 1 volt here then 2 volts, 3 volts, so on and so forth and so this will be 1, this will be 2, this will be 3. And this divided by R_D will say your… so 1 volt divided by 1 kilo ohms will give you the value of 1 milliamp right, so this will be 1 milliamp, 1 milliamp, similarly this will be so this is 1, this is 2, 2 by 1 will be 2 milliamp and this will be 3 milliamp right and so on and so forth. So these are known as the Load lines so to understand this issue this is actually known as the Load line, right and the reason of the Load line is that they exactly follow the issue that inverse of that is basically the slope, in fact inverse of the load is basically the slope right and higher that value lower is the slope which is available with you.

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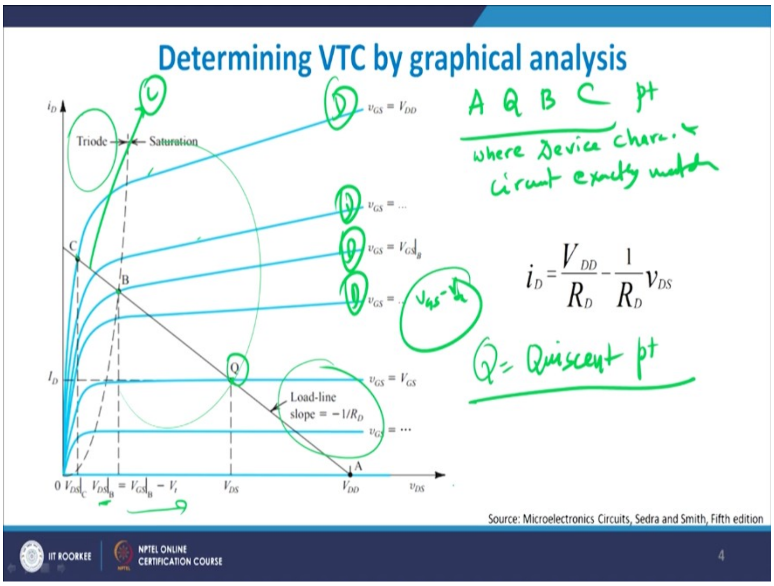

Now with this knowledge what we can therefore write down is we learned two things out of it, the first thing is basically that you do have always current which is flowing through the device, will depends upon many factors but primarily upon external circuit factors. The second idea was that always there will be a load line whose slope will be equal to minus 1 by R_D, and whenever it cuts your IV characteristics of the device which is this, this, this are the points AQBC so AQBC are the points where device characteristics right and circuit they exactly match, right why because this is the device but this is device, this is device, this is device, this is device whereas this is basically a circuit.

So when it cuts both of them are the points where both devices and circuits properly give you a match current available with you right and therefore these are effectively known as the points of operation of the device out of which we take one point which is also referred to as Q point quiescent point, Q point is known as quiescent QUISCENT primarily meaning that this point is very-very insensitive. So even if your voltage is varying slightly, the Q point will be varying but output will be very stable in output side right and this is where it cuts almost in the middle of the saturation region. So this is the saturation region right, and this is the middle of saturation region you will find the Q point, this is your triode region when your V_{DS} is very-very small alright so that is what we were discussing here that in the bulk side you will have a low value and as you increase it, so this is basically your V_{GS} which is equal to V_{GS} -V_{TH} also known as over drive right.

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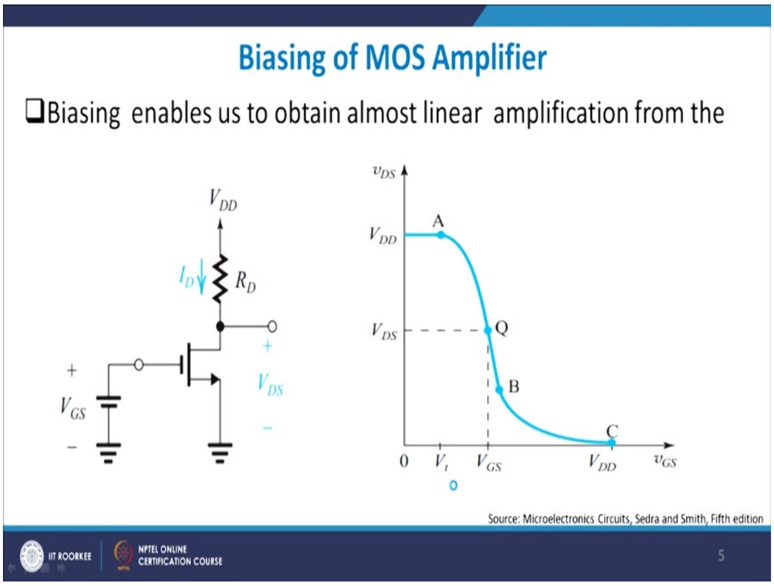

With this knowledge we come to important point that I always want a linear amplification primarily meaning that my gain should be almost independent of the input voltage and should be fixed for a given value of or a range of input voltage right. So you can see here from this basic operation principle that you have this region available with you so I have to V_{DS} and V_{GS} and threshold voltage V_{TH} and so on and so forth. Let me now explain to you that given a VTC right, how can we therefore draw the output characteristics of the device and what will be the fundamental characteristics of the device.

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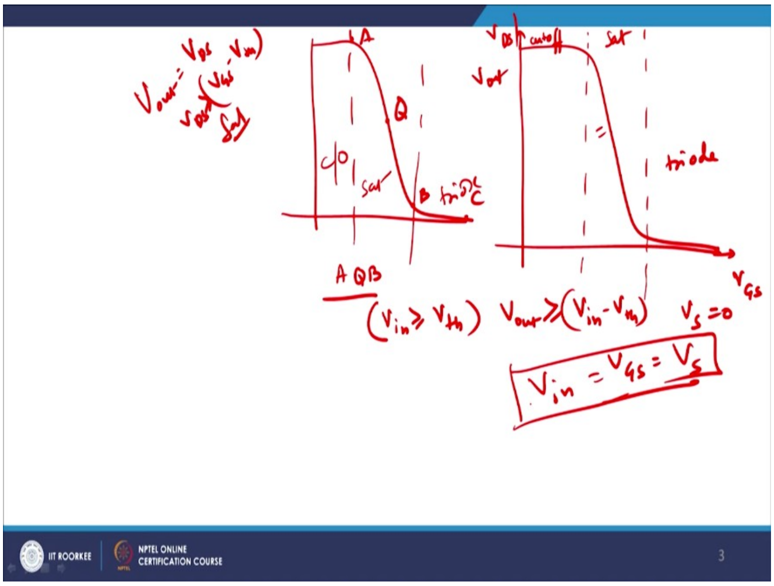

So let me just draw for you right and this is your point, right, this is your cut-off, this is your saturation and this is the triode region and this is V_{GS} and this is your V_{DS} also referred to as V_{out} fine. So let us at each point at each section of our voltage transfer characteristic let us see if we can evaluate the I_D -V_D characteristics right and then try to find out voltage gain available here. So with this knowledge let me first start with the saturation region of operation which is this one and let us see how current is formed there, current is formed in saturation region of operation right.

So what we do here is, we take up this case and then we draw a profile here right and we say that it is like A B and then how many like this, so we referred to this as point B, this is point C, this is point A and let us suppose this is point Q, this is the quiescent point right and we mark it as this and then this. Of course we discuss with you saturation, cut-off and this is your triode region. And the behaviour of current is totally different in all these 3 regions; in cut-off region current is 0, in triode region it is a strong function of V_{GS}, in saturation it is almost linear function of V_{GS}. Now, in this region, in region AQB let us suppose, I will get V_{in} input voltage should be greater than equal to threshold voltage of the device, we have already discussed this point and V_{out} is greater than equals to V_{in} - V_{TH}.

Remember why? Because V_{out} is equal to V_{DS} right and V_{DS} should be a greater than equal to V_{GS} - V_{TH} for saturation right and therefore I get V_{out} to be greater equals to V_{in} - V_{GS}. Now since V_S is equal to 0 right therefore, V_{GS} is equal to V_S and therefore this equal to V_{in}

input voltage which you see is almost equal to the source voltage in general, right. Now the second is the output, so output is given as V_{in} - V_{TH}.

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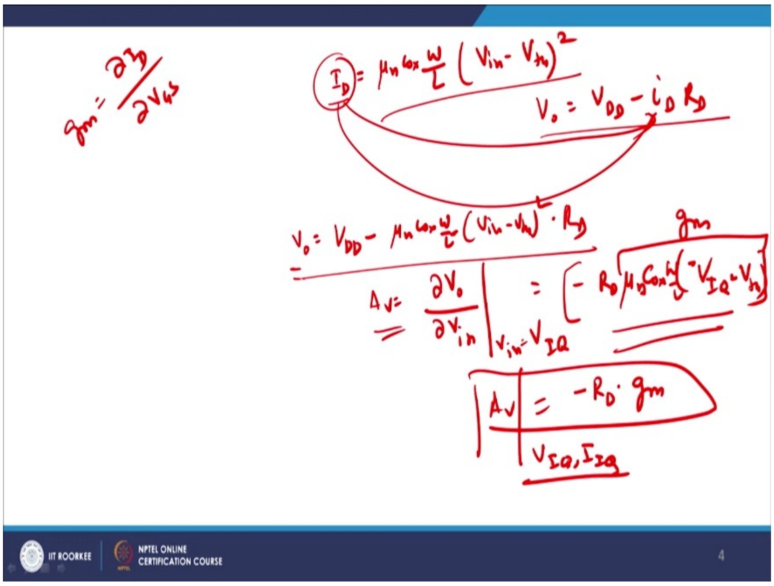

With this knowledge we can safely write down I_D which is the drain current will be equal to μ_n C oxide right, W by L into V_{in} minus V_{TH} whole square which therefore again means that so therefore V_O will be equal to V_{DD} minus I_D R_D and therefore if you place this value of I_D back into this equation and get V_0 equals to V_{DD} minus I_D is μ_n C oxide W by L right multiplied by V_{in} minus V_{TH} whole square into R_D right and this is what you get. Now if you therefore see this is your V_0 right so I need to find out therefore A_v as Del of V_0 to ∂of V_{in} right and V_{in} is equal to V IQ, this comes out to be minus R_D μ_n C oxide right W by L into V_{IQ} minus V_{TH}, this is the gain in the saturation region fine.

So let me again recapitulate what we did, I am assuming that device is fully into saturation right and there is no CLM and therefore I can write down I_D to be equal to μ_n C oxide W by L into V_{in} -V_{TH} whole square, and V_{out} will be equal to V_{DD} minus I_D R_D. We also saw that in saturation that V_{DS} or V_{out} should be greater than equals to V_{GS} minus V_{TH}. Therefore putting the value of I_D into this equation here I get this into consideration, then if you find the differential of V_{out} to V_{in} which is basically the voltage gain, I get this consideration and therefore I will just give you an idea that R_D into this is known as trance conductance gm this whole thing is known as gm also referred to as trance conductance of the device.

Tranceconductance primarily means g_m basically means ∂I_D and ∂V_{GS}, which means that how fast is your drain current changing with respect to similar change in the value of gate to source voltage right which means that how much your device is sensitive to input gate voltages right. If g_m is high transconductance of the device is high, I would expect to see a large change in the output current for the same change in the value of V_{GS}. Whereas when the transconductance is low, I will get a drain current which is actually smaller with same change in the value of V_{GS} right. So please understand therefore the gain as this point but one point to be noted at this stage is that gain at which point only at V_{IQ} or I_{IQ} which means that if you go back to your previous slide which means that.

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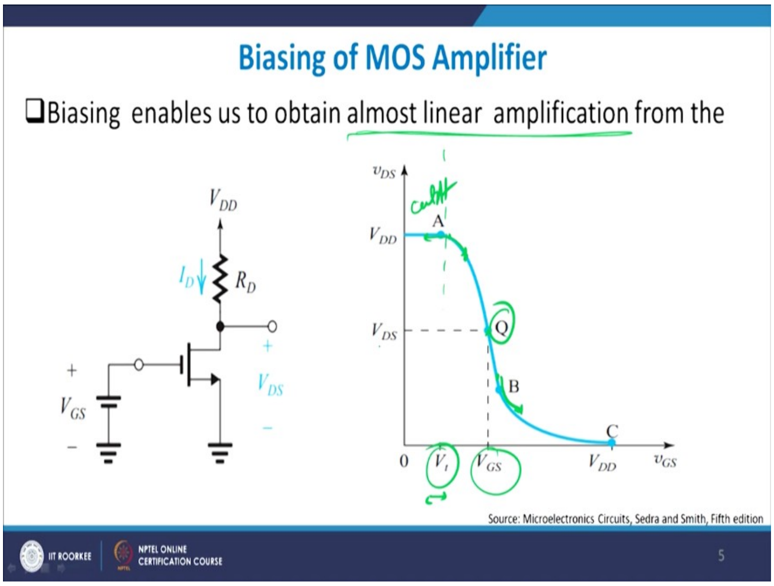

I have set my Q point to be Q. If you shift your Q point somewhere here or here very edge to the triode region or very edge to the saturation region right then even if there is a small change, so you see you have placed it here right. Now you do a small change in V_A then this will either shift back into A or it will come this side, if it will come this side you will have great nonlinearity as I discussed with you. And if it goes this side then it will go to cut off fine and both ways I do not want it and then similarly if I place it here and I allow it to subtract then most of it will go to triode region, so people thought that let us put a Q value that is somewhere in the middle of the two and help both of them right and that was the reason why this all sorts of variations came into picture here.

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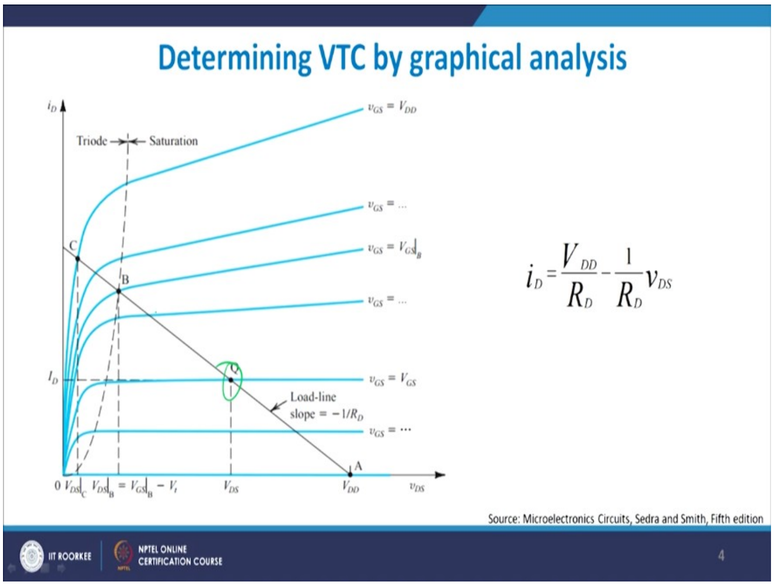

But I wanted to stress again here one important point is that just as you saw in the previous case, try to keep your Q point in the middle of the saturation region rather than in the edge here at the edge here that makes sense also. So we have understood the saturation region and we have understood the voltage gain

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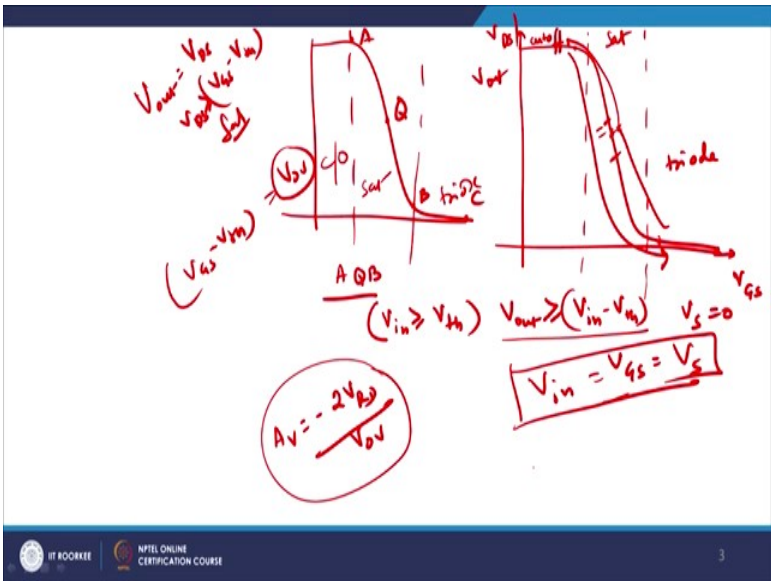

Another popular formula for voltage gain is basically given by this formula that A_v equals to minus times 2 V R_D divided by V overlap, V R_D is the voltage drop across the resistor R which is there on the drain side so V R_D, divided by V overlap is basically the voltage V_{GS} minus V_{TH} is basically the voltage overlap right and that is quite interesting phenomena which we get. So I am not deriving that part, you can do it yourself but that is typically what we are trying to do. With this idea understood and we have understood therefore in this lecture the basic concept of amplifier, how does an amplifier works, why do you want to bias the amplifier so that it works in a proper manner and does not give you a distortion. We also looked into the fact that given a MOS device and cut-off region, saturation region and triode region, exactly at which point should you bias your device so that I get the best available linear amplification available to me.

As I discussed with you, if you keep your Q point very close to either the cut-off region or the triode region, chances are that by application of input voltage the Q point may actually shift into cut-off or into saturation region or triode region, and as a result you will get non-linear output so it is always advisable to keep your input signal in a small signal mode and therefore the peak to peak input signal should be as small as possible then I will be able to maintain linearity into the system which I just showed you that which means if you bias it here and then if you move from this place to this place it is almost linear, but if you bias it here and then apply a very strong input voltage then it go somewhere here and then it again comes back here to here and so on and so forth right.

So if you see very carefully, you will find that these are the areas where you will have excessive nonlinearity coming into picture but there will be surely large gain available with you at this point and this point. We have also understood the basic functionality, what are the regions of operation for a MOS device. In our next class in our next module we will be actually following the triode region as well as the various biasing schemes in a MOSFET fine with this let me thank you for your patient hearing, thanks a lot!