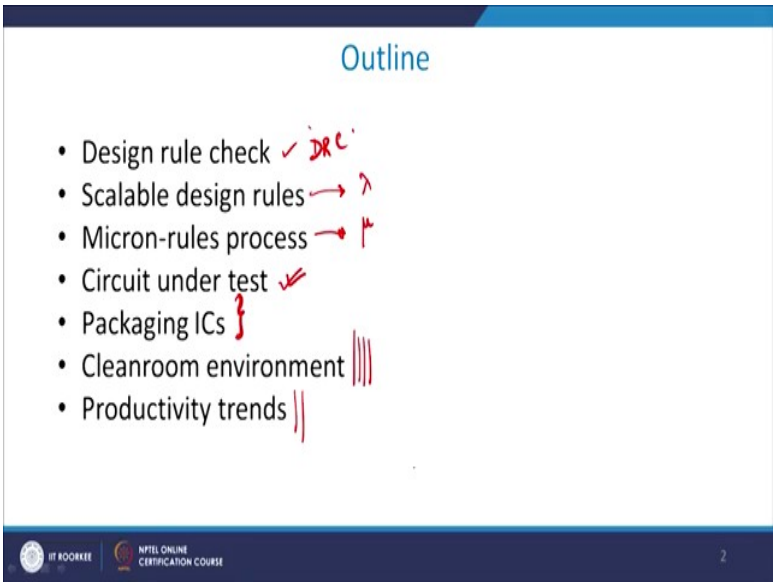
Microelectronics Devices to Circuits
Professor Sudeb Dasgupta
Department of Electronics and Communication Engineering
Indian Institute of Technology Roorkee
Module 05
Lecture 24
Fabrication Process - II

Hello everybody and welcome to the NPTEL online course on Microelectronic: Devices to Circuits and we take up fabrication processes part 2. So this is basically VLSI technology part which we are dealing with, so there will be two modules which we will be devoting to fabrication. Actually it requires a whole set of lectures to go in details of it but at least for a design course you should know the basic idea of fabrication and hence this lecture and the previous one.

(Refer Slide Time: 1:07)

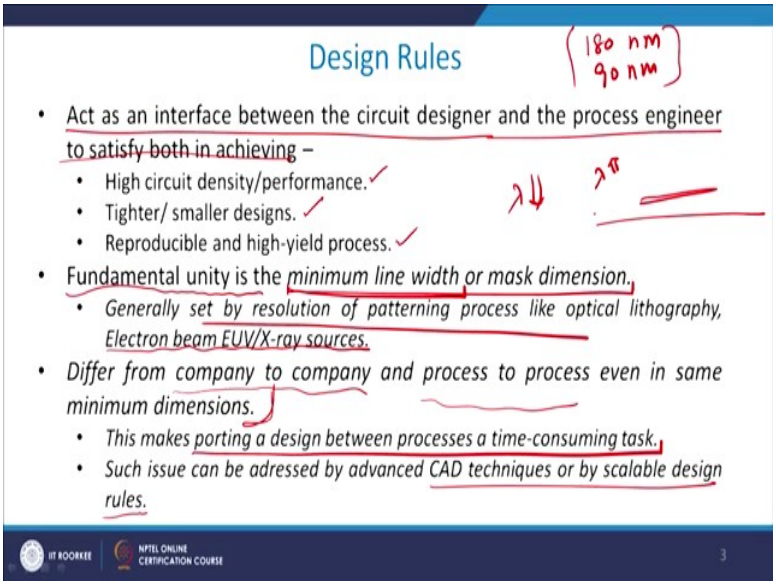


What we will be doing in this lecture series is the outline of the talk will be, so I will give you certain design rule checks, also known as DRC. So means that once your design has been done on a simulation platform, your layout has been done, you need to check whether this,, for example, whether the width of the contact which you have drawn is as per the requirement of the fabrication facility, right? So it might be true that the fabrication house can only make a contact which is say in a very layman's language 1 millimetre by 1 millimetre, and you have made a 2 millimetre by 2 millimetre so it will be rejected once your design actually goes to the Fab house. So the work is that you need to therefore do a checking of your design and therefore this is known as design rule check, so whatever design you have done on silicon using simulation platform tools, you need to do a thorough checking of that.

There are two types of rules such as Lambda-based design rules which is called Scalable design rules as you can see, right and we have a Micron-based design rules and this is the second design rule which we see, so this is basically **λ**, this is basically Micron right. And have been device from quite a long time but as the name suggests, Scalable design rules are design rules which are scalable in the sense that if you have a design which has higher dimensions right, say it is 4**λ** then you can scale it down to 2**λ** and everything will be scaled down by half in a sense so that is known as the scalable design rule. Whereas what is the micron-based design rule? Micron base design rule primarily means that the dimensions of the structure are actually fixed and given to you beforehand so you need to fix up those processes.

We will look into the fourth one which is basically circuit under test. We will look at some issues of packaging which itself is again a very big topic but I will be dealing in a detailed manner later on but at this stage we will touch and go for the packaging. We will have a look at typical cleanroom environment which is with us, and then finally we will look finally at productivity trends which is the current VLSI technology of fabrication gives me in a real sense so what is the design rule first of all let us see that.

(Refer Slide Time: 3:22)

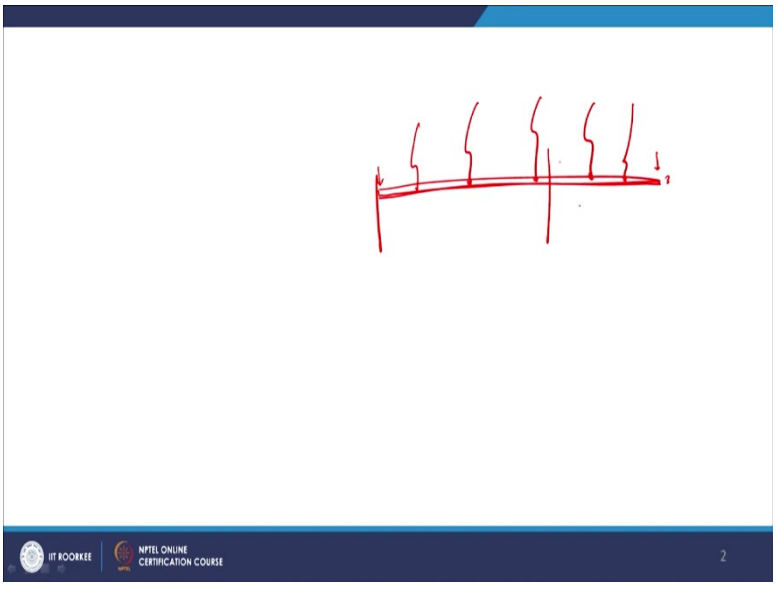


This acts as an interface between the circuit designer and the process engineer to satisfy both in achieving high density or performances, smaller design or smaller area and high yield processes. So as I was saying in the first slide that basically design rule checks are such that in is a common set of rules which a process engineer and circuit designer both have to follow,

so this is sort of a talking point between the circuit designer and the process engineer, right. And therefore if a circuit designer follows these rules very thoroughly then chances are that his design will be accepted by the process engineer and he will be able to send it for proper fabrication. If not, then he has to again iterate back to the circuit designer to change his design rules.

Why they are required? They are required because we require a very high performance which basically means that for example, I will give you, for example, if your contact is very large in dimension, you eat up into area but again if it is very small you then have larger resistance offered by the contact, so you need to optimize the contact area. And the process people have already optimised the contact area for you, say the metal contact should be same 0.5 micron by 0.5 micron, so they will let you know so then you design that much exactly onto your profile and you get the best results. Similarly, since we already optimise designs so the area of silicon utilised will be typically very small so there will be much tighter design that is the second point and the third point is since the circuit has been based on perfect design rules and they are satisfying the perfect design rules, the yield will be also very high because the production will be also very high, there will be less chances that the fab will fail in delivering the circuit.

(Refer Slide Time: 5:35)



Now the fundamental limit or the fundamental unity is the minimum line width or mask dimension, so this is basically very important. See, as I discussed with you in the previous slide that if you have for example mask and the mask has got something like this opening then you can ensure that means you can understand that this much amount of mask with this

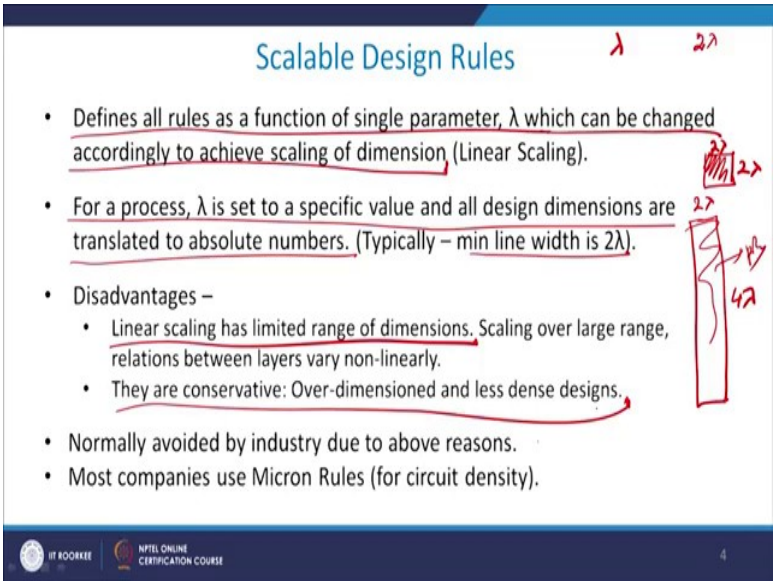
much amount of opening will be actually responsible for all the photolithographic raised to go through it and as a result you will have a dashing table typically available with you. So the line width which you see here, minimum line width which can be drawn and you can draw it safely with best results is basically the fundamental unit also referred to as minimum line width, so minimum line width is available dimensions. Who sets it? Of course it is set by the resolution of the patterning process.

Say for example, if you are using optical lithography where you are shining using an optical light typically an optical light you are doing it, then the **λ** values are typically large right. So if you are using **λ** large, you very well know that you will have heavy scattering right and therefore, if you wanted to grow let us suppose this much amount of Channel length, you might end up growing this much amount of channel length, right. So what you do, to make the design tighter you lower the **λ** value, and to lower the **λ** value you ensure that **λ** value is lower you have less scattering available to you, you go to E beam as well as X-ray sources.

Once you do that then you are not only able to reduce the dimensions which is an obvious advantage, but you will be also able to make the design much more stable because for example, when you have optical lithography there is chances of diffraction at the edges of the mask will be very high, so you wanted to grow 1 micron you end up growing 1.5 micron. Whereas, when you are using silicon or when you are using X-ray or direct E-beam that is very-very small, the diffraction are very-very small and therefore the exact length will be replicated on silicon, right. So therefore, it depends upon the type of source which you are using to a larger extent. Now this also differs from company to company and process to process, and with the same dimensions the process will change and it differs from company to company what type of process flow the company takes.

Now therefore that is what is important, porting a design between processes is a time-consuming task, which means that let us suppose today I have a process flow at 180 nanometre right, I want to port it at 90 nanometre right this is my job. This porting is quite difficult because it is not that you just reduce the dimensions by half and everything and everything will be fine, no it is quite complicated and therefore it is very difficult to port it from either lower to higher or higher to lower. So therefore there are certain CAD tools or CAD techniques which scale the design so we use scalable design rules, so I can either use CAD tool to do that or I use scalable design rule to take care of that this thing. Let me therefore come to what is scalable design rule.

(Refer Slide Time: 8:45)



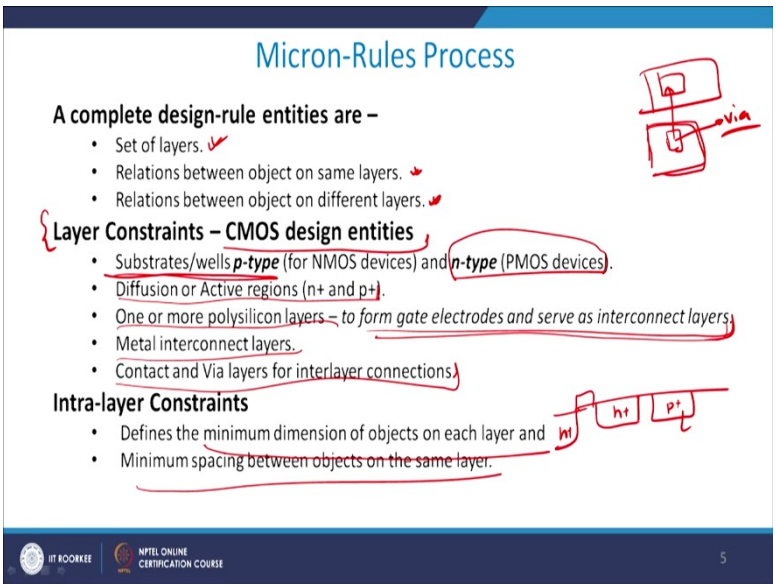
Now what is happening is that the scalable design rule is that defines all the rules as a function of single parameter **λ** and which can be changed according to achieving the scaling of the dimensions, so linear scaling which is here. Secondly for a process, **λ** is set to a specific value and all the design dimensions are translated to absolute numbers typically minimum line width is 2**λ**. So let us suppose I have a **λ** right process width **λ**, so we define minimum line length to be equal to 2**λ** there are certain reasons for that. Therefore, let us suppose I have a contact whose dimensions are 2**λ** by 2**λ**, so there is a minimum contact which you can get.

Similarly, you have a poly silicon which is basically say 2**λ** by 4 **λ**, this is poly this is poly let us suppose right so it will be always dimension of so it may be 2 **λ**, 3 **λ**, 4 **λ**, 5 **λ**, 6 **λ**, so that is the reason it is scalable. So once your **λ** is defined you just have to put the integer value to change it from the high to low value, so on and so forth. Now and therefore the advantage is of course that it is scalable and therefore you can use it but disadvantage is that it is not scalable over a large range of design or over a long large range right because you can see here the linear scaling has limited range in dimensions right and they are conservative in nature and therefore they are dimensioned and less dense design is available to you, which means that they tend to give you though they are scalable but has a limited range in dimensions and they also set a nonlinearity at higher values and therefore they are less dense design with us.

Now generally avoided by industry to a larger extent because of the above problems as most of the industries use micron rules for their purposes and they use micron quite conveniently

in this case. Micron rule is a set of layers as I discussed with you earlier, so **λ** based design rules are based on the fact that you have minimum length of **λ** and generally typical line widths of 2 **λ** right. And if you take 2 **λ** as a dimension and then you take either even or odd multiples of 2 **λ** and you automatically start getting the scale designs so you can have 2 **λ**, 3 **λ**, 4 **λ**, 5 **λ** as a scale design and so on and so forth.

(Refer Slide Time: 11:13)



In the micron-based design rule or the micron rules, a complete design rule entities are there are set of layers right, and relationship between object on the same layer and on different layers. So what we do is, in this case we have layers for example, if you have an interconnect layer which is a metal layer, then you have poly silicon layer then you have field oxide layer then you have silicon layer, so on and so forth. At each layer we start defining the distance between 2 active points or 2 passive points right, we can also define the distance between 2 layers across the particular board, right.

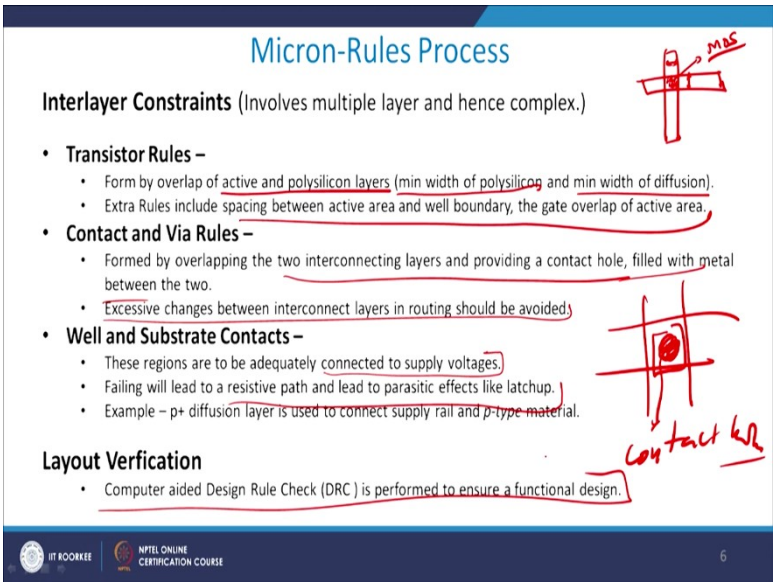
So what are the constraints the layer constraints? The layer constraints are you have CMOS, let us look at CMOS design styles. So substrates are p well or p-type right and is n-type, for PMOS device of course if you remember substrate has to be n-type and for NMOS device the substrate should be p-type right. Second layer is diffusion or active layer N^+ or P^+ by which you make actually the source and drain regions. One or more poly silicon layers to form the gate electrodes and serve as interconnect layer, and then this is for gate electrode whereas, this is for metal interconnect layer.

So interconnect basically means that so there are 2 layers of metal, one is the metal layer itself which connects the contact with the external world and you have an interconnect layer which contacts the external world with the peripheral devices. Now contact and via layers for interlayer connections, so I have a contact like this right and there is a via available here which starts to make contact with the upper layer right, makes a contact with the upper layer so this is known as via. So via is a sort of a through silicon metallisation right and that is known as via right.

Now so you already have an intra-layer constraint, now within the inter-layer constraints are, defines the minimum dimensions of objects on each layer, and the minimum spacing between the objects on the same layer. So what does it tell me is two things micron is what should be the minimum dimension for example, an N^+ diffusion layer or a P^+ diffusion layer, right that tells me that, and then secondly it also tells me what should be the minimum distance between N^+ layer and P^+ layer.

Suppose you are able to get pictures for example, you are designing a system which is something like this and you have an N^+ layer and you have a P^+ layer then what does it tell me is this is substrate and this is source drain and this is source and then you have something like this, so what do they tell me is what should be the minimum dimensions of this N^+ layer and what should be the minimum distance between these 2 layers which is this one right. If it is closer than this, the design will fail so two things gives you the intra-layer constraints in a certain sense. Now to continue with the micron process, for inter-layer constraints are obviously more complicated because between the two layers you need to talk.

(Refer Slide Time: 14:22)



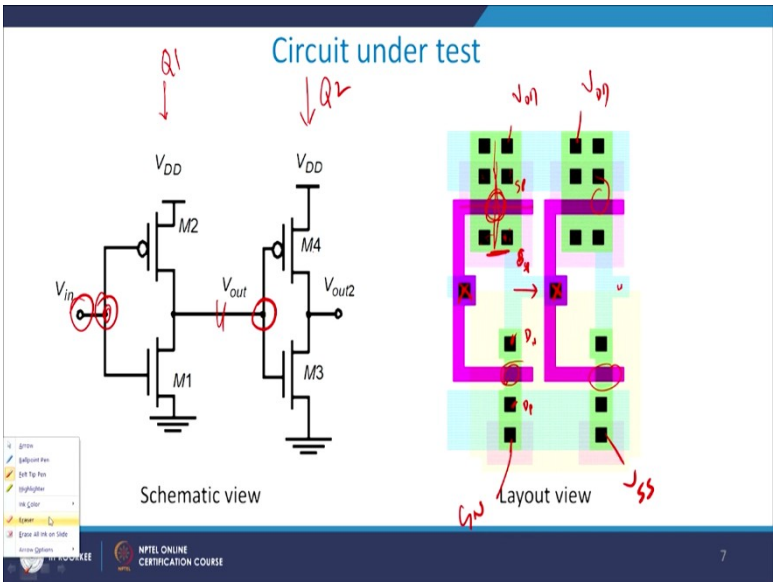
Now what are the transistor rules? The first rule is that when an active layer and a poly silicon layer cross each other we get a transistor that is a very simple basic rule number 1 right. And therefore the minimum width of poly silicon and the minimum width of diffusion is primarily, so if you have something like this as a poly and you have something like this as a diffusion then typically this is your active MOS device right transistor. What are the extra rules? Include the spacing between active area, well boundary and gate overlap of active area, so you need to set out what is this, what is this distance, how much should be this distance, so on and so forth.

Now contact and via rules, so we have understood transistor rules, transistor rules are those in which the active and poly silicon layer cross each other and dimensions are set by the crossing principle. Contact and via rules, well they are formed by overlapping of two interconnecting layers and provide a contact hole filled with metal between the two. So let us I have one layer here and another layer here, we have this empty here, here I fill up with metal right and therefore this we refer to as a contact hole, right. Excessive changes between interconnect layers in routing should be avoided, I think this is very interesting. So you might have, so I was discussing with you only two metal layers right, but you might have multiple metal layers looking into the fact that you might have multiple interconnect layers right. So you have 1 interconnect layer 2, 3, 4, the last one becomes your V_{DD} layer which is the final power supply layer.

Typically while designing we should not transverse between layers too much, within the layer we make a design and then we move to the next layer and we keep these micron-based design rules effectively okay with this. Now “Well and substrate contacts”, they should be adequately contact connected to the supply voltage as we have discussed already. Failing this will lead to resistive path and lead to parasitic effects such as latch up right. This is pretty important, you seldom found problem areas specially the micron-based design rules is that, if you do not connect the substrate and your wells, substrates and your n-well, p-well procedures either to the supply or to the ground and you keep it floating, chances are that there is a problem of latch up.

Latch-up basically means that maybe it latches to a particular state and stays there permanently which you do not want it to happen right, so that is one of the pretty drastic problem which happens due to latch up, so that is what I wanted to say for the well and substrate layer right. Generally your CAD tool for example is performing a functional design check using DRC. And you can use one of the standard Cadence for example is one of them which uses the typical layer , there is a DRC for you. If there is a problem, it gives you the problem at which point you have a problem in layout and then you can correct those again on the DRC. When this DRC clean then you freeze your design and send it to the fabricator.

(Refer Slide Time: 17:30)

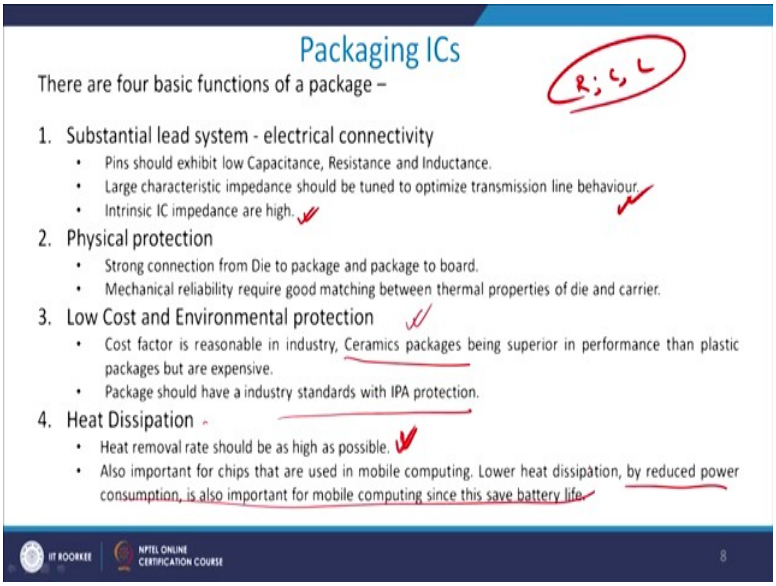


So look at the circuit under test, as you can see we have got two CMS inverters driving each other, so this first one is let us suppose Q1, next one is basically Q2. So Q1 is driving Q2 and therefore as you can see here very interestingly that you have a contact here right so this

contact is this one right. And when the poly and the metal layer, this metal layer and the poly layer cuts, this is basically your MOS device similarly this is your MOS device here, similarly this is your MOS device which is M4 and this is your MOS device M3. Since this is PMOS you will have metal layer twice the width because you do not want it to be skewed, you want the t_{PHL} to be t_{PLH} and therefore the width is almost double that of NMOS here that is we can see.

So this is your source drain and this is your V_{DD} and ground, so this is your V_{DD}, V_{DD} right and this is your GND and this is your V_{SS} or GND, and this is your this contact is this contact right and this contact is this contact or this contact in fact, and this is drain and source. So you have a drain here so this is drain of NMOS, this is drain of PMOS, this is again the source of PMOS and this is source of PMOS and these 2 are shorted and I get this, so these 2 are interconnect, similarly this is interconnect which is visible to you. So this is a typical circuit under test, typical layout which you will see here as you can see here right and these are the metal layers which you see, so metal layers are responsible for carrying the V_{DD} ok.

(Refer Slide Time: 19:20)



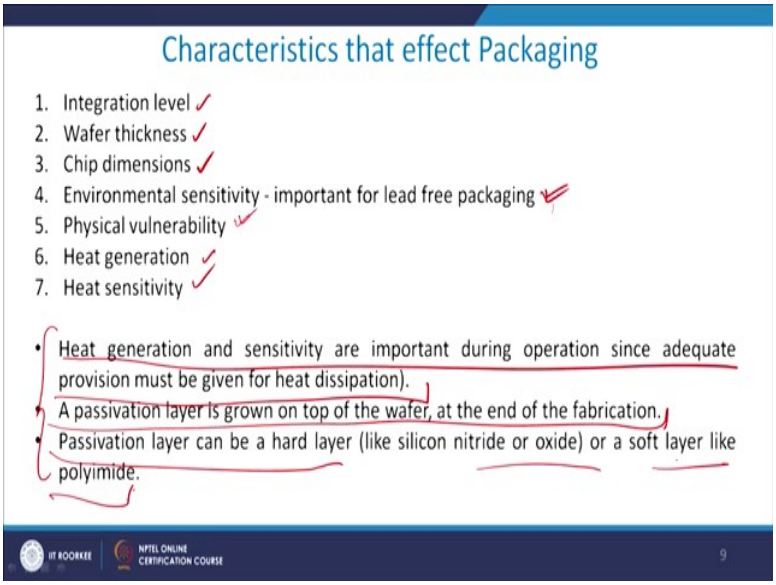
Let us look at the packaging of IC, well there are 4 basic functions of the package. Generally, you should have pins which will be IO pins means input output pins, they should exhibit low resistances, capacitances and inductances so that the delays are minimise across the pin. It should also have large characteristics impedance to reduce the noise at those particular pins which is the second part. And intrinsic IC impedance should be high which we have already discussed in the second part.

The second point is the physical protection, physical protection means strong connection between dye and package, and package and the board. So if you have those dye, even if you remove it physically you can remove it easily that should not be the case and it should be properly bound with the board. Now mechanical reliability require good matching between thermal properties of dye and the carrier right so that is very important that mechanical reliability is important for example, if there is shaking of the table or something like that, your dye should not be extracted right from the board itself.

It should be low-cost, the cost factor is pretty from industry point of view, ceramic packages are most superior in performance then plastic packages but then they are very expensive in nature. So whenever you go to the Fab and you tell them I want the ceramic package they will provide you a set of ceramic packages, if that matches with IO of your design input output map of your design, you can take that ceramic package and do it. So typically what people do over the years, if you want a package design you first look at the package and then you because if you want to do a package design then you first of all look at the package, look at the number of pins and IO pins and then decide how to change your design so that it fits to the package right.

At the last stage you cannot do it so therefore it is always advisable to look at the package first and have a look into it. And it should have industry standards as I discussed with you right with IPA protection. Typically, you should be protected from surges electrical surges and so on and so forth. What is heat dissipation? Heat removal should be as good as possible so you should have good heat sinks, but you can do it by reducing the power consumption and generally we use mobile computing for saving the power nowadays right and most of the time the packages help you to reduce the power drastically right.

(Refer Slide Time: 21:39)



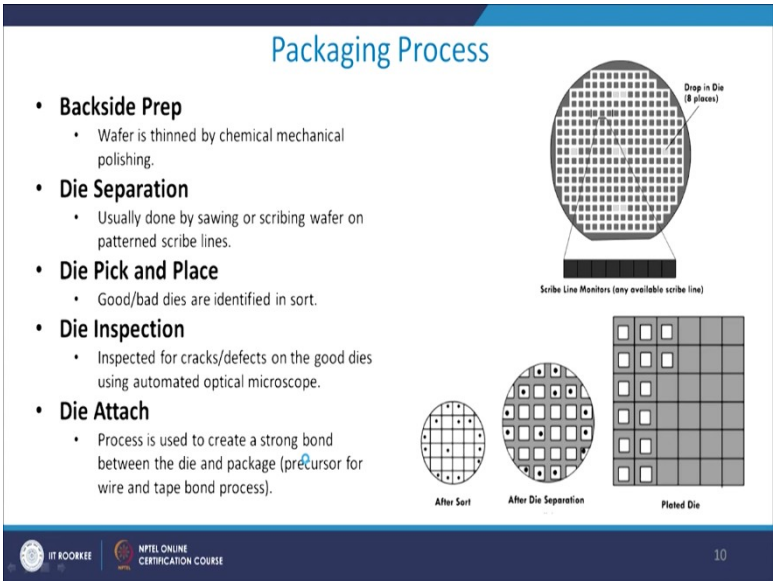
What are the characteristic that affect packaging? Well of course, what type of packaging you will be using it depends upon the type of integration level which you are using. Similarly, how much wafer thickness are you using, what are the dimensions of the chip which you are using right, and then you look into an environmental sensitivity for example, people generally do not like obviously for obvious reasons arsenic, lead as part of the packaging technique and therefore it is not a very good idea to have these materials as part of the package.

And then it is physical vulnerability because how much it is prone to mechanical instability as such. Heat sink and heat sensitivity are two important points, heat generation and heat sensitivity in the sense that even if the heat is generated for example, all mixed signal block generates very heavy heat and analog will generate very heavy heat but then we should ensure that it behaves as a very good heat sink and removes all the heat even before everything comes to the surface. Now therefore as I discussed with you that heat generation and sensitivity are important during operation since adequate provision must be provided for heat dissipation, right.

A passivation layer is grown on top of the wafer at the end of the fabrication, and we know the reason why because the passivation layer will be there, it will help you that the lower devices active devices are not in touch with the active environment and therefore we do not expect it to get back. Passivation layer can be a hard layer like silicon dioxide or a soft layer like polyimide right. And that is quite an interesting one which we needs to look into that

they have a soft layer like polyimide or even a hard layer passivation can be done right, so this is the effects of packaging which you see.

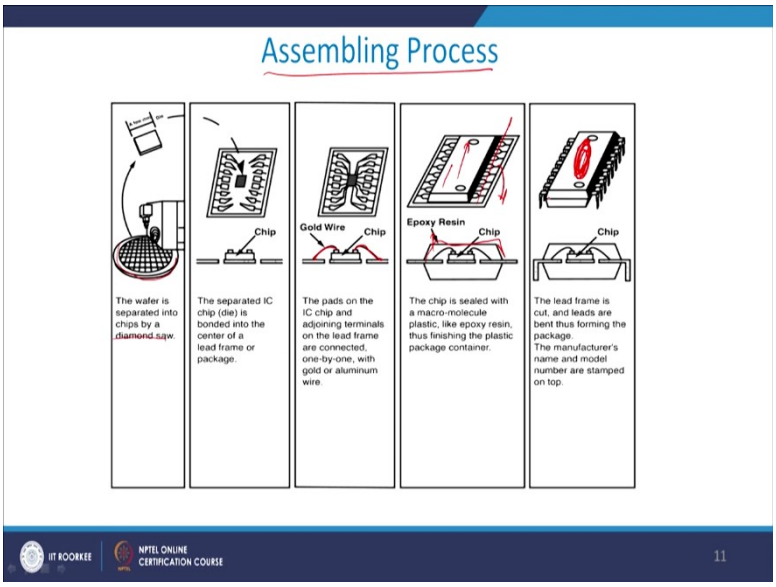
(Refer Slide Time: 23:23)



Packaging process if you look very carefully, we generally do wafer thinning by chemical CMP which is chemical or mechanical polishing. Generally these are known as dyes and these dyes are separated by diamond patterning, by diamond patterning you can actually remove these scribes, you can describe you can remove it, so these are actually known as Scribe line monitor as you can see this is the scribe line monitor. Over this you will have a dye on this side, you will have a dye on this side. Good dyes and bad dyes are sorted and they are identified and they are identified even when they are part of the silicon wafer itself.

You do dye inspection for physical cracks and defects, and generally we use automated optical microscope and that is enough to see whether a dye has cracked, or if it has not cracked then is there any physical discontinuity within the package itself, and if there are it is automatically removed from the system. You have to also have a good process to attach your dye with the package right, and therefore there are techniques of doing packaging and dying to a larger extent. And this is quite an interesting or important steps by which you can process these dyes ok.

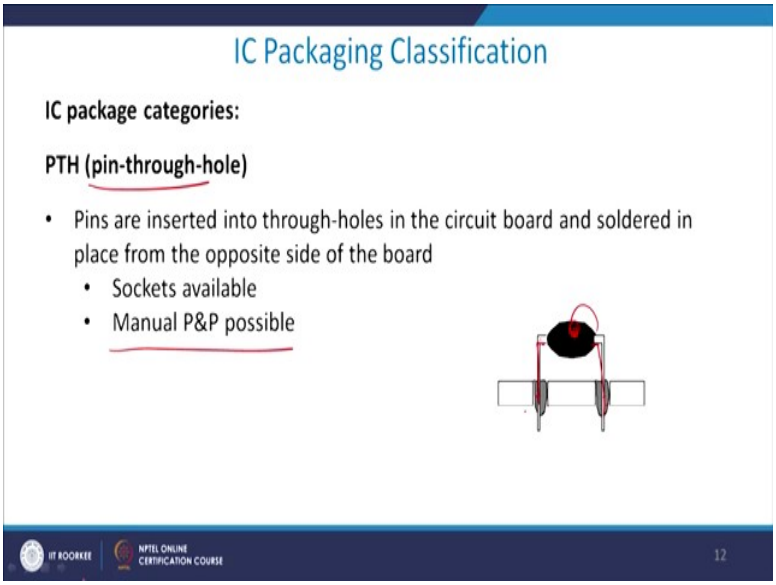
(Refer Slide Time: 24:47)



As I discussed with you, let me just give you a brief of assembling process. As I discussed with you the wafer, if you look at this is the wafer right. This wafer is separated using a diamond saw as I discussed, the separated IC chip which is this one is bonded into the centre of a lead frame or package. So I have a chip here and I place it here, these are your IO pins which you see in the pack, you do not able to see it but these are the IO pins. And these are the wires which connect the IO pins to the external world, IO pins and these are gold wires which connect to the external world. So the pads on the IC chip and the adjoining terminals are connected one by one with gold or aluminium wires, right.

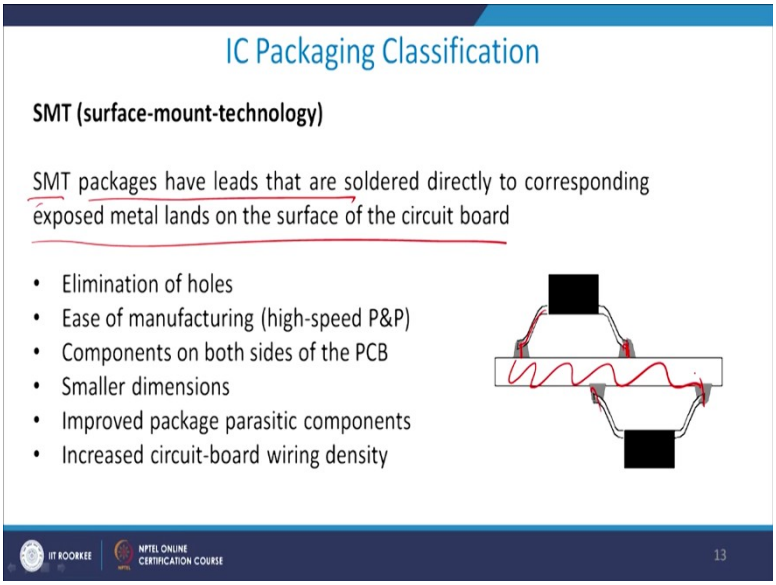
So after you have connected them, the chip is basically sealed, this is the proxy seal, is sealed with a micro-molecular plastic like epoxy resin and this is the plastic container which you can do it right. So this chip and this is the epoxy resin, so epoxy resin is over the whole chip so that it does not get disturbed right. The net frame is then cut and bent, so what you can do is you can cut it and then bend it around this direction and then we can put the name of the firm which has made this process and so on and so forth, what type of IC is this so on and so forth, its identification mark can be placed here in this case right.

(Refer Slide Time: 26:14)



IC packaging, well there are 2-3 important packaging techniques, the first is a pin-through-hole. Pins are inserted through holes as you can see here in the circuit board and soldered in the place in the opposite side of the board. So this is soldered from where? So this is through holes and then you soldered it here right, so manual PNP is possible manual pin through holes can be possible and you can actually solder it manually to a larger extent.

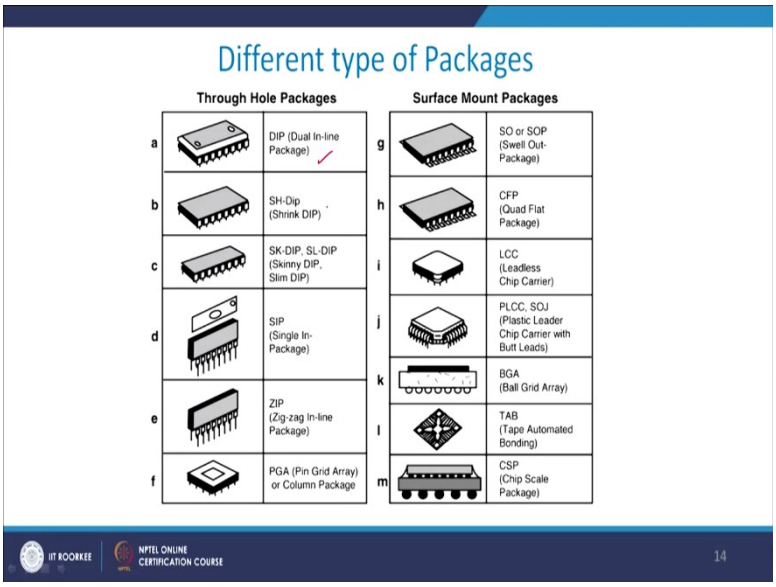
(Refer Slide Time: 26:44)



And then you have surface mount technology in which what you do is that so you do have SMT packages or surface mount technology packages that have leads right that has soldered to the surface of the exposed metal lands. So this is the circuit board, you just have to solder it here right you solder it here. So you do not have holes, elimination of holes is the first

advantage, it is easily manufactured and you can use both side of PCBs to do that, they have much smaller dimensions and therefore they have reduced parasitics and larger wiring density and therefore you do have a tighter control over the wire package right and that is what is the advantage of IC packaging in this case.

(Refer Slide Time: 27:28)

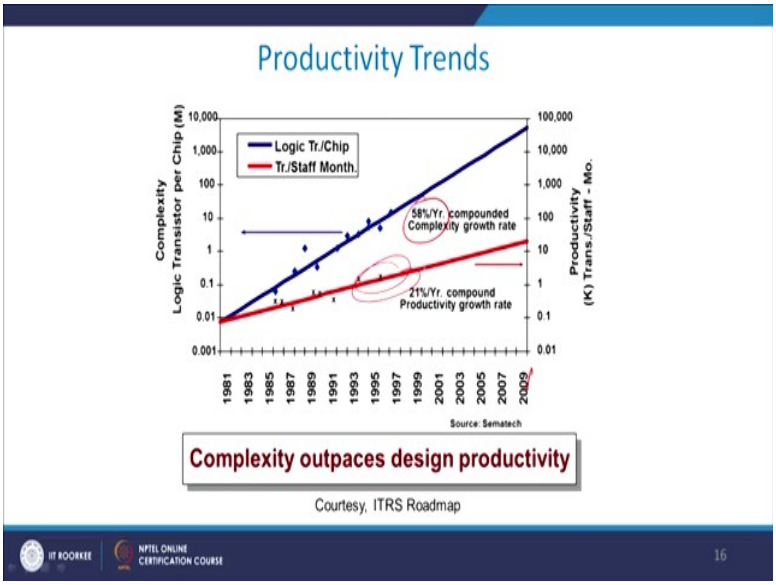


Different types of packages you can get it on various books. We have a DIP which is dual in line, we have shrink DIP, we do have SK-DIP these are all through hole packages right. So which means that you draw the whole through the system through the silicon and then you wire bound it here or you can do bonding here or you can do moulding here right and these are all types of packages available with you. So the left one is basically Through Whole Package and the right one is basically the Surface Mount Packages right. And so surface mount packages and through hole packages are available with you, but SMTs give you much much lower parasitics as compared to through hole and they are more reliable as compared to through holes right that is what you get from this idea.

(Refer Slide Time: 28:29)

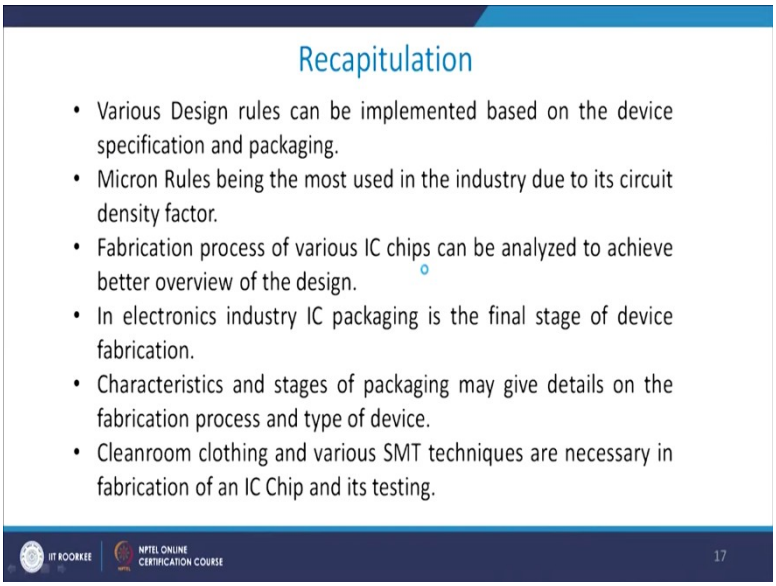
Let me give you a small maybe a figure or a photograph of the cleanroom. This is from TSMC which is basically Taiwan semiconductor manufacturing company, courtesy their photograph is there. And basically you can see the cleanroom, it is filtered such that the particles are 35 particles in the per cubic feet per unit volume which means we use cleanroom clothing to remove all the dust particles, and there is an air flow maintained and generally you can have it. So you generally have cleanrooms marked as 10, 100, 1000, 10,000 so on and so forth. 100 basically is the best one because there are 100 numbers of particles per unit volume of that area. Similarly 10,000 will also have some particles, so lower the value, higher is the cost for running as well as fabricating the cleanroom environment right, so this is typical environments which you get in cleanroom.

(Refer Slide Time: 29:06)



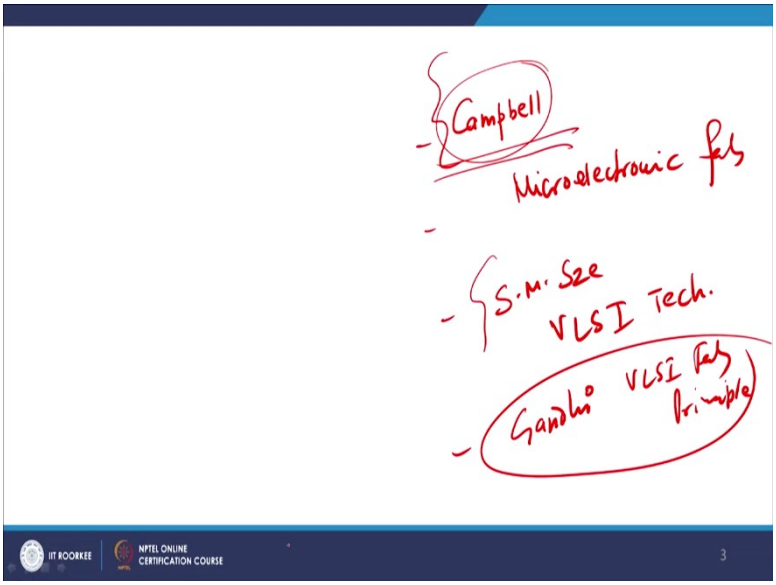
Now the Typical productivity trends which you see over the period of year. Though this is a bit old data 2009 data, holding good still is that the logic is actually growing much faster as compared to the transistor growth rate. It is approximately 58 percent growth is there in the logic right whereas, transistor per unit star is relatively small relatively smaller 21 percent growth is there right and therefore higher the complexity, better is the trend nowadays happening so yield is getting higher and higher in this case. So this gives you a basic trend, so let me recapitulate what we have done till now.

(Refer Slide Time: 29:46)



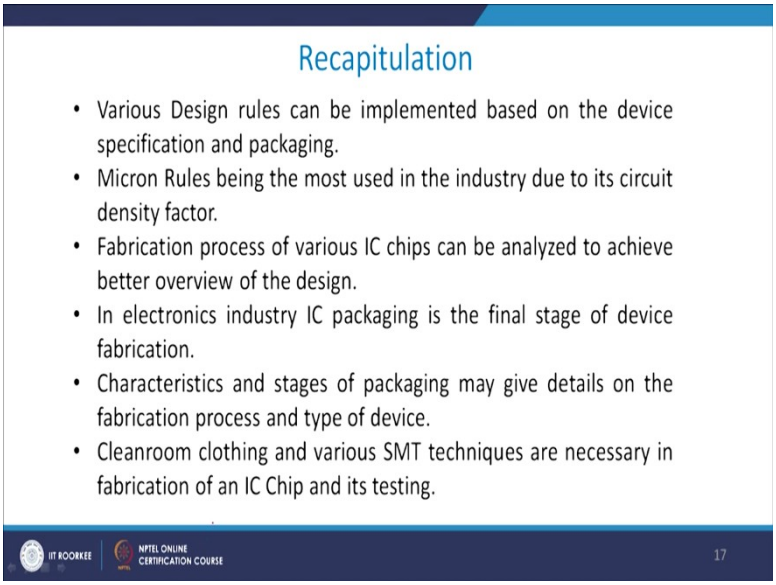
We have understood what are the various design rules which one is the lambda based design rule and another is the micron based design rule. Micron based design tool is the most used in companies due to its circuit density factor. Fabrication process of various IC chips can be analysed to achieve better review, so what you do? You just have to go through the fabrication processes, there are certain good books at which if you refer quite interested to go through a book, maybe I can give you some idea about the books which you can use.

(Refer Slide Time: 30:20)



There is a good book by Campbell on Microelectronics Fabrication. You also have typically SM Sze a good book on VLSI technology, Tata McGraw-Hill I think and but this is what there is a book by Gandhi, VLSI Fabrication principles right Fab principles but I would recommend that this is quite a heavy book, only meant when you are actually wanting to study deep inside the fabrication. Most of you what you will study in Campbell as well as in Sze, Sze is also slightly higher, I would recommend that at this stage if you are doing graduation and if you are actually in the first or second year of the study, have a look at Campbell. If you are slightly ahead and you have already done your bachelors and you are doing Masters, try to read Sze. And if you are faculty somewhere and you are a Ph.D. or post-doctorate maybe look at Gandhi first of all right. So these are the few books which you should be capable of or you should be able to handle them

(Refer Slide Time: 31:30)



We have also understood that the packaging may be given in detail, we have discussed the packaging type. We have understood 2 types of packaging; through holes and SMT surface mount technology, and we have seen how a cleanroom facility typically looks like as well as the trend in the industry towards logic as well as on Semiconductor in general right. With this I thank you for your patient hearing, till we meet next time goodbye!!!!!