Microelectronics: Devices to Circuits
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Module 5: Microelectronics: Devices to Circuits
Lecture 23: Fabrication Process - I

Hello everybody and welcome to the NPTEL online course on Microelectronics: Devices to Circuits. This module is dedicated to the fabrication procedure for an ordinary silicon based design. So, what we will be looking into this module is if you want to manufacture IC or integrated circuits on silicon then what are the steps you should do.

In our previous discussion we have already discussed about in detail about bipolar junction transistors and metal oxide semiconductor field effect transistors and we have also seen what are its possible usage in both digital and analog domain. We will be taking up MOS as an amplifier in our subsequent modules. So, typically as the course is progressing you might be seeing that I am giving you a flavour of both digital as well as analog electronics, right?

Subsequent few modules will be devoted for analog and during the later courses or later sections of this module we will be actually moving to, when we go to week 10, 11 and 12 we will be actually looking into digital applications of these MOS devices. So, this gives you a full breadth of a design flow as far as silicon MOS device is concerned. Now, we have already looked into those basic facts. Now, let me give you a basic idea about the basic fabrication steps which is available with us typically in the design.

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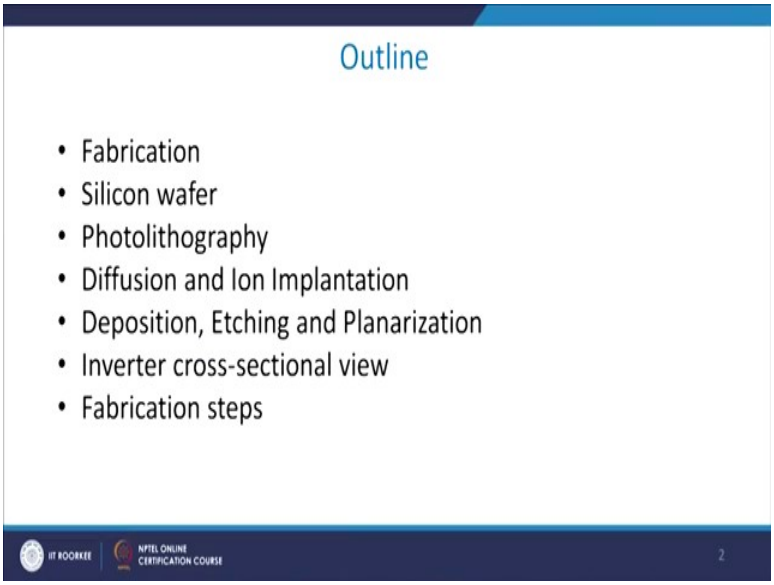

Now, the outline of the talk therefore will be we will be going to the basics of fabrication, right. We are looking into the basics of fabrication. We will actually look into the various concepts or various meaning. What is the meaning of silicon wafer? What are the limitations of silicon wafer? We will also be looking into a very important term known as photolithography which is actually determines the channel length or the dimension of the devices. So, that is photolithography we will be looking into.

We will be looking into diffusion and ion implantation. These are primarily meant for doping doping and then this doping if we want to change the doping or we want to alter the doping then we use diffusion or ion implantation system. Then, for example, if you want to do a metallisation, for example you want to grow a metal then you need to do a deposition or even maybe a simple silicon dioxide growth over silicon will require a deposition.

We require etching because etching will help us to remove the areas where you want to grow metallization. And then planarization means making it plane by doing a by doing a polishing. We will therefore, then going into the inverter cross sectional view from the fabrication point of view. And then finally we will look into the various fabrication steps in this design, right? So, that is a typical outflow for this for this outline for this design for this module. Let me see what is the silicon fabrication?

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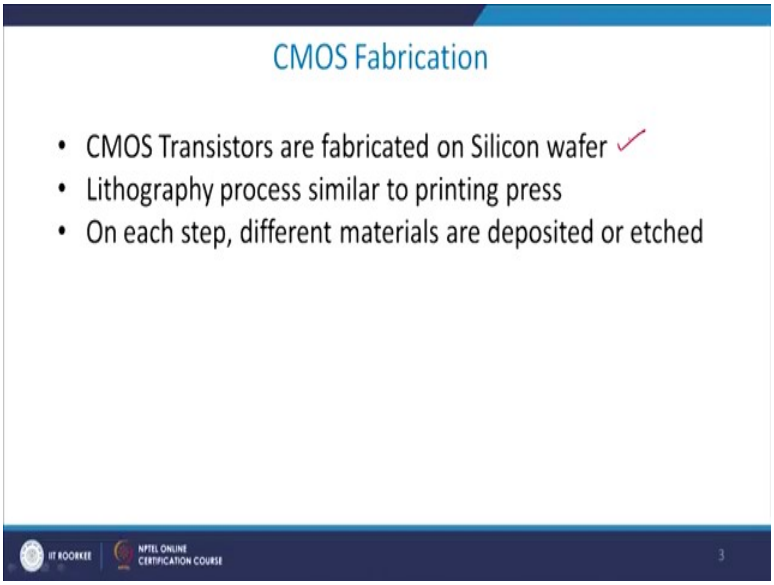

Most of the time as you can see CMOS transistors are fabricated on silicon wafer, right? There are a few reasons for that silicon for 2 reasons. Silicon is first of all, if you go back very clearly, silicon if you look very carefully then you will understand that silicon is very economical in nature, right?

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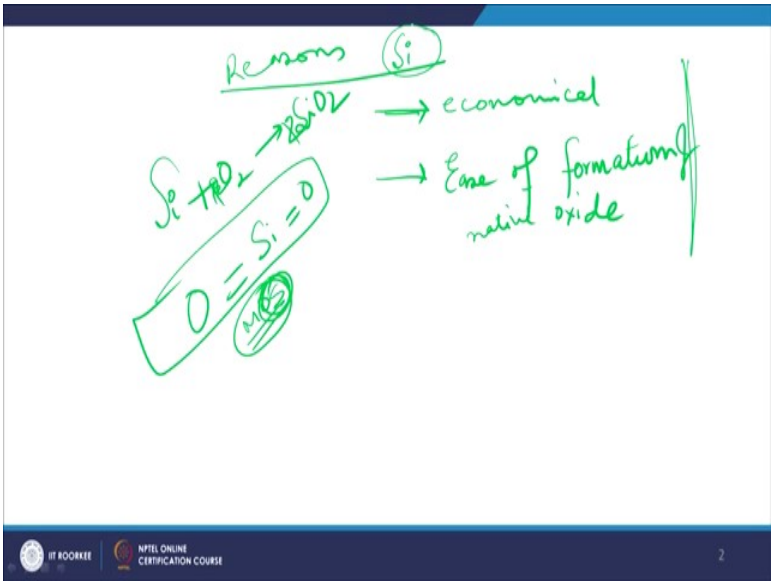

It is very economical. So, that is the reason we use silicon, so reasons for using silicon. If you want to use reasons for silicon, it is pretty economical right, and the second is ease of formation of native oxide, of native oxide. So, if you leave even a simple silicon wafer here it mixes with oxygen to form silicon dioxide, right? So, this is what you get silicon plus silicon dioxide which means the silicon automatically does a double bonding with O and forms silicon dioxide.

So, formation of native oxide is very easy. So, if you want to grow a MOS, this MO metal, sorry MOS, OS which is oxide and silicon is a very natural growth, right? So, that is the reason we use silicon for all practical purposes, right? The cost we pay for it is, for example, we cannot use silicon for optical domain, right? And that is the problem area of silicon then we have to go for III-V, III-V semiconductors. For the time being, we will be concentrating on silicon itself.

Now, the lithography as I discussed with you is just like a printing press. So, what you do is, you have a sort of a silicon wafer over which you want to write something by using by using certain techniques that is known as lithography. Now, every lithographical steps will have different materials. For example, if I want to grow interconnects then I will be using copper in the lithographic techniques. If I want to grow, for example, just the contact maybe I will be using something else, maybe I will be using aluminium to do that and so on and so forth.

So, depending upon the usage of those photolithographic (tech) lithographic techniques, you generally have photolithography an electron (E beam lithography) or direct E beam writing also is there. But these two are the most important ones. Photolithography as the name suggests is very simple. If you if you go back to your basic, this photography right; when you do a negative, what do you is that you do have a negative and you let the aperture open for a small duration of time, light flows in, right?

Wherever there is a human being or a structure outside the reflectivity is low. As a result, the chemical within that negative gets reacted less slowly and other parts gets more reacted and therefore, when you make a positive one you automatically get the image. Exactly the same thing happens in silicon as well. So, photolithography is an important step on each step we use different devices.

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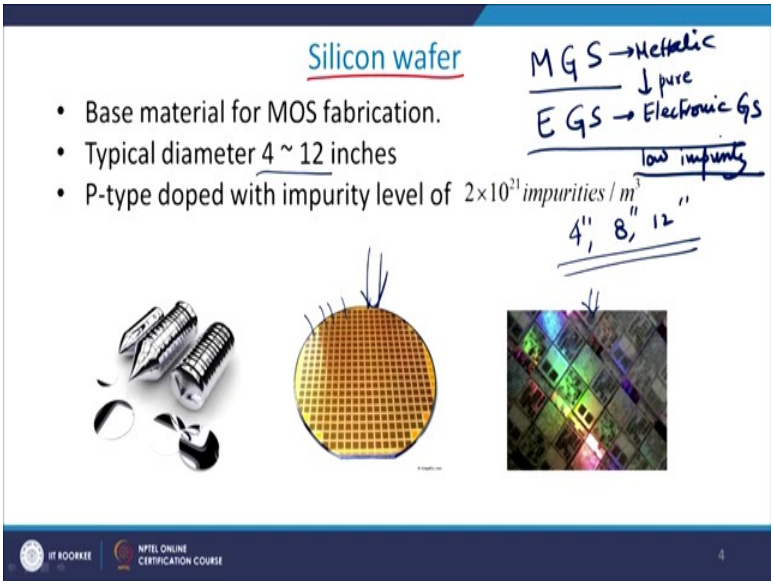

Now, the starting materials is what is basically what is known as a silicon wafer, right? There are 2 types of silicon available to us one is known as MSG which is known as, sorry MGS, sorry. Let me rub it for you. It is basically, it is basically your right, it is basically metal metallic grades silicon. So, it is metallic grade silicon. You also have an electronic grade silicon. So, this is basically your electronic electronic right grade silicon and this we have metallic grade silicon. So, as you can appreciate this is much more purer, so this is much more pure as compared to metallic grade.

So, typically when you fabricate silicon wafer, you first fabricate MGS and then you do more refining to get EGS. So, in EGS you will have very-very low impurity, very-very low impurity both in terms of doped external agent in terms of external agent as well as the crystal itself. The crystal itself will be so even that you would not be able to distinguish between a bad crystal and a good crystal, right? Typical diameter is from generally 4, 12 so we typical have diameters of 4, 8 and 12 inches, right?

So, these are fixed. You cannot have you cannot have more than these diameters of silicon because there is certain fundamental problem area if you go beyond this particular diameter. You will not be able to stabilize the system and moreover there will be large amount of defects inserted within silicon if the diameter of the system silicon grows too large, right? Okay! So, this is the photograph which you see is basically that wafer has been cut into smaller parts. So, each

one of them is basically a silicon chip here and you can actually start doing wafering there. This is the final form of wafer which you see where you are actually doing the layout and the designing.

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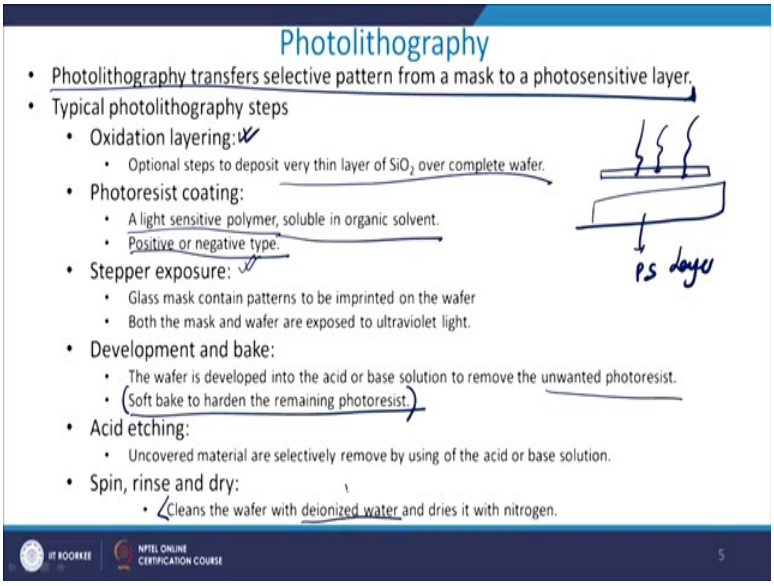

With this knowledge, let me come to the photolithography. Photolithography transfers selective pattern from mask to a photosensitive layer, right? So, I have a mask, for example, if you mask right and if your mask is an open mask here like this then light can filter through this mask and fall onto a maybe a photosensitive layer. So, this is my photosensitive layer, photosensitive layer, right? When it falls there is some chemical reaction. The first reaction is basically your oxidation layering, right?

Typical photography step is that, it is an optional step why because you do not want the wafer to go bad. So, what people do is that let a small width of silicon dioxide grows over silicon. So, a small layer of silicon dioxide is grown over the silicon, right? Over the complete wafer. When you do a resistive coating then what you do is that a light sensitive polymer, photosensitive polymer which is soluble in an organic solvent or an agent and you put a layer of that over this silicon dioxide, right?

It can be positive; it can be negative as well. Positive basically means you can drive it out and let the material remain there and negative means let the material come out the other parts be there.

Now, my third point is basically my stepper exposure. So, you do not have a glass mask over which you have imprinted the pattern by which you want to photolithography. You put it over the wafer and then both mask can wafer are exposed to ultraviolet light. So, when the UV light falls wherever there is a mask there is a transparency the UV light will fall on the silicon and will expose it whereas those areas where you do not want to expose it will remain fixed like this.

Then the wafer is developed into acid or base solution to remove unwanted photoresist. So, whenever unwanted photoresist will be there, you just remove it by via chemical etching and then soft bake to harden the remaining photoresist. The remaining photoresist will be what will be useful to you. So, what you do is soft bake, soft bake means that you do it at very low temperatures and automatically only those photoresists remain there, right?

Acid etching basically means that once you have actually done all these things and removed unwanted photoresists and you have hard baked your photoresist which you want or the required photoresist then you do acid etching. What is acid etching? You uncover by using acid or base you do the partial removal of the uncovered material, right? So, that you do not end up having spots in your wafers. Then you do what? You clean the wafer with a deionized water distilled water also referred to as deionized water and dry it with nitrogen, right? So, we get the wafer with us in a detailed fashion.

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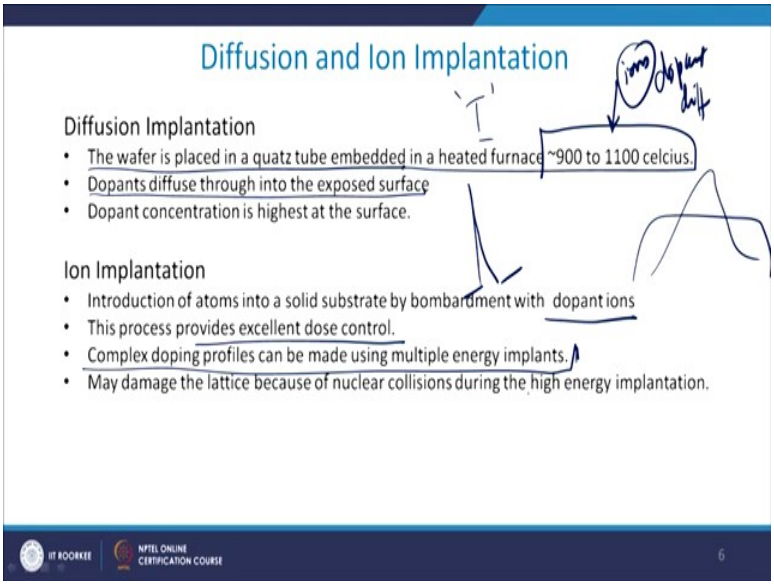

Now, let me do a diffusion and ion implantation. Well diffusion as the name suggests is basically for (purp) generally for the purpose of dope inserting dopant species and as the name suggests what does doping do? It carries species from region of high concentration to a region of very low concentration and as a result what happens is that there will be a diffusion species between point A and point B.

Depending on the concentration gradient as well as on the diffusion constant of that particular material, the particular material will either sink deep inside the original species or if it is not much ahead of it, right? So, as I discussed with you dopant, so typically the wafer is placed in a quartz tube because it is quite pure and you do not have any reaction on quartz and it is heated in a furnace with 900 to 1000 degree centigrade. So, when you heat it becomes more reactive in nature, right?

And therefore, you allow dopant species to diffuse through it, through the exposed surface. Of course, as you can understand the diffused species dopant concentration will be highest at the surface and as you go inside the surface, the percentage of the dopant species starts to fall down, right? And these are standard problems area which people face while doing doping is that the doping is always highest on the surface and goes on reducing as you move within the surface, right? And therefore, the doping concentration is highest on the surface.

Please understand diffusion is again temperature dependent phenomena, right? So, on chip temperature you do which is basically by heated furnace will determine the most optimal value or the procedure for fast movement of ions, right? Fast movement of dopant ions in this case through using diffusion. So, it is very critical to set your temperature of the quartz tube in such a manner that it is the most optimized one.

So, for example, if you keep it very largely heated up the chances are that the dopants will move so fast that it might not sit even with the silicon because energy is very high. Similarly, if the gradient is very-very small then it would not be moving from point A to point B by virtue of diffusion and that is you should be very careful about as far as diffusing an ion implantation is concerned. Let us look at ion implantation.

What is ion implantation? Ion implantation is bombardment of dopant ion using an accelerator. So, you should have a good accelerator. This process provides an excellent dopant control, right?

And complex doping profiles can be made using multiple energy implants. Say you want to first of all make something like this, right? And then you went on to make something like this. This is the dopant profiles. You can easily do using ion implantation, right?

For example, you want to make a profile something like this up so peaked, right? Then use a Gaussian profile and make your FWHM - Full Width at Half Maxima as possible and keep your doped D as large as possible, dopant species as large as possible. So, within a short domain, since, we have developed FWHM, FWHM is at Full Width at Half Maxima, right?

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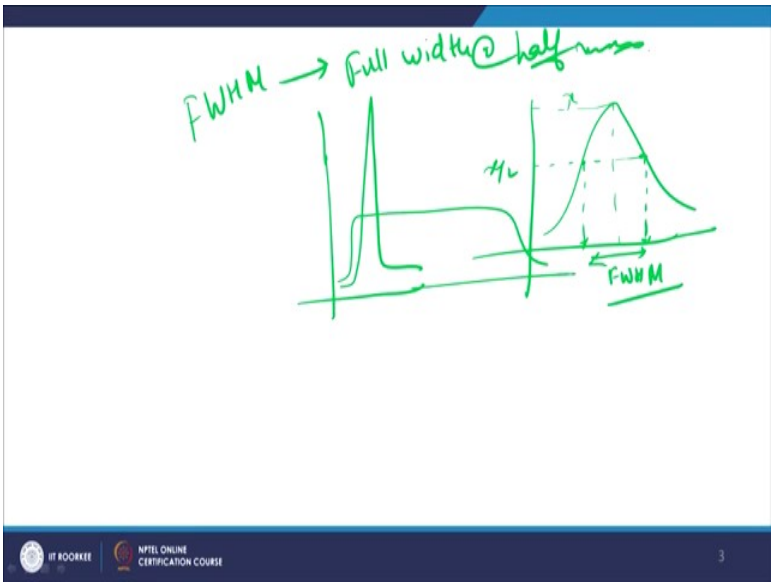

FWHM if we want to point out FWHM. This is basically Full Width at Half Maxima which means that if I plot using a may be a Gaussian surface, then we try to find the maximum value which is this one, X. And we draw a graph which is from X by 2. This is X by 2 and then we check the values of dopant species here and then we say that this is my FWHM, fine? So, this is Full Width at Half Maxima, right? So, when you get Full Width at Half Maxima it means.

So, now if you want that the profiling should be peaked or you should have a peaked profile, keep your FWHM small and you can actually get a peaked profile. Similarly, if you do not want a peaked profile you want a wide profile then it is also advisable to keep wide profile and you get something like this. So, depending upon the type of dopant species you are using and the type of

temperature which you are using you can actually have either a either a like you can either have a proper control over the channel and ion implantation and other channel wise.

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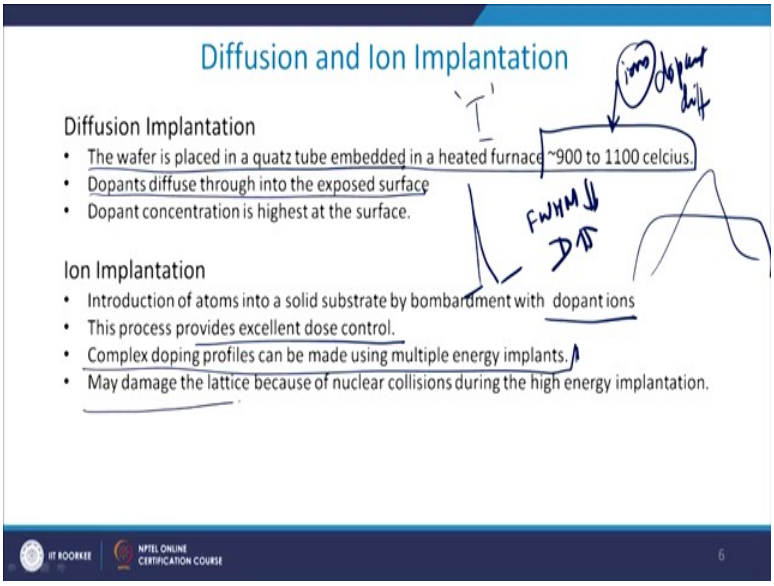

So, but the problem with this ion implantation is that the energy is so high the energy is so high that you end up having maybe dislocation of the atom itself through which these charged particles are passing, right? And that is a problem area which people face.

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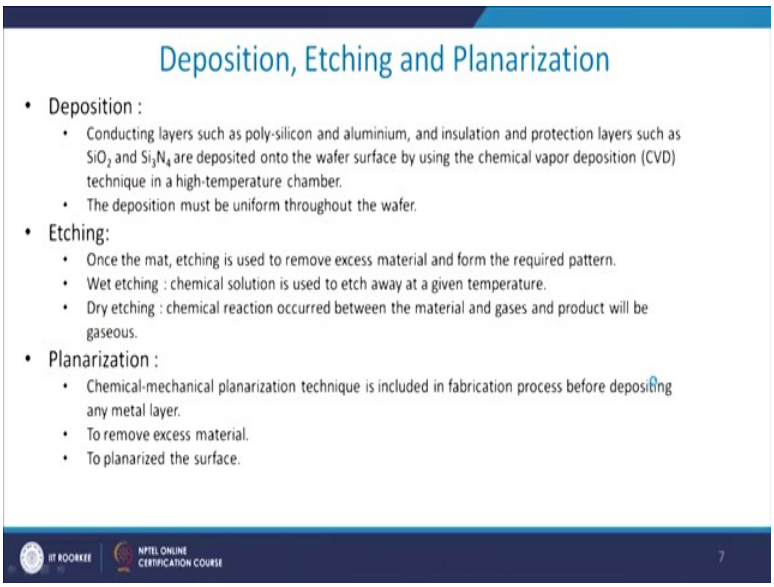

Let me come to deposition. When deposition is conducting layers such as poly-silicon and aluminium, and insulation and protection layers such as silicon dioxide and silicon nitride and they are done by CVD process at high temperature high temperature chambers. So, I have a high temperature chamber, right? So, once I do a CVD which is a chemical deposition and I deposit layers of silicon dioxide and nitride which is both by the way directive in nature over this area.

Now, so, once you have actually the material and then you have been covering it with the material across the board then what you do is that depending upon the pattern where you want to photolithography to work, you start to remove; if you are doing a positive photolithography start to remove those areas or etch those areas through which you want the light to go inside, right? And you do that easily using any of the dry etching or the wet etching, right?

So, chemical, in case of wet etching we use a chemical solution to etch away at given temperature. What is dry etching? Chemical reaction occurred between the material and gases and the product will be the gaseous itself, right? So, seldom people use dry etching most of the people use wet etching and that is the reason why, the reason for wet etching is simple but the cost you pay for it is that you are not very accurate in terms of appropriate etching, right?

What do you mean by planarization, it basically meaning chemical mechanical planer mechanical planarization and is used to techniques fabricate any metal layer to remove excess material and to planarize the surface, right? So, what will we do is that they have a planarization technique by which excess layer is removed first of all. And after the removal of excess layer what you try to do is that you try to have the model layer perfectly plane in dimension.

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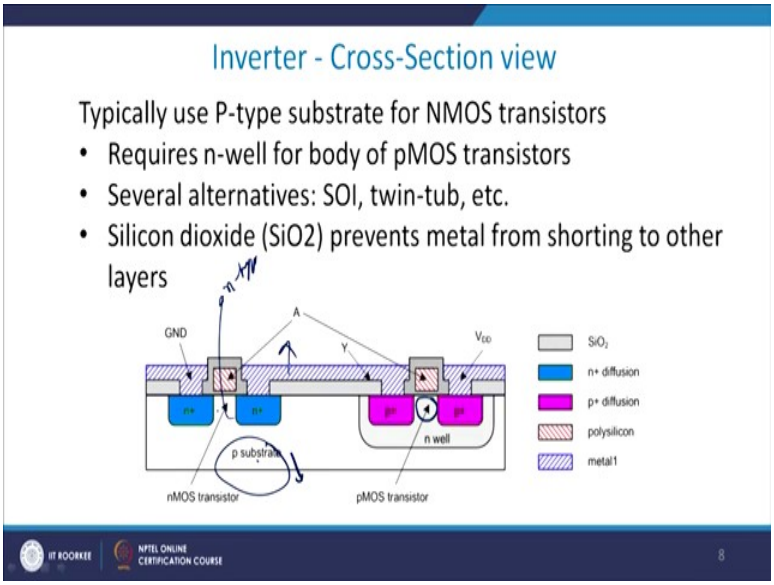

So, let me see inverter cross section view. In this you can basically see it is a twin-tup process and in twin-tup process I have p type substrate. This will act as the substrate for NMOS. However, you need to grow an n-well within the p substrate, for a p type substrate to be formed here, right? So, for a p type substrate to be formed here you require a, you want to have a pMOS transistor, try to make this one. So, this is basically your n-well and you try to make within the well another well which is basically n-well and from there you can get the value of your p type material.

Similarly, the p substrate itself adds a substrate to the MOS transistor which is basically your n type. And therefore, this is your n type substrate which you get. So, I want n type and p type, they are separated by this metal 1, right? So, this metal 1 is separating the 2. And from here and here and here you take the output value of voltages or currents, right? Okay!

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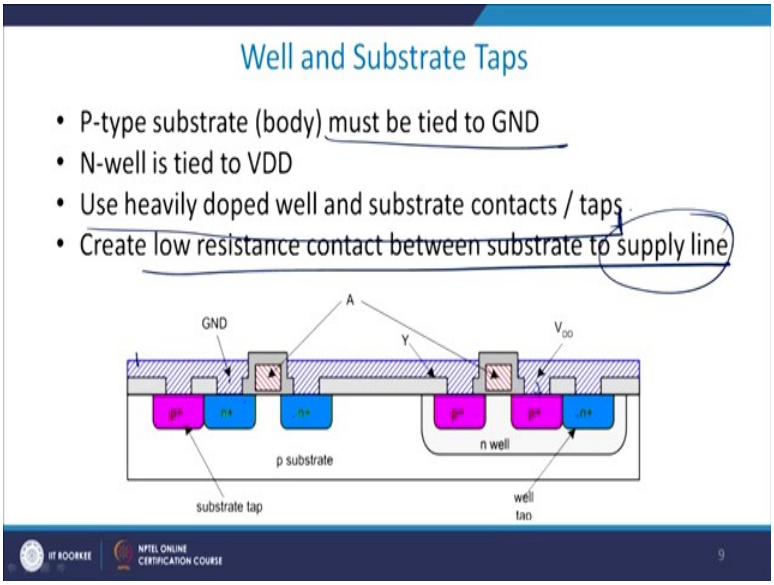

Let me look at the well and substrate taps. So, I have a well tap which is basically my, the well tap and substrate tap if you look carefully. This is my ground tap, right? This is my ground tap. These 2 are the taps where you put an input, right because this is gate to, this is gate to source. This is also gate to source and therefore, I would expect to see these to be latched together and this is the value of V_{DD} which you use. And here is another well available with you, right? So, these are a few n-well processes which you use which is typically there with us.

Now, any transistor or mask, sorry, any substrate must be tied to the ground. So, if a p type substrate that must be tied to the ground, right? So, I have a p type substrate always tied to the ground and n-well is always tied to the V_{DD}. N type devices are always tied to higher value of voltage and p type devices are always tied tied to a lower value of voltage, right? And use heavily doped wells and substrate contacts taps. So, if you use if you use very heavily doped wells and also substrate contacts, your effect of n will be reduced drastically in a device, right? Now, you have moreover you have to create a low resistance contact between substrate and the supply line.

Otherwise, if you do not do that there will be excessive voltage loss across the across the across the supply line. And therefore, effective voltage available to you for running the MOS device would be relatively small, right? And that is the problem over here.

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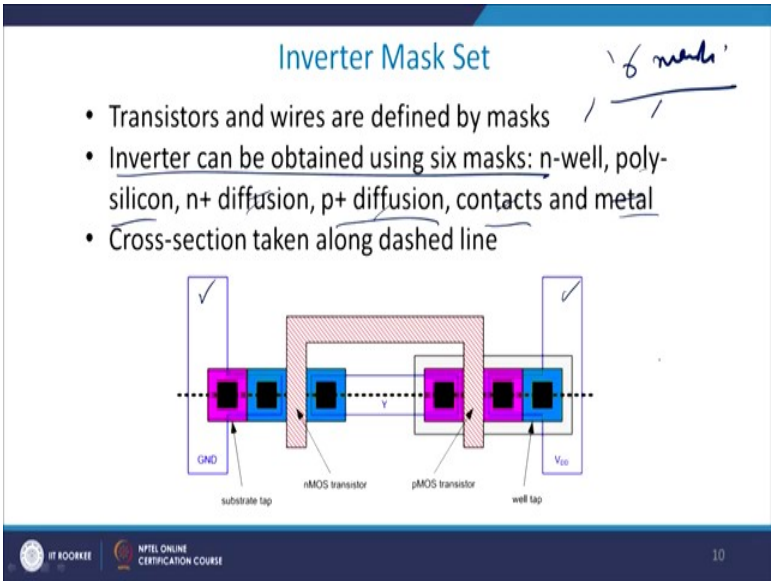

Now, let me come to the inverter mask set, right? We have got transistors and wires are defined by masks. So, these are basically the masks which are available with you. And inverter can be obtained by using 6 masks; n well, poly silicon, N^+ P^+ diffusion contact and metal, contact and metal. So, it is 1, 2, 3, 4, 5 and 6. So, you require 6 masks in order to do it right and 6 masks can easily be purchased and can be used.

But, when you use these masks for fabrication purposes the fabricator will come to you and ask you to change this mask according to his fab lab right according to his fab lab. So, please be careful that just by saying that you have been able to generate the fabrication mask means that you have done everything, no. Fabrication mask as well as its final utilisation is quite important as far as inverter mask is concerned.

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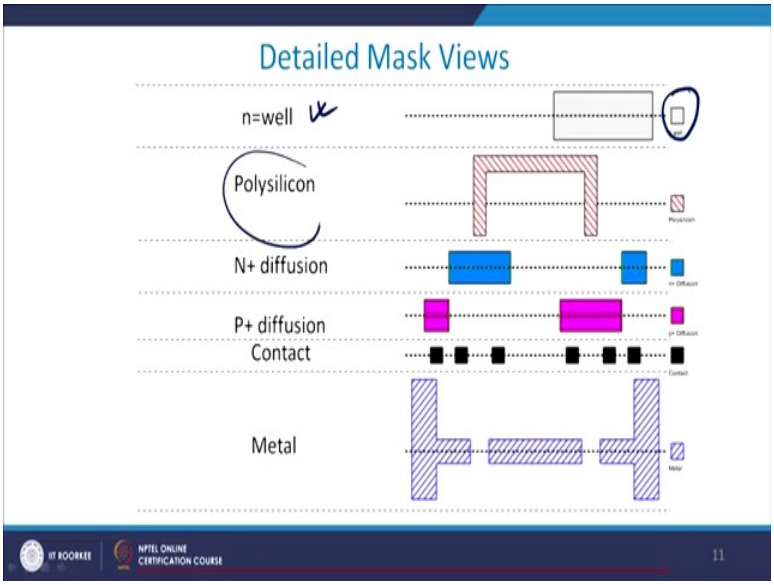

Let me give you a brief idea nothing to worry about you have to just learn. For n-well this is the mask which you see in front of you for p poly-silicon it is this thing, right? For N^+ diffusion we have we have N^+ diffusion shown by red. This is for P^+ diffusion, right? P^+ and this is the contact which is given by the black one, right? So, so if you look at this point metal is this and this are metal, right? And this is also a metal which is available with us and it is connected in series like this, right?

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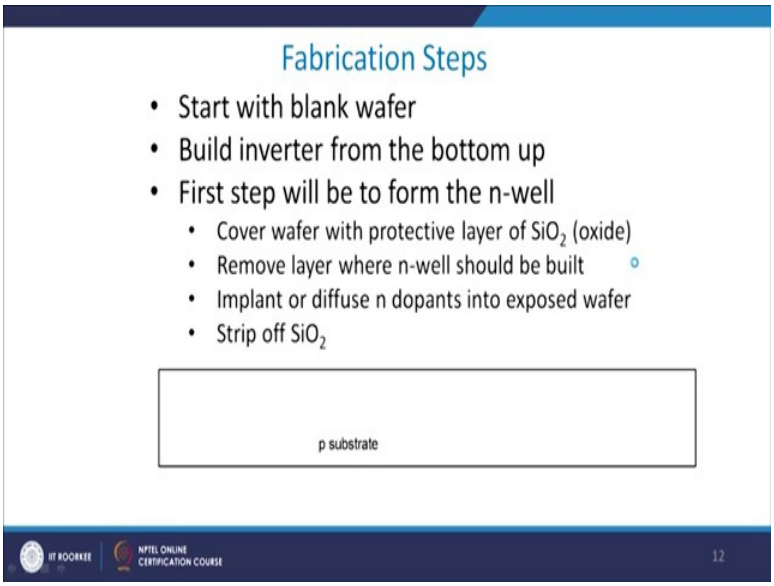

Let me start now with a blank wafer and let me innumerate the fabrication steps which are there. We start with the blank wafer build inverter from the bottom up. First step is to form an n-well cover wafer with protective silicon dioxide we discussed this point, right? Sorry, with silicon dioxide remove layer where n-well should be built. I think that is clear why n-well should be built. So, remove the layer where you want to remove where you have where you have plan to have n-well and implant or diffuse dopant into exposed wafer, right?

So, we appropriately change into n type or p type and then strip off silicon dioxide. So, you have a silicon dioxide initially present over that you form the n-well. And after the formation of n-well you try to do a protective covering of silicon dioxide. Remove it and remove it, and try to do your implantation or diffusion using dopant species which are basically your non silicon dioxide based, right? And then if you are using silicon dioxide based, then strip off the silicon dioxide and throw it outside.

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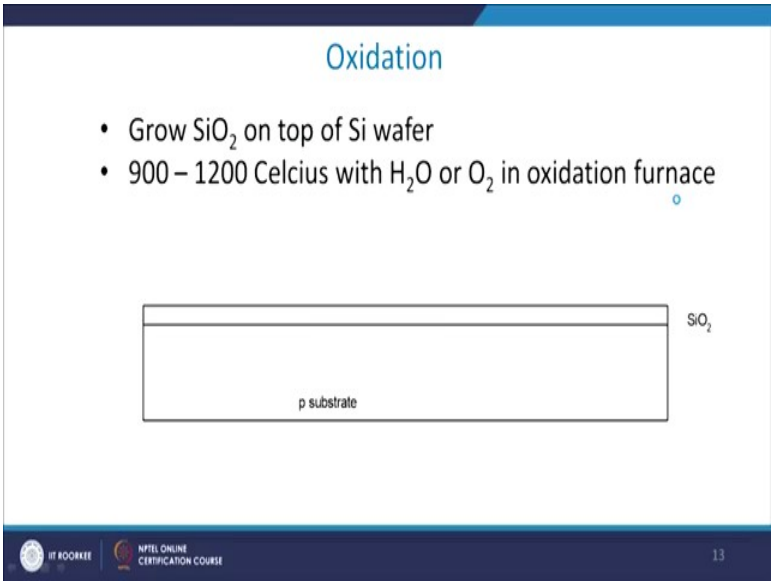

Now, oxidation is you have to grow silicon dioxide on top of silicon and the temperature range is basically 600 to 1200 degree centigrade, right? With H_2 Oand O_2 is basically the reason you are putting this acts as catalyst, right? They act as catalyst means they themselves do not part in the reaction but they hasten the speed of the reaction in a much more detailed manner. So, we use oxidation for doing all these things and it is done at 900 to 1200 degree centigrade.

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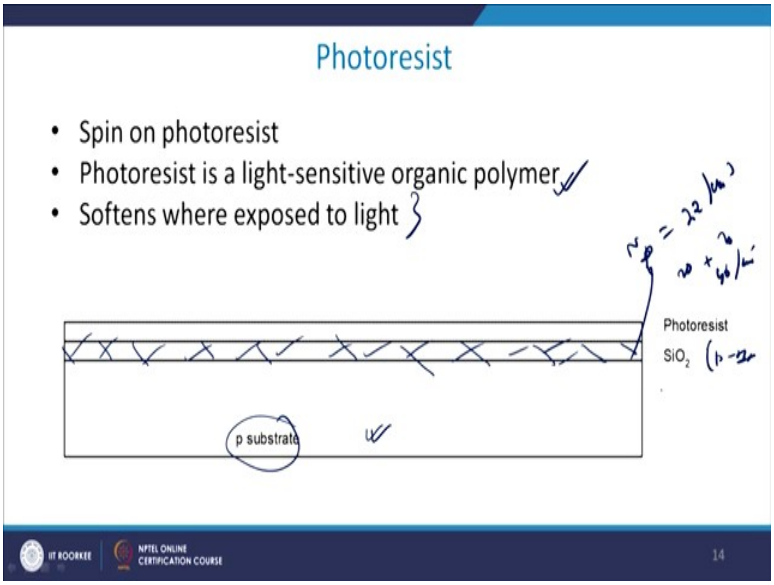

So, what is a photoresist? Photoresist as I discussed with you is a polymer photosensitive material in which if the photons fall, it becomes sensitive to input voltages and there is a problem. Now, as I discussed with you photoresist is a high-sensitive organic polymer. For example, there are many organic polymers available and what are the examples that happen to be photoresist? Now, so when you expose to light it softens that the photoresist itself softens when light is exposed to it. So as you can see here I have the native p type substrate I what do you mean I do something like this which means that I try to make this internal one as to be as silicon dioxide maybe p type.

So, what we get from here is that that you get np to be equals to say you had 16 plus and suppose you add 16 and now you have 6, 16 plus 6 will be 22 per centimetre cube, right? Whereas if you have metal layer you will have already 20, so 20 plus large number 26 per centimetre cube. So you can see same technology and you get a larger doping profile as compared to the previous case.

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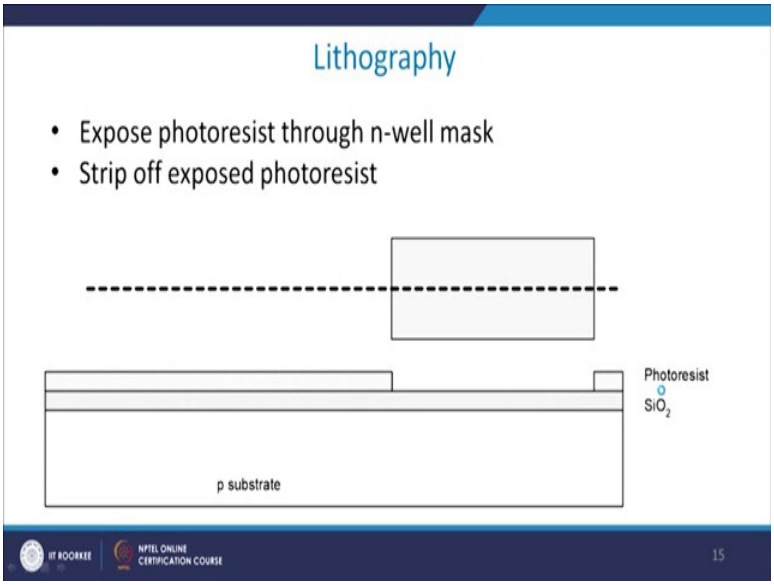

So, let me come to lithography, you need to expose the photoresist through an n-well mask, right? And then a sign of strip off the photoresist. Once you do that you are stripping off your all other things. So, what you do is that this is basically you're the photoresist that has fallen on to this bank this bank. And as a result, you strip off the photoresist from this directly, right?

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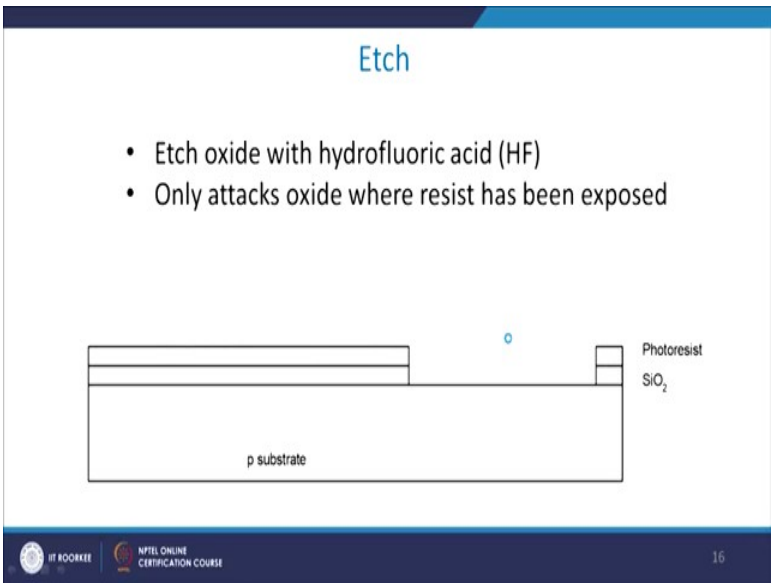

What is etching? Etching means that, You etch the oxide with Hf. So, I have an oxide formation means I want to remove it for whatever reasons. Then what I do is I put Hf or hydrofluoric acid

and that strikes off that metal layer and there is and makes it almost non-existent. HF actually attacks the oxide layer where there is no, where the resist has been exposed, right? So, wherever the resist has been exposed this HF will try to attack those exposed parts in order to reduce the value of your or to reduce the attacks, right, parasitic attacks or others.

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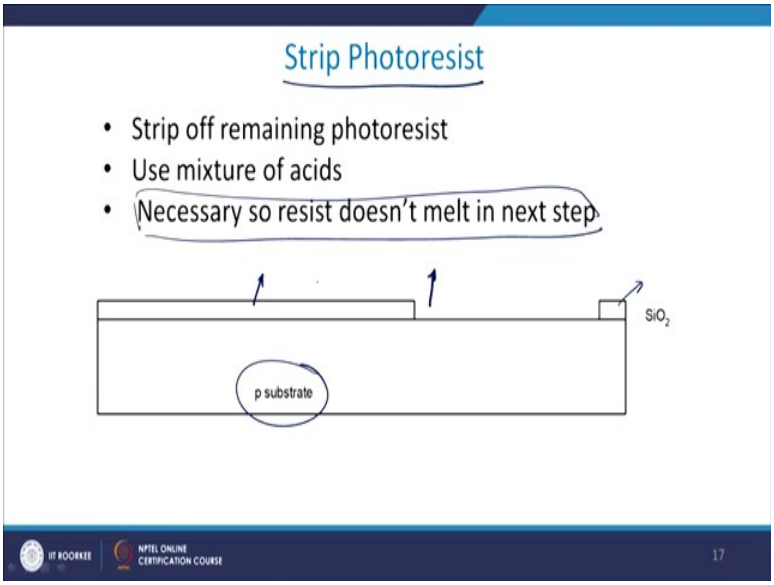

Let me come to the strip photoresist. As we are discussing we strip off the excess photoresist, we generally use in this cases. So, we have a strip photoresist which is basically what you do is remove the photoresist from here and the remaining part is what is there, right? So, the reason we strip off is that we do not want the other part to melt away, right? So, in the next step when we do we do not have to melt the photoresist. So, we strip off the remaining photoresists. This is what we have stripped off. So, I have a silicon dioxide layer here and I have a p type substrate over which I am doing the photoresist, right?

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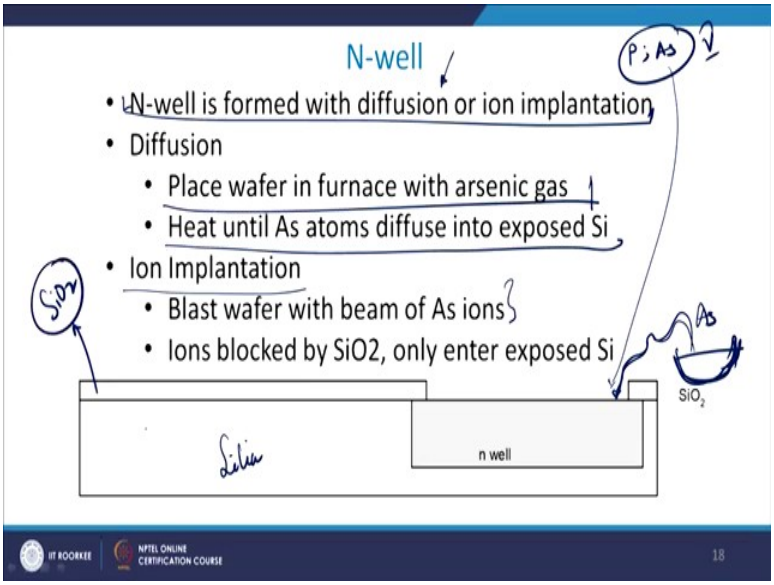

We come to the n-well formation. Now, n-well basically meaning that you are doping with either n type dopant concentration which is basically either phosphorus or arsenic, right. This is group V element which you are doping with and what you do is that this n well is formed with diffusion or ion implantation, right? So, typically in most of the organisation or fabrication techniques we use diffusion, right?

What we try to do is that the phosphorus and arsenic are kept in a chamber at elevated temperatures and then and this material is kept at a lower temperature respectively. So, there is a temperature gradient and there is also a dopant gradient which results in the atoms of these phosphorus and arsenic coming towards and sitting at these positions, right? And you do have do have diffusion.

You can control the speed of the diffusion by changing the temperature also by changing the dopant species. You can also change the amount of dopant species by increasing or decreasing the dose in the ion implantation machine. So, the diffusion if you look we use arsenic gas in a furnace, right? What we do is that arsenic gas is there and we heat it as arsenic atoms diffuse into exposed silicon. So, the arsenic atoms will diffuse and sit, these arsenic atoms will from maybe a this thing a glass and from there the arsenic atom will be coming and sitting on the silicon wafer which is this.

The silicon wafer which you see, right? And silicon dioxide, right? In ion implantation we try to do blast with arsenic atoms. So, arsenic ions are there since, you are accelerating you require the particle to be charged and therefore, you have to first ionize your arsenic or phosphorus atom. So, when you ionize your phosphorus or arsenic atom, then you through an electric and magnetic field you try to push it and a large dose of that charged particle falls onto the material.

As I discussed with you earlier, I can change the dose as well as the doping concentration directly. Now, so now you can understand why this silicon dioxide is so important. The silicon dioxide is important because then this silicon dioxide does not allow for these arsenic or phosphorus atoms to enter in these regions. So, this region is devoid of those group V materials whereas this region is having large amount of group V materials and therefore, it is basically your n type well is formed, right?

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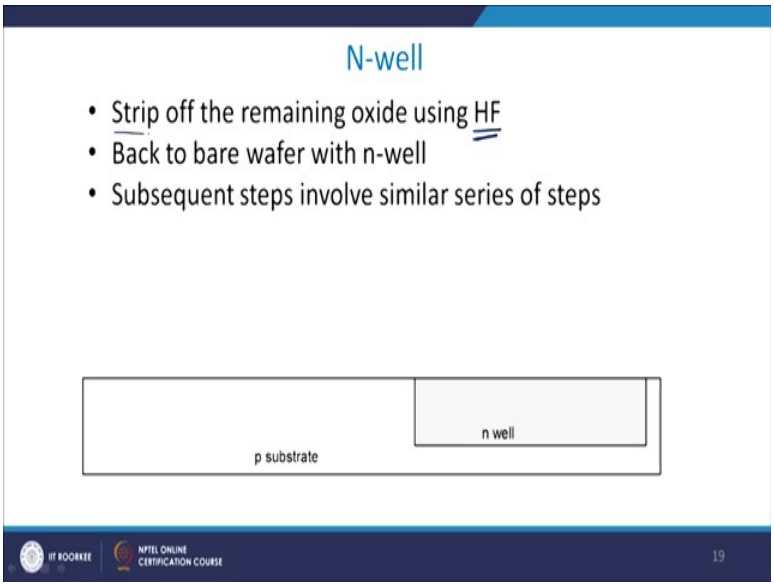

Now, we come to the n-well. We are using HF or hydrofluoric acid. We strip off the remaining oxide, right? So, whatever oxide layer was here at this point and at this point we just use HF to remove it. Then therefore, now what we have is the bare silicon wafer which is this one and we also have n-well which is kept here, right? And we will be using similar steps later on.

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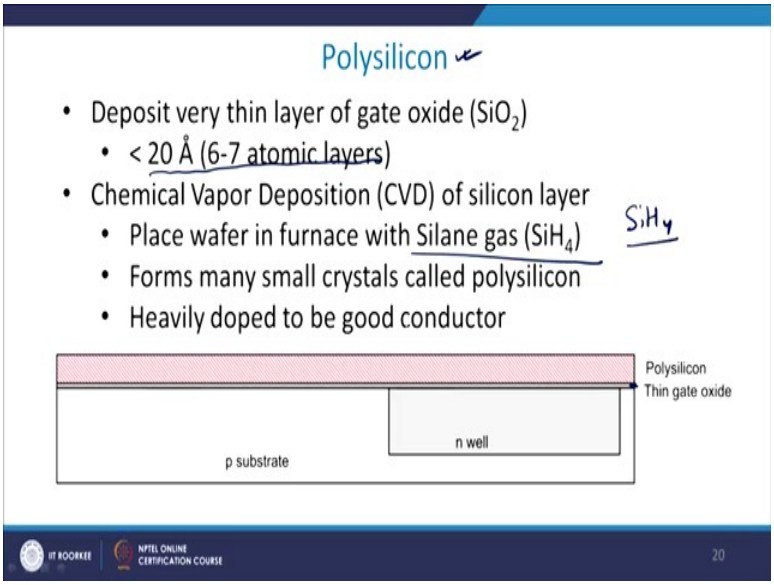

After this we grow a layer of polysilicon. This layer is polysilicon, right? We deposit a very thin layer of gate oxide. So, this is basically a thin layer of gate oxide which you see here. This is a thin layer of gate oxide, right? There is approximately 20 A^0 which means approximately 6 to 7 atomic thickness available to me. Then you have then after this after we have grown the gate oxide which is basically native growth you allow for CVD and you use a silane gas SiH_4 to do that, right? Silane gas will be forming and form small crystals and they form polysilicon.

So, polysilicon is basically sort of a silicon arranged in a special manner. They are crystal in small domain but in larger domain they are still amorphous in nature. So, they are heavily doped. You can heavily dope it to be a good conductor, right? So, polysilicon is used in that manner. So, now you have polysilicon, you have a thin gate oxide then you have n well and then you have p type substrate.

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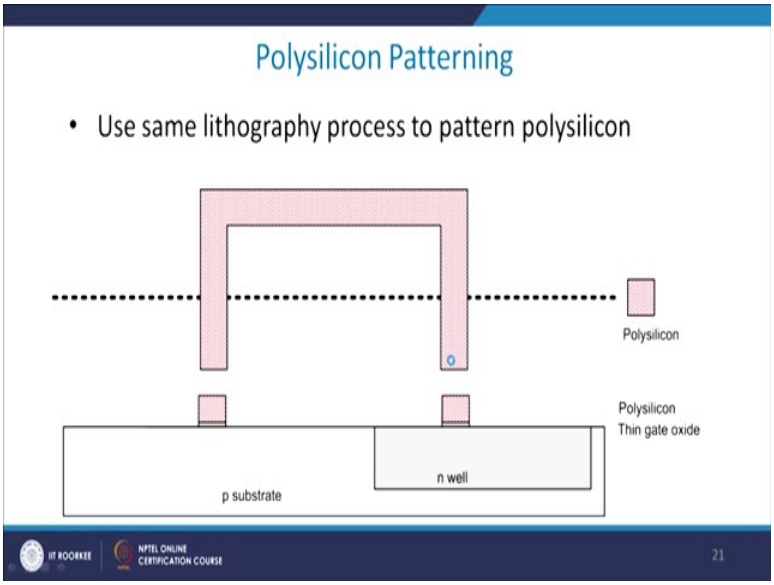

Now, you use the same lithographic process to pattern the polysilicon. So, what you do? You use a polysilicon you have a n well here, and then you pattern it say, for example, you want to grow here and grow here; the same procedure which I discussed earlier you can actually etch and remove the oxide layer and the polysilicon layer at these places, where you have marked it which is discussed in our previous lecture. An important point which is current technology is that you require self-align processes. Self-align primarily means that if you have a.

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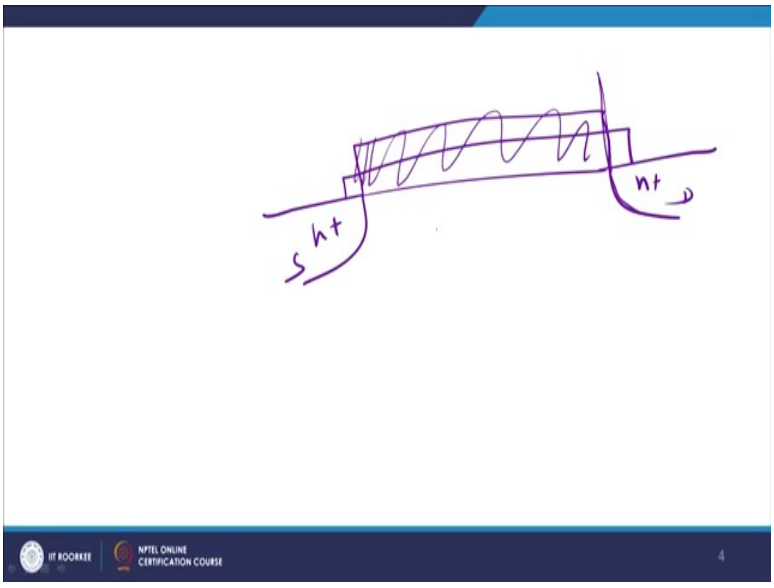

Let us suppose you have a device you have a device which is something like that this is your n and this is your p. $N^+ N^+$ and this is your source and drain, right? If this is overlap so you would be overlapping with it. Self-align primarily means that you should have your oxide layer like this. This is the oxide layer. This is the oxide layer and this self-align means, when the alignment of the oxide and the metal is exactly that way as that of the source and drain material source and drain material.

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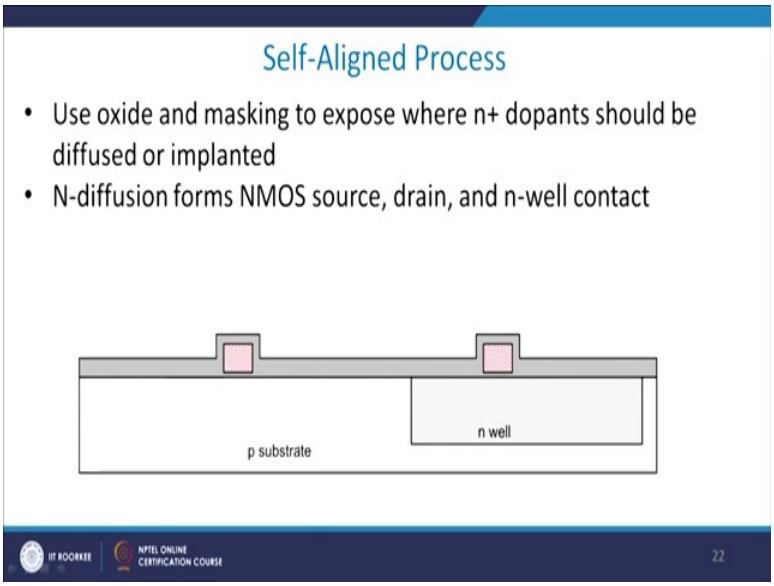

And that is how you do it here. So, what do you do is that you grow it like this and then use oxide and masking to expose N^+ dopants should be diffused or implant means now, what we do is we expose the polysilica and we try to those places where we want the N^+ dopant to go we expose it and for other reasons we stop it. Now, n diffusion forms NMOS of course, and if you want to have p type device you will have p type diffusion and therefore, you will have n-well contact, you will have source and drain available with you.

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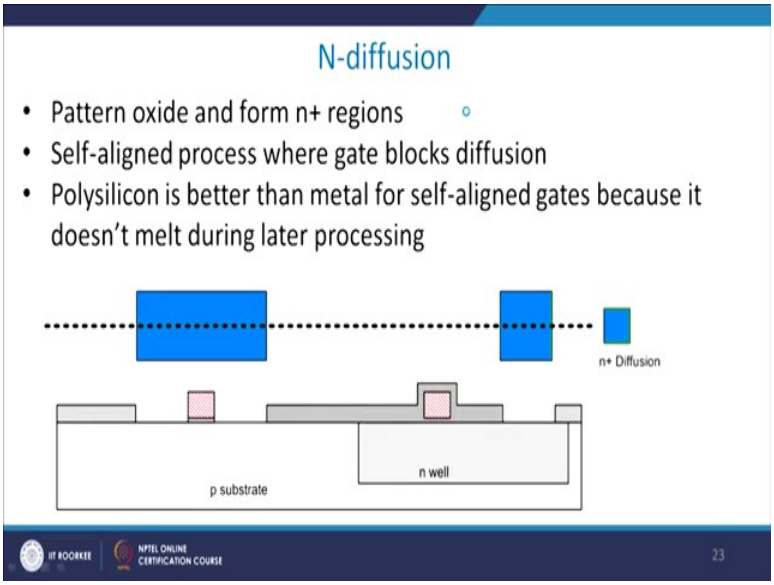

We also use the n diffusion as I discussed with you these are actually self-aligned processes where gate blocks the diffusion. So, gate will be typically polysilicon. You try to put your diffusion from outside and the gate will block it from going inside just below the gate. So, polysilicon is better than metal for self-aligned gates because it does not melt during later processes, right. So, its melting point is relatively high for polysilicon as compared to even metal, right. And that is the reason you make it. So this is the diffusion, right? So, this will be N^+ diffusion here and there will be N^+ diffusion here as well as at here.

So, this gate will not allow this diffusion to go inside this material, right? Okay, So, after you have actually diffused into the n type material now you have N^+ region here you have N^+ region here and you have N^+ region already from, right? Now, usually nowadays initially we used to have diffusion but now we used ion implantation to do it but still historically it is done by diffusion. So, I have an n-well here and I have diffusion. So, this is a diffusion, this is a diffusion and this is a diffusion generated region. Now, what you have done is let me see what we have done. Therefore, now, what you can do is you can strip off this layer of polysilicon, right?

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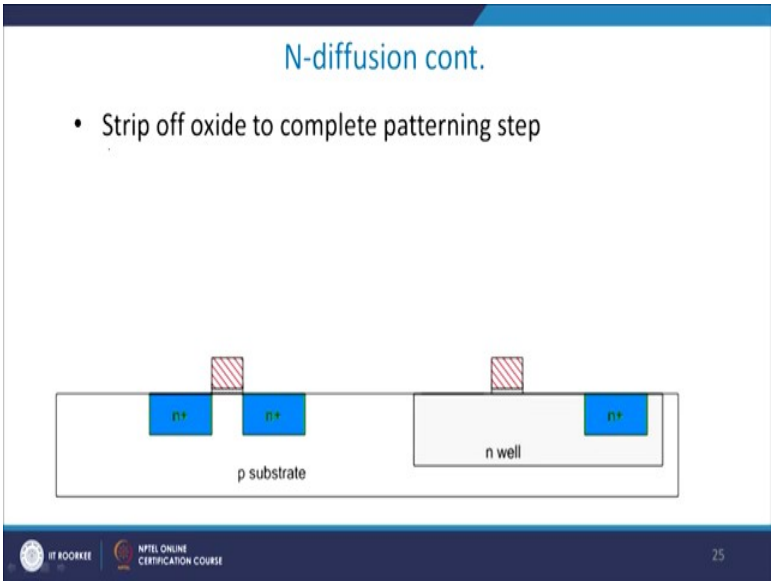

So, next slide as you see I have removed this polysilicon by doing oxide layer. You remove the oxide layer and therefore, what we have done is all the oxide layer here has been removed. If you go back to the previous slide this was the oxide layer which was there. Now, by doing HF etching or using some other technique I can remove this oxide layer directly and I get almost devoid of any oxide layer in this case, right?

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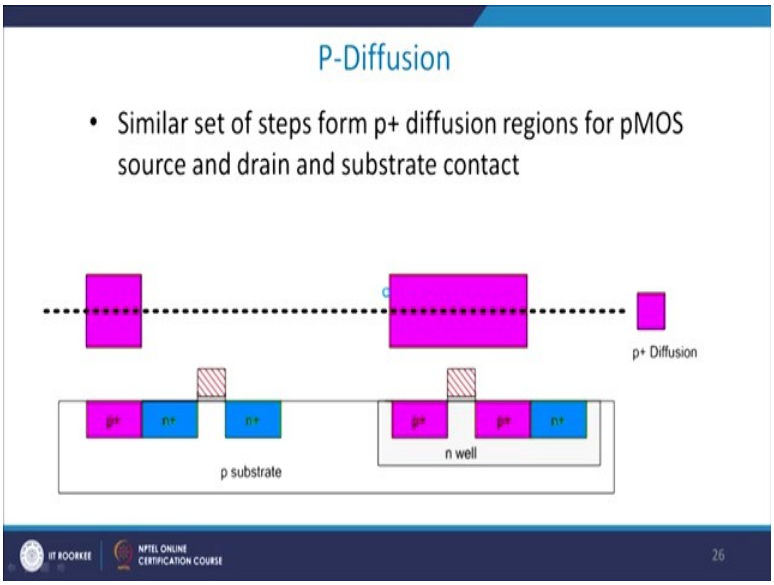

If you want to do p type dopant and n type dopant is finished, I have an NMOSFET formation here but I also hold a p formation over the n-well. So, what I do is that, we exactly as we started with diffusion with n type MOSFET we do diffusion using a p type material which is group III boron material. And we dope it with source and drain and substrate contact. So, what we do source, this is the source, this is the drain right, and the substrate contact which is this one. All these 3 can be done using the p well diffusion process.

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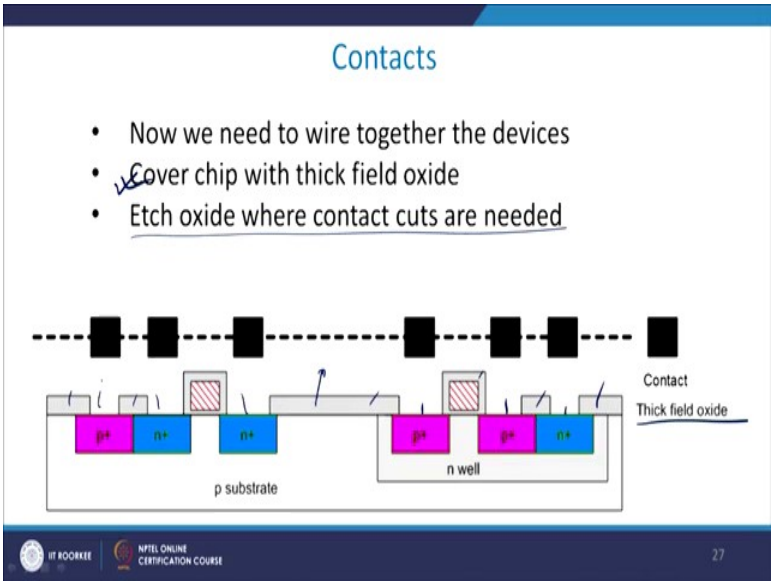

After we have done the p well we need to have the final layer which is the metal layer and to do that you require the grower contact. So, what we do, we cover everything with a field oxide. Field oxide is a very thick oxide. So, this is the field oxide which you see, thick field oxide. This are very thick field oxide here, right here, here,,, When you grow it you do not allow any external species to enter anywhere else except the region which you have opened. Now, what do you do? You cover it with thick field oxide and then etch oxide where contact cuts are needed. So, I etch at this point at this point at this this this and this, right? And then you grow the contacts here.

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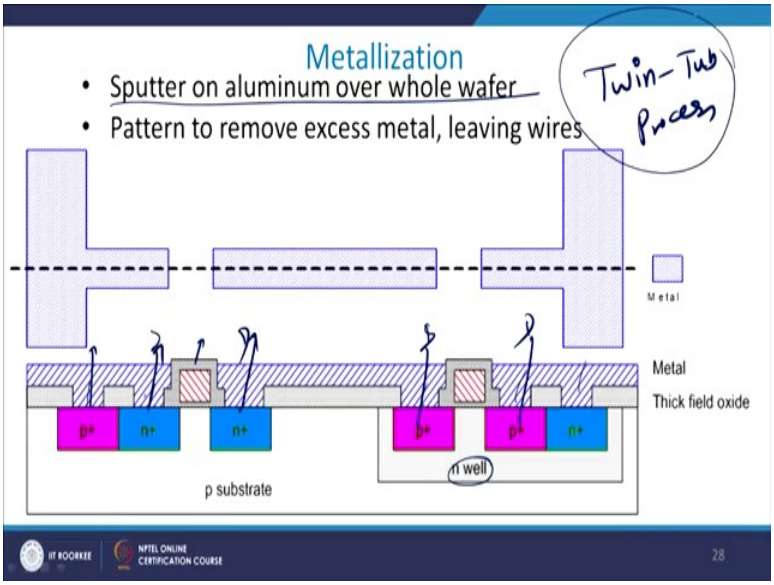

Once, you have grown the contacts which is this one; we have grown the contacts, we then sputter after we have grown the thick oxide layer. Now, my now my region where you want to grow the oxide is opened. Then what I do? I sputter with aluminium over the whole wafer. So, I do a sputtering using a sputtering technique; I sputter over a whole aluminium. The aluminium actually sits at those places which was opened, right?

These were open spaces and the metal fills in all these open spaces, right? And as a result what happens is that sorry, as a result what happens in this case is that now you do have now what you can do is now you can now you can remove this etched oxide here, right. And you will have a contact here, a contact here and a contact here. So, these two will be source drain contact for NMOSFET. This will be source drain contact for source drain contact for PMOSFET.

This is also known this whole procedure is also known as twin tub process, right? Because you grow a p substrate, you grow an n-well within that and then this is known as a twin tub process. With this I have given you a brief insight into the flow of fabrication in a silicon and we will take up further issues in this as we move to the next slide. Thank you very much!