Microelectronics: Devices to Circuits
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Lecture – 21
Power Analysis - I

Hello everybody and welcome to the NPTEL online certification course of Microelectronics: Devices to Circuits. In our earlier modules and interactions we have understood what is the meaning of propagation delay of an inverter, we have also seen how an inverter using an N-channel MOSFET and a P-channel MOSFET can be formed and what is the basic electrical functionality of a inverter, we have also seen what is the meaning of noise margin as far as inverter characteristics is concerned, what is the meaning of voltage transfer characteristics, how we are able to calculate the high noise margin and low noise margin, and its importance in terms of digital as well as analog logic.

We have also seen the various functionalities of basic inverter and the basic concept of power dissipation. In this slide or in this module we will be actually dealing with the concept of power analysis in a much more detailed manner, so that is what the outline of this talk is that and therefore, it is named as power analysis part 1. Let me give you an let me give you an idea about what the power analysis is all about.

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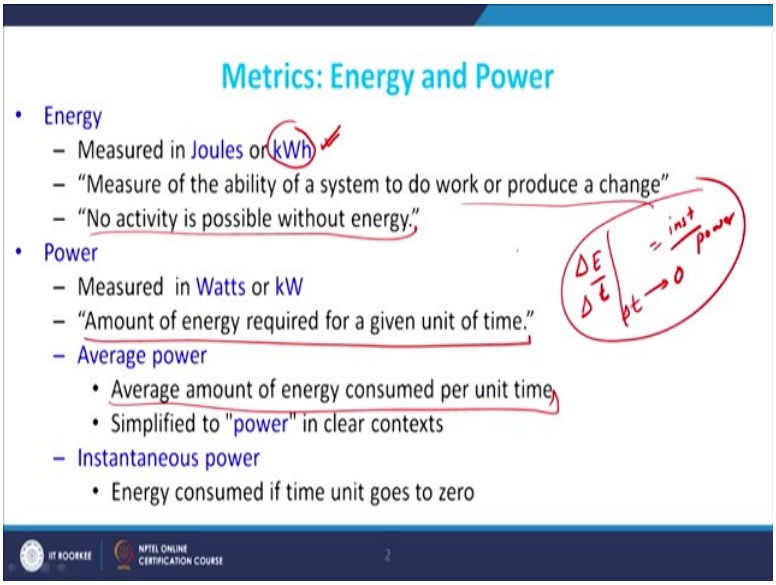

Generally you must be aware of the fact that energies are always represented in form of Joule or also referred to as kilowatt hour, right and it is also defined as the measure of the ability of a system to do work or produce a change so therefore, no activity is possible without energy,

right? So that is the reason why we always talk about energy in terms of whenever we have an electronic circuit coming into picture because without energy you will not be able to do any computation you will not be able to do any logical operation.

If that energy per unit time is basically power, so energy by time is basically my power and that is what is written. An amount of energy required for a given unit of time is basically referred to as power. So it might be true that I might be doing a very small amount of spending small amount of energy over a period of time, but if my time domain is very small I could have I could spend large power in a small interval of time, right so that is pretty important.

When we say average power it primarily means that the average amount of energy consumed per unit time. So let us suppose you were consuming 5 kilowatt during the first hour, 3 kilowatt in the second hour, then 5 plus 3, 8 by 2 will be for a 4 kilowatt will be the average power. So average power is therefore, defined as a power where you take the average in the time domain, right?

So 2 things take away here from the slide, energy is primarily the ability to do work or if you want to do some work you have to have energy with you and what is power energy per unit time is defined as power, you might have a high power and low energy as well, right, because power is energy by time so if your time domain is pretty small and your time domain is relatively small by energy spending is large you might get a large power.

We have also defined the average power concept here, we now therefore, define also an important term known as instantaneous power. Instantaneous power primarily means that when this t tends to zero, right, so ∂E ∂t is my power and when ∂t tends to zero we define this to be as an instantaneous power which means that when we are calculating power and this power we are just transient at a particular time t, we define that to be as an instantaneous power, right, okay. So we have 2 types of power instantaneous power and average power.

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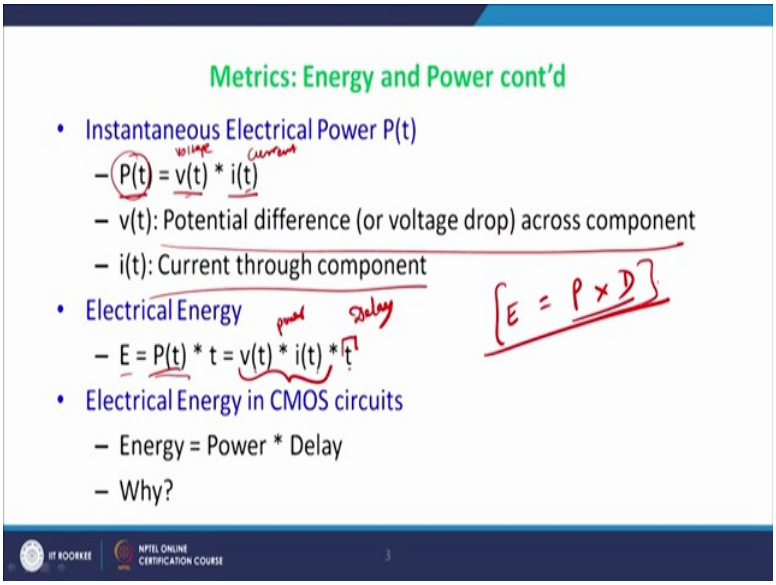

As I discussed with you therefore instantaneous power when you want to find out P of t is exactly equals to v of t and i of t, so well voltage v of t is the voltage and i of t is the current which you see this is the current so voltage into current which is a function of time t will give you the power here so v(t) is basically the potential difference across the component, function of time t and i (t) is the current component.

So electrical energy will therefore will be electrical energy will therefore will be power per unit time power into time, sorry, so power into time will be there so v into i into t will be the value of electrical energy, right. I am not going into the details of this one I think these are pretty simple basic concepts even taught in class 12th sort of a mechanism or even in your school days you have taught all these things.

All right, we define a new term also and therefore, if you see very clearly you have a component this of power, right, and this is primarily your time t across which the power is being spent also referred to as a delay. So energy will also refer to as power into delay, right and that is why it is known as a power delay product, energy is also referred to as a power delay product, right.

And this has been used for quite a long time to find out the power delay product in terms of energy, so if you multiply the power multiplied by the delay in the signal going from primary input to the primary output and if the power dissipation is P then we can find out the energy is to be equals to P into D, right and that is what standard mechanism of power and energy is all about.

Therefore in all practical examples you will see that you have V_{DD} rail and you have a ground rail passing through the chip. Now, whenever you accept power, you accept the power from the V_{DD} rail, V_{DD} rail is the rail where you are giving the voltage a DC voltage or an AC voltage you are giving and from this DC voltage you are dragging power and feeding it into various active components of the device, right?

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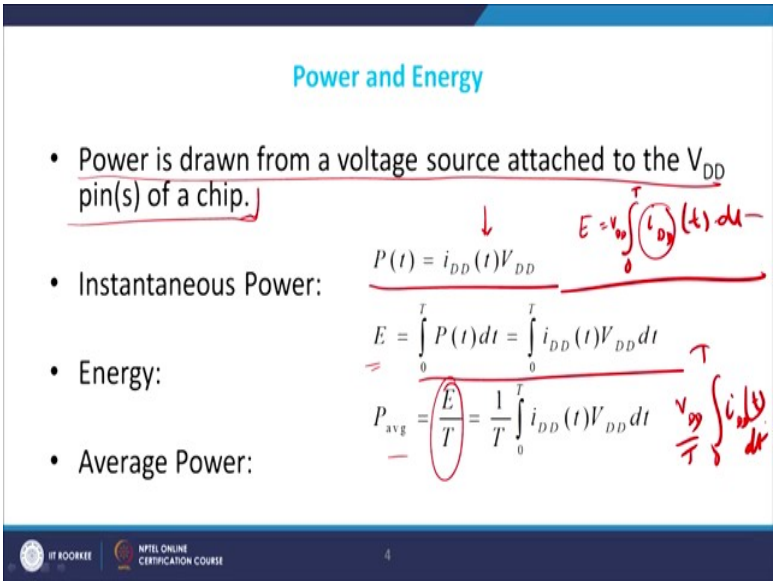

So what I am trying to tell you therefore, is that power is drawn from a voltage source attached to V_{DD} pin of the chip, so I have a V_{DD} pin, it connects to the voltage source and I am able to therefore, have a power being drawn from the voltage source at this point, we have just now discussed that the instantaneous power P (t) is equals to i (t) into V_{DD}, V_{DD} is a DC bias so it will not be a function of time t, right.

We define energy therefore, is equal to 0 to t, integral 0 to t P(t) dt and therefore, I can safely write down P (t) dt as i_{DD} (t) V_{DD} dt, so again you can also say that since V_{DD} is constant you can bring it outside and therefore, I can say write down energy to be equals to integral 0 to t V_{DD}, right into i_{DD} (t) dt, right. Now since current is a function of your time t you will always have energy integrated from zero to time capital time T where capital time T is the time period across which we are measuring the energy.

Average power as I discussed with you is energy per unit time and therefore, if we divide this expression by t, I get this thing so I get V_{DD} by t V_{DD} by t integral of 0 to t i_{DD} (t) dt. So we will see later on that this drain current or the i_{DD} current is not a constant current, but it is a function of many other factors. Like for example whether the transistors are in saturation,

whether they are in active mode or they are in the non-saturated state, are they working as a voltage variable resistor, depending upon that the value of i_d will be changing, so i_d will be either linear, it will be either nonlinear, or it will be saturated and we should be very careful about that particular point that where we are talking about in terms of power.

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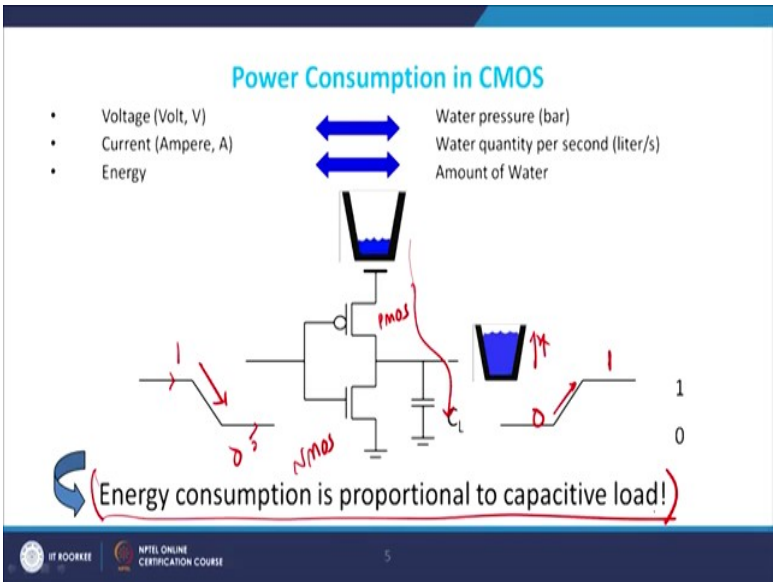

Now let me see what is the power consumption let us suppose that this is a MOS device this is PMOS, right and this is your NMOS here right and your input goes from 1 to 0, right, so when it was initially 1 this was on and therefore, C_L had discharged and now what you are doing you are giving a 1 to 0 transition. So once you give a 1 to 0 transition, right, then what you see a very interestingly that the voltage here falls across this path, this path and charges my capacitor C_L and therefore, the water here rises and therefore, you have a 0 to 1 transition taking place here, right. So I have a 1 to 0 transition and it goes from 0 to 1, fine and this gives you an idea about how fast or slow your design is, right.

So when you are doing it you are actually drawing power or you are consuming power from the V_{DD} rail right because charges has been drawn from the V_{DD} rail and you are able to therefore, have this power available to you. As you can see therefore energy consumption is proportional to the capacitive load, why? Because higher the value of your capacitive load, more charge it can store and therefore, more charge can be drawn from the V_{DD} rail right and therefore, you will be consuming larger amount of power from the V_{DD} rail right and that is the reason that energy consumption is proportional to capacitive load.

So if you want to reduce your energy reduce your capacitive load, once you do that you require less amount of charge and less amount of charge will be therefore discharge from the V_{DD} rail and you will have a lower energy profile available with you, but otherwise it will remain so in a larger state.

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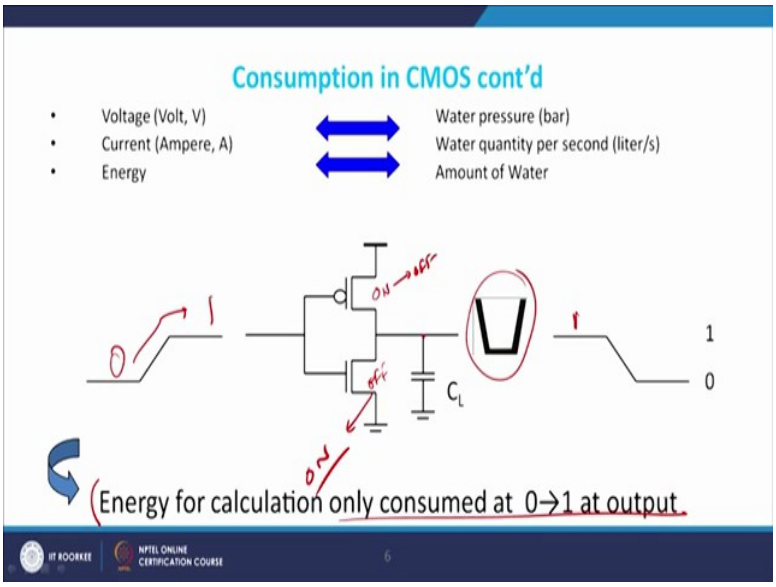

Then let us see what happens when your input goes from zero to 1, so I have initially zero and then it goes to 1, so initially zero means this is ON state this is ON right, and this is OFF, right and therefore, this whole C_L is filled with water which means that this C_L is actually 1, voltage across the C_L is actually equal to V_{DD} and now I go from zero to 1 which primarily means that this goes from ON to OFF state and this OFF it goes to OFF to ON state.

As it goes to ON state I will explain to you, now you see now this discharging takes place to the ground, right, why this discharging? Because now you have a low impedance path with you in the input side, right and therefore, you will always have this output available to you, right. And therefore, you see the CMOS inverter your CMOS design, one very critical aspect is that your output node is typically not a floating node, it is either connected to V_{DD} or it either connected to ground, right.

And that is quite an important observation at this point of time we are not going into further details of it and we see that it is there.

So now energy for calculation only consumed at 0 to 1 transition when the output was 0 to 1 transition that was the only point when you consumed energy, when the output is going from

1 to 0 you are actually dissipating energy and you are able to dissipate energy to the environment or to the heat sink whatever you name it.

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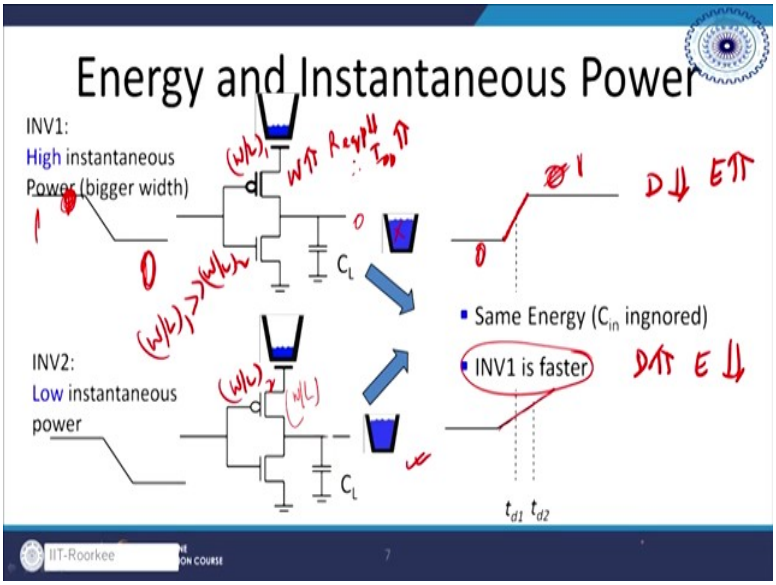

Now the idea therefore is let us see what the idea is, the concept is that, let us suppose your PMOS width was PMOS width was very large, right, so if the width is very large I will expect to get a smaller resistance, so R on or R equivalent P will be small and therefore i_{dd} will be relatively large and as a result what will happen is that if you look very carefully that is what is happening, when input is going from 0 to 1, the output is going from 1 to 0, right, I will just show it to you, or it go to 1 to 0.

But the rate at which it goes from 1 to 0 is very fast, sorry 0 to 1 I am sorry 0 to 1 to 0 to 1, so this is going from 1 to 0, this is going from 1 to 0 and therefore, output will be 0 to 1, right. Now, 0 to 1 means basically that if you look very carefully look at the first figure here, look at the first figure here, so it was initially unfilled which means it was initially 0, now you start giving your voltage, this starts to fill up means the voltage is rising and the voltage is rising like this, after that it remains constant here.

Same concept applies here also, but only thing is that here W by L ratio for the PMOS is smaller, so this has got a bigger width W by L is larger and this is W by L is smaller, right, so W by L 1, let us suppose 2, so W by L 1 is much larger as compared to W by L 2. Primarily meaning that you allow larger currents to flow and charge your C_L therefore, the rate of charging is smaller and you are able to achieve 1 very fast, right, but when your W by L ratio is small you allow a larger amount of time to move and therefore, inverter 1 is faster so the

inverter 1 is faster, so why it is faster? Because I am able to do a large amount of transfer within a short period of time, which means that, that since the delay is lower now I would expect to see the energy to be high and that is true also because for a smaller duration of time you are sending a large amount of charge, so the energy is large.

So what happens is that the delay though is reducing, but the energy is basically typically very large in this case, whereas in this case delay is large right and therefore, energy is reduced in the second case, second case W by L ratios are very small for the pull-up device in this case PMOS devices.

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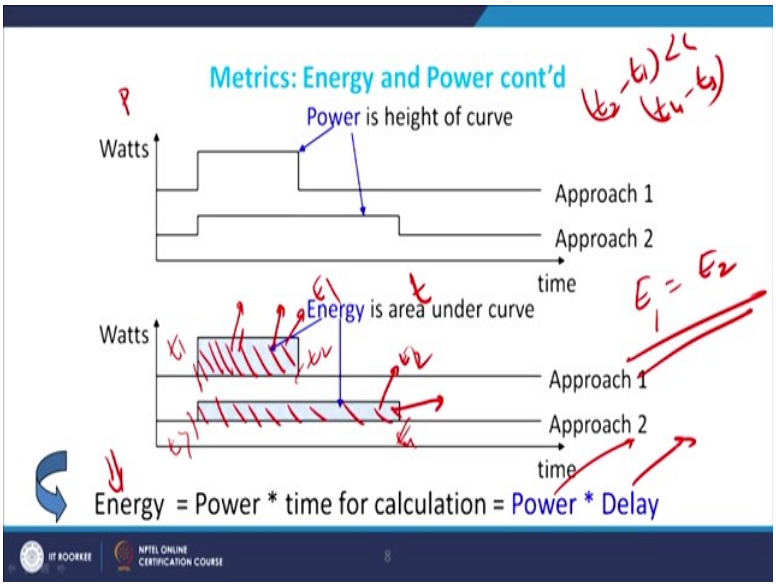

Now therefore, there are 2 approaches which is available with us, now if you look at the approach this is power versus time, right, the area under the graph is basically your energy P because P into t is basically your energy, right so this is E_1 and it is E_2, both see if we look at in that way both E_1 equals to E_2, it primarily meaning that the energy consumed by both the transistors please understand, both the first transistor and the second transistor is large, but the first transistor does this energy at a shorter duration of time, whereas the second one it does it larger duration of time t and this is a larger duration of time it is doing it and this is doing it a shorter duration of time, right.

As a result so energy is the area under the curve, right, so energy is same, energy is same because the area is same, but then you are dissipating more amount of power here in the first case the reason being you are doing it in a smaller time domain, so this is t_1, t_2, right and this

is t_3 and t_4 . Now if I subtract t_2 - t_1 it is much smaller as compared to t_4 - t_3, as a result this energy E_1 so the power is much larger as compared to the second power.

Okay, so we write down therefore, power into delay equals to energy, so energy is equals to power into delay, right, so this is this is what a standard mechanism which we follow.

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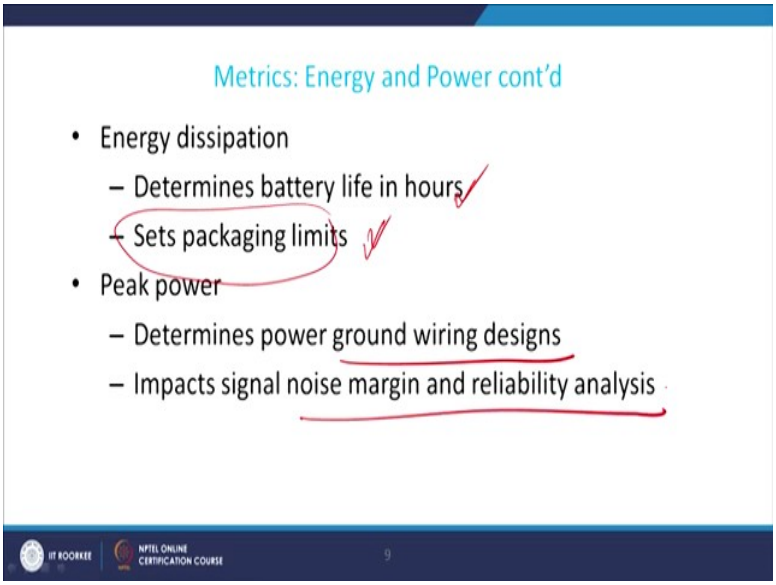

Now, let me therefore come to the matrix the problem of energy dissipation is that the battery life will be in hours rather than minutes if I reduce the power if I reduce the power dissipation and it sets the packaging limit, why packaging limit? The reason being if it is highly dissipative in nature you should have proper sinks, heat sinks in the packaging so that you are not able to let the heat or the power dissipate within the chip, but outside the chip, right, so your packaging limits are set in that, right.

Peak power is defined as the power which is peaking at any particular time t and therefore, depends upon the wiring design, as well as a noise margin and reliability analysis so we will not go into details of this 1, but primarily therefore, we if you look very carefully I can have therefore, 2 energy which are equal, but in 1 case the power will be higher and in other case the power will be lower, right that is what we know as basic concept which you see here.

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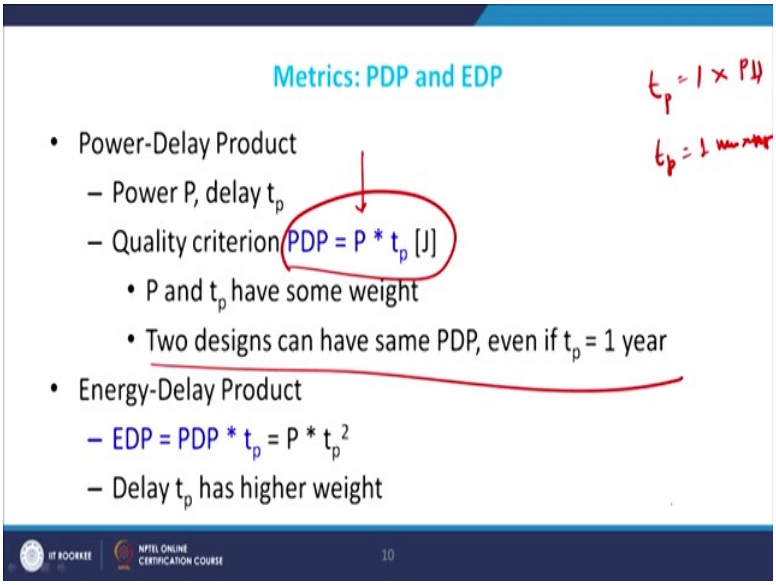

So therefore, the quality criteria power delay product as we discussed was an energy PDP was equal to $P^* t_p$, p is the power dissipated multiplied by t_p which is the propagation delay, right. So you see 2 designs can have the same PDP even if t_p is 1 year, I hope you understand. For example in 1 case the t_p is 1 year and another case t_p is basically say 1 month or whatever small value, then for the same PDP this will have a lower power, whereas this will have a much higher power, right.

So if you if you are able to achieve a functionality within a small duration of time, you end up having a larger energy or larger power, whereas if you do the same computation for a larger period of time you are spending less amount of power. So power depends not only on the total energy, but also on the time domain analysis of each 1 of them right, and that is quite an interesting one.

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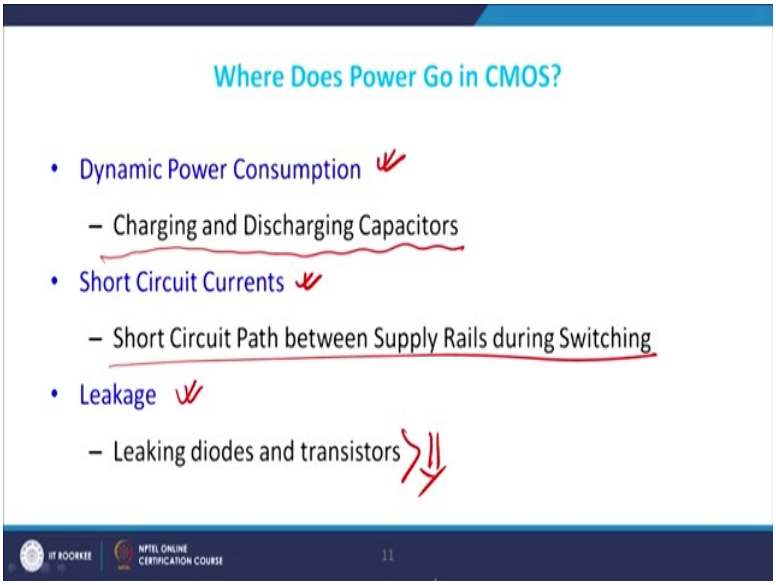

So where does the power go in a CMOS? That is pretty intriguing question and people have been asking this question for a long time and there is a straight answer available here also. We have 3 types of power consumptions, we have got dynamic power consumption we have short-circuit power consumption sorry short-circuit and leakage, so you have dynamic power, we have short-circuit and we have leakage.

So dynamic as the name suggests it is basically not fixed, but goes on changing with respect to time which means that charging and discharging of the capacitor of the design is defined as the dynamic power consumption. So faster the charging discharging more will be the power available with you or more will the power dissipated for you. Then of course as I discussed with you in a previous term, you will have a short-circuit power between supply rail and ground during switching and there will be also some leakage current which is primarily your reverse leakage current, also due to Zener leakage current and so on and so forth and the transistors will show you a drop here.

So these are some of the problem areas which you will face, the last 2 and the major contribution which the this will give you is basically I will have a larger dynamic participation or a smaller dynamic power dissipation, I will have a larger or a smaller short-circuit power dissipation and we also have a smaller leakage which is basically a sub-threshold leakage with us and this is what we get from here.

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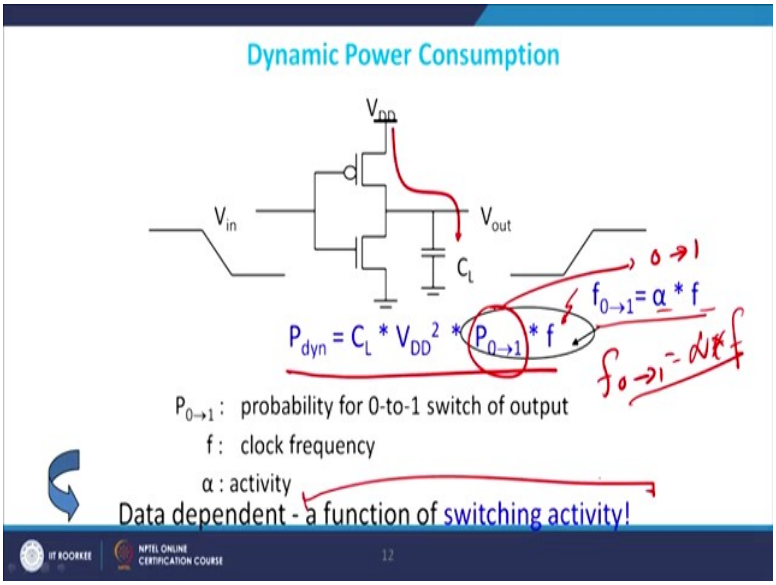

Now let me come to the again the basic dynamics or the basic equations of dynamic power dissipation and if you remember correctly half C_LV_{DD} square you are taking from the V_{DD} rail and then you are pushing the half C_LV_{DD} square into the ground, right. And therefore, for a 1 cycle you are actually taking half plus half which is actually exactly equals to C_LV_{DD} square and that is the reason you get C_LV_{DD} square as the dynamic power, initial dynamic power.

Then what you do is you multiply this with P 0 to 1, P 0 to 1 is the probability that you get 0 to 1 switching done in the circuitry, easier said than done because you do not have any control over the circuitry and the second thing is that if you do a 0 to 1 transition you will automatically have almost half the maximum frequency of operation and that is the reason the probability for 0 to 1 switch of output is kept at the last point, f is the clock frequency and α is the activity, we had already discussed the activity concept in the previous turn.

So for example, if you have a clock, the clock will have a surely an activity and that therefore, will have our activity equals to 1, if you do not have a clock, but you have some complex logic gate maybe your α will be 0.75 and so on and so forth. So on 2 factors primarily a dynamic power depends and that is known as the frequency of operation as well as on the probability that the output will go from 0 to 1, fine, that is what is dynamic power dissipation is all about.

Now let me come to therefore, as I was discussing with you, you get 0 to 1 and this f of 0 to 1 is defined as α into f, please understand that f of 0 to 1 is basically the meaning of

functionality from zero to 1 is defined as α multiplied by f, α is the activity vector and f is the frequency of operation of the device and f is the clock frequency.

Let us look at the dynamic power dissipation as I discuss with you ($C_L V_{DD}$ square)* the probability that you are going from zero to 1, since so zero to 1 multiplied by f, where f is the frequency of operation of the device. As I discussed with you data depended, why is it data dependent? And it is a function of switching activity, why? The reason is it is data… but data dependent in the sense that if your both inputs are 1 1 and you have a NAND gate also, logic is also there, then your pull down network will be fully activated and your output will be very strong 1 to 0 transition.

So which means that it is very difficult for you to go from 0 to 1 transition and the reason being that if your data depends on the functionality of the switching circuit activity which means that how the input, how the output goes high or low will depend upon whether the device is switched ON or OFF, right and that is the problem area of the data being inserted here.

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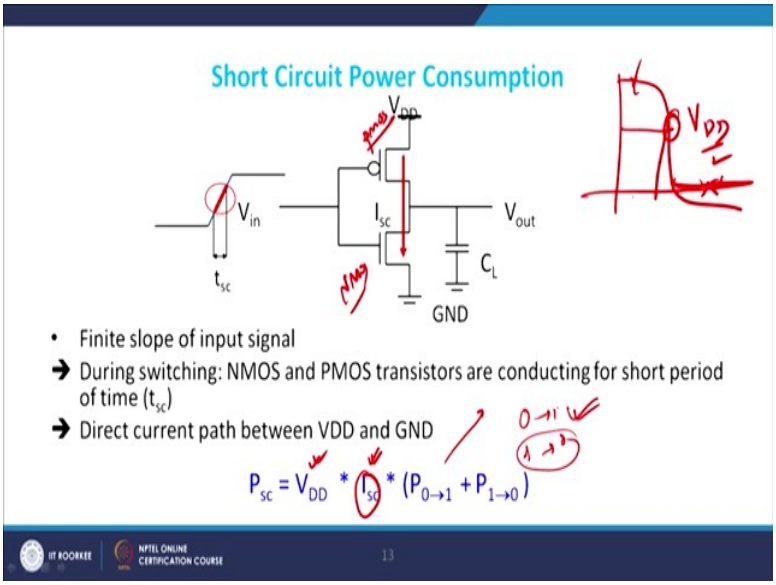

Let me come to the next part that is the short circuit power dissipation or consumption, we have just now discussed with you the dynamic power which primarily depends upon the frequency of operation and the capacitive charge, we not depend short circuit, we have already discussed this point earlier also, but I will dealt in slightly more detail.

If you remember we were discussing that the during the ON state when your device was ON, we define the device to be in the ON state and we also say that the output will be switched

OFF because typical inverter characteristics we discussed yesterday, right something like this. So when your input is low output is high, if input is high output is low, the input is high output is low.

Now if you are biasing a device here or here you will have a problem and the problem is that you will… though you will have no current flow through it, but there will be a loss in the voltage value. Somewhere here in the middle where you have switching thresholds available approximately equals to V_{DD} by 2, then your NMOS and PMOS, this is your PMOS and this is NMOS, these 2 are equally ON, getting my point? Which means that both are equally ON which primarily means that both the transistors will be able to pull the charge carriers from the peripheral onto the capacity load, fine, is it okay?

So that is the reason the short-circuit power dissipation is very very low in case of in case of a simple CMOS inverter right, and this is what is an interesting idea. Now as I discussed with you there is a direct path between V_{DD} and ground, so I write V_{DD} into I_{SC}, I_{SC} is the short-circuit current multiplied by P 0 1, P 0 1 is the probability that the output goes from 0 to 1 and then you have a probability the output goes from 1 to 0.

So we are actually not interested in this domain, we are either interested in this domain which means to say is that given a complex logic gate can you find the probability that the output goes from 0 to 1, so there is a, we will do it as we move along, but that is what it is all about here, so short circuit depends upon all these values.

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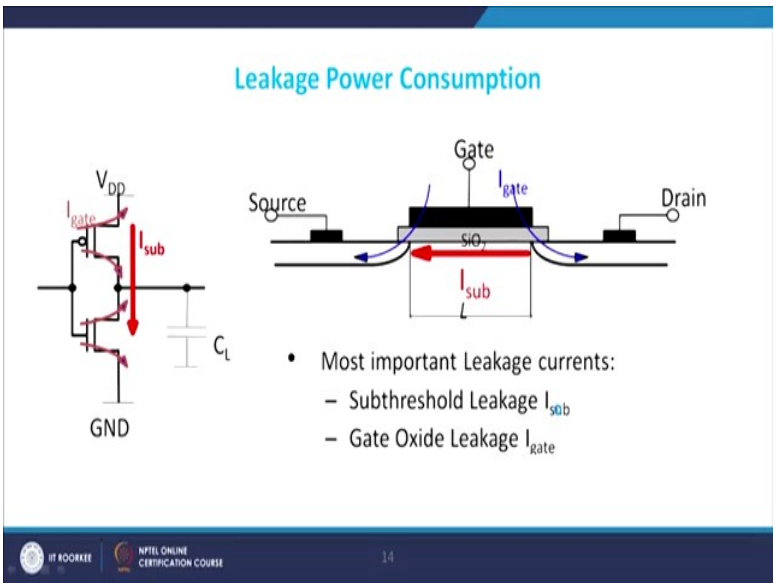

Let me come to therefore, the leakage, so I had saturation in which the gate voltage was very large or very small and therefore, the output will be either switched ON or switched OFF. The second issue which came up was that of the static power dissipation or yes the short-circuit power dissipation, when both the devices are equally ON you will have a direct path between the 2 end up with last leakage power which is of sub threshold leakage.

So when your gate voltage is just smaller than the threshold voltage device there will be large carrier movement which will be available which will result in the sub threshold leakage, we will not go further than this, but P peak equals to I peak into V_{DD}, now I peak can be written as I_{sub} plus I get multiplied by V_{DD}, so this is what an important this thing we get.

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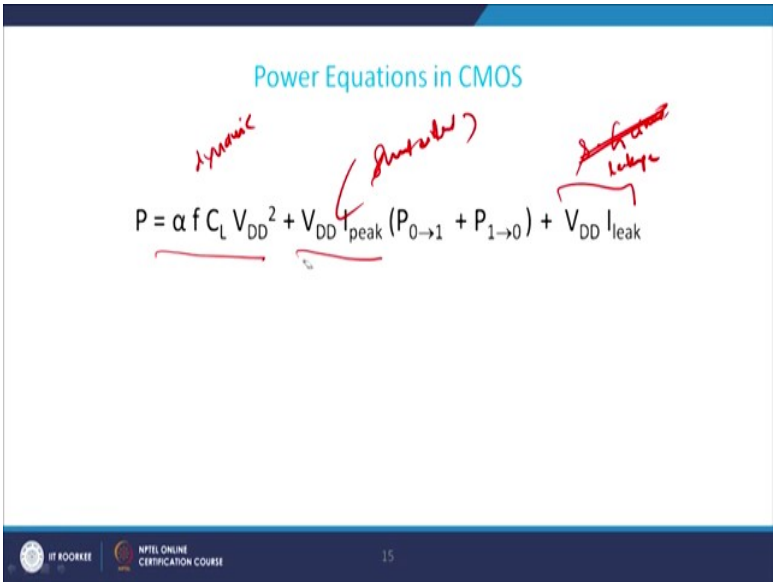

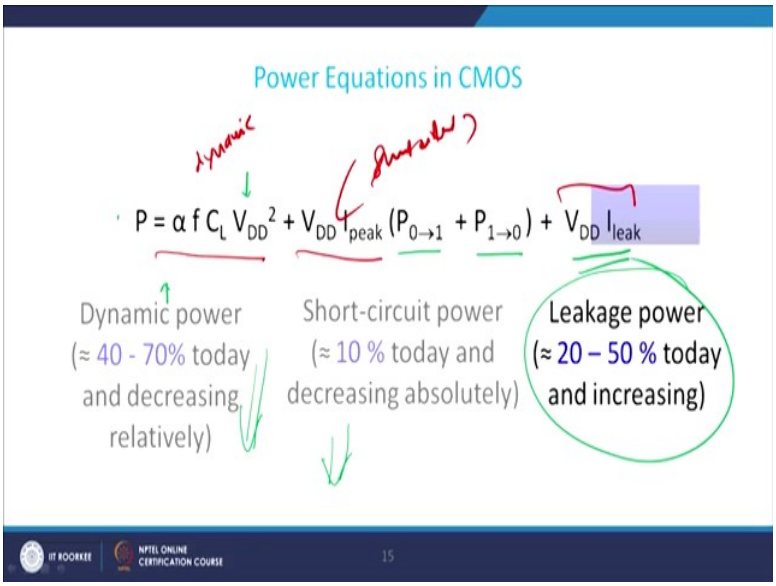

Next we get the power equation, the power equation as I discussed with you C_L f times V_{DD} square is your dynamic power dissipation, we have V_{DD} times I peak as the so this is basically your, so this is a dynamic, this is your short-circuit, short-circuit power dissipation, this is your not short circuit, this is a short circuit, short circuit, circuit power dissipation and this is basically your power dissipation by virtue of leaking so I have a leakage available with me.

Now if you see carefully in with all these discussions or all these ideas you will you will appreciate that if you look carefully it tells me that the total power dissipation can be broken down into 3 parts and those 3 parts are mentioned in this region that some of them will be in, so what I tell you is that if you have some voltage variations your V_{DD} will change and your P will change.

Similarly, if your probability of 0 to 1 and 1 to 0 if it happens you will obviously get added up with the total probability and that is the reason you will get a higher energy. Similarly, V_{DD} into I leak will also give you a higher power. Now a dynamic power is approximately 40 to 70 percent of the total power and it is decreasing yearly and that is sort of a good thing for us.

The second is short-circuit power is relatively small is approximately 10 percent of the total -,,,,,,,, to total charge available and this is decreasing, so this is decreasing, this is also decreasing, what is increasing is basically my leakage power because of the reduced dimension you do have a larger chance of the charge carriers being leaking and that is the reason it is leaking by 20 to 50 percent, then here where people are actually concentrating large for optimizing power.

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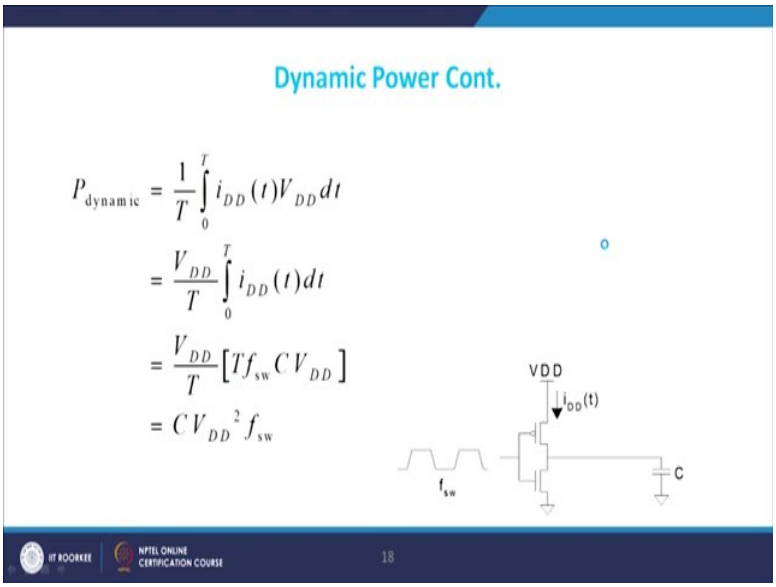

As I discussed with you dynamic powering, I will not go into further details of it, but I will give you a brief idea about dynamic power dissipation, it is actually V_{DD} by T f SW t times f SW is basically the frequency operation or number of times the output change before time t and this is what is known as this thing. We came to dynamic power dissipation given by CV_{DD} square times f of SW, f of SW is the frequency of your short way, the frequency of your wave.

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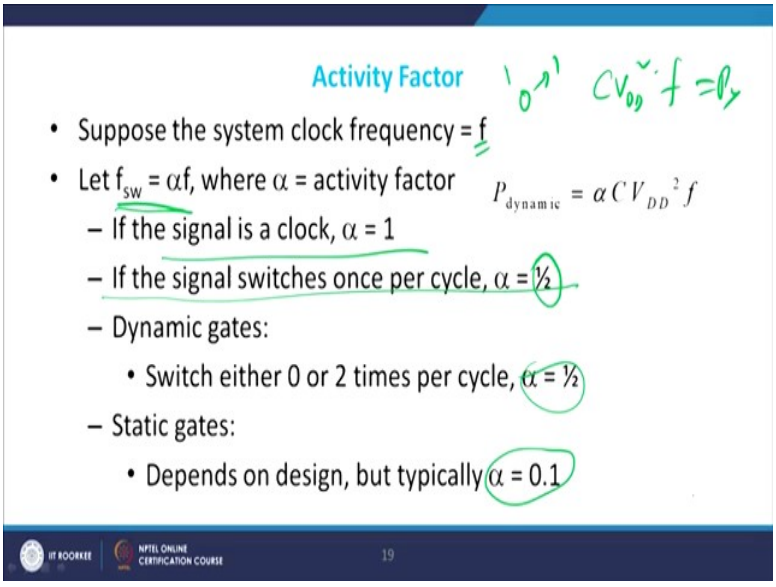

Now suppose a system has system clock of f, then f_{SW} is let us suppose α into f, but α is the activity factor. Now if signal is a clock as I discussed with you, α will be equals to 1 and therefore, I will get CV_{DD} square multiplied by f as equals to P dynamic. Similarly, but if the

signal switches once per cycle, so there is a one 0 to 1 transition between the 1 full cycle of this input, we can give you an α equals to 0.5 or 1 by 2.

For static gates typically α will depend upon the value of the static gates it is equals to 0.1 and if you are using a dynamic gate at this point 0.5 or 1 by 2. So we have seen one important point of activity factor is that activity factor depends upon the type of logic level you are deciding, as well as on the structure which you are designing.

Now let me come to the static power, we have already discussed static power, the static power is primarily the power which is dissipated across the board or across the device when you do not give any dynamic power, so which means that when you do not give any V_{DD} at that point of time whenever the device is in the OFF state maybe or just simply OFF you have leakage currents available or you have a sub threshold current available which basically gives you a larger power.

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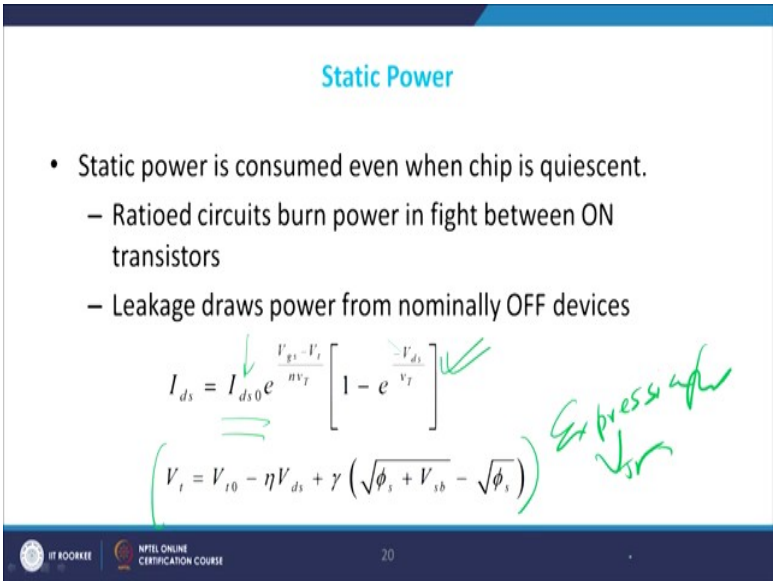

So this is a larger power, I_{ds} equals to I_{ds} 0, I_{ds} 0 at V equals to 0, the amount of current flowing is given as I_{ds} 0 and we get this big equation available here, and I got the equation, but the threshold voltage.

So this is the expression for, expression for threshold voltage and that is quite an interesting result which we get, but if you forget about this 1 the last 1 you will see that with increasing V_{DS} e^{-VDS} will go on decreasing and therefore, 1 minus that will go on increasing and as a result you will get larger ideas value. So mathematically it seems that this should work fine.

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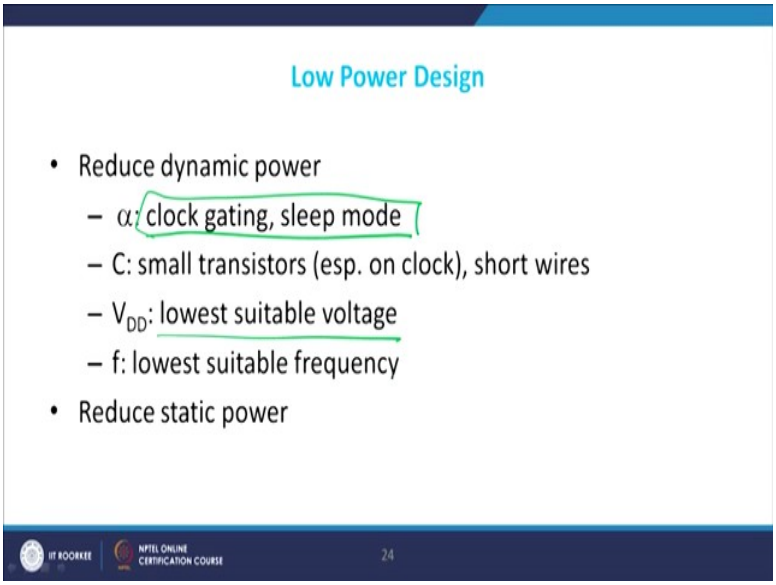

Now, let us see how can you reduce power, that is the most important part which we learned from all these things. The first thing is that reduce your clock gating or do you put it into sleep mode? So when the system is not working either you put it into sleep mode or you put your the devices into clock gating, so once you put through clock gating, it primarily tells me that you can reduce the value of α, C should be small and therefore, you do not have to work with large wires, it should be small in length and that will give you a small transistor based design.

You should also work with this lowest suitable voltage in all sense and the reason being if it is not the power dissipation levels will be will be typically very large and you require the lowest possible frequency. So possible frequency, voltage power and you should actually therefore, rely on small transistors and on short wires and this takes care of our low design concept.

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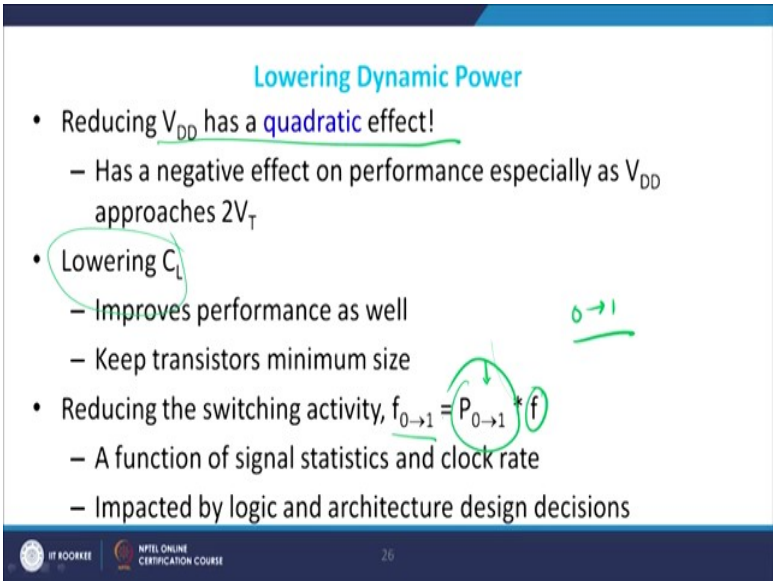

So how do you decide, how do you reduce your dynamic power as I discussed with you α, C capacitance, V_{DD} which is the lowest suitable voltage available to you and α f is the lowest suitable frequency, how do you, so this is that, how do you reduce static power? Selectively ratioed logic selectively use low V_T devices you will have leakage reduction provided you arrive at stack devices, body bias and temperature.

So what you see is that I can reduce static power by using certain changes in the circuits itself making it ratioed logic, whereas if you want to reduce dynamic power or want to reduce the branding power to a bare minimum I need to concentrate primarily on for the purpose of reduction on the dynamic part of it. Now if you look carefully how do I lower my dynamic effect?

So since V_{DD} has a quadratic influence so therefore, even if you double your V_{SS} which is doubling a power supply that will lower your power dissipation by 1/4th and that is quite an interesting phenomena people have observed. Okay, so lowering a C_L, lowering C_L of course will be meaning that you will be able to improve your performance because when a capacitive load reduces, you achieve a much better performance with you.

Now reducing the switching activity, switching activity is again defined as the probability of 0 to 1 multiplied by frequency of operation, right. So this is the probability that you have got 0 to 1, the 0 to 1 transitions are power consuming transitions and that multiplied by f will give you the frequency of 0 to 1 transition in this case.

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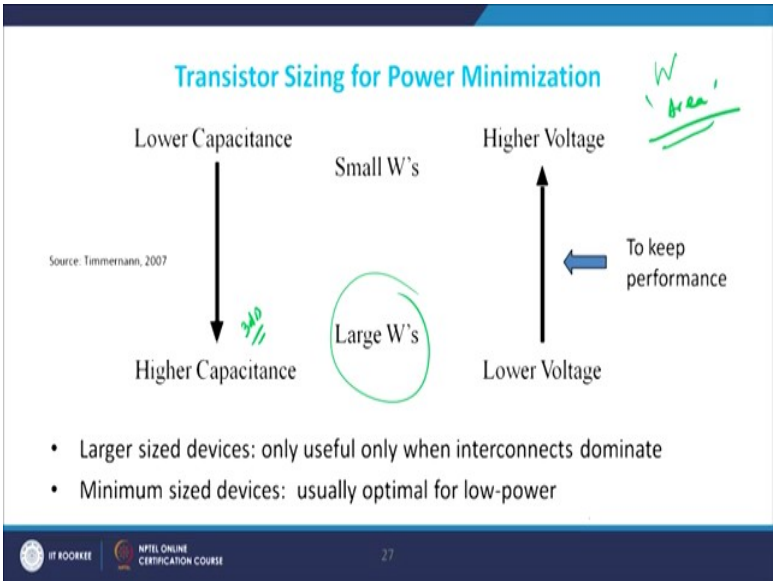

Now, let me come to the transistor sizing concepts, so if you have a small W which means the width is small, I would expect to see, I would expect to see of course the lower capacitance because small W primarily means that the area under the this thing gate is very small and therefore, you require a lower capacitance. Whereas if you make your capacitance higher and higher I obviously at larger W, I get a higher capacitance and therefore, this restricts my 3 dB bandwidth and so on and so forth.

What happens if you want to work at higher voltages? And the reason is that sometimes my requirement is not high speed by high performance which means that I cannot sacrifice on the performance and therefore, what I do? I increase the value of V_{DD}, once I increase the value of V_{DD}, I make it larger the performance increases at the same instant of time the power dissipation also becomes large.

So this is a methodology which people use that they try to do what is known as an adaptive scaling in terms of this thing in terms of both V_{SS} and in terms of other devices as well.

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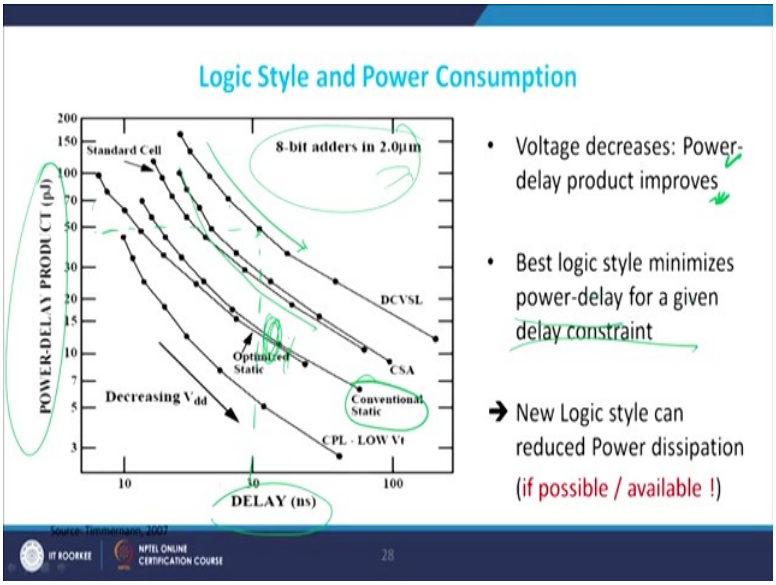

So I will not go into details of this 1, but just give you an idea if you look at this graph it is between the PDP power delay product versus the delay, right. So if you see that the delay increases the PDP also goes on increasing for all that design, which means that you did not contribute to the design beyond a particular time limit and therefore, you see it is actually getting reduced drastically.

For the conventional static CMOS this is the equation of the graph of power design failure and for non-standard 1s these are the case of the design available with you. So this gives you a best logic style for input-output combination and gives you an idea about how this works for, so this is this example is for an 8-bit adder, so I had used an 8-bit adder in a 2 micron CMOS technology and I got this these are the outputs so these dots are basically your output available to you for the PDP versus delay so when your delay is 30, or whatever 30 microsecond or nanosecond, I will see this to be equals to approximately 50 PDP of pico joules, as you make your delay large, this PDP will fall down and that is 1 of the major areas or advantages of this system. As you can see therefore, as the voltage decreases the power delay product improves. Now the best logic style minimizes power delay product for a given delay constraints, this is the example, okay. You can achieve a new logic style and reduce the power, but that is the way beyond the scope of this work. So we have learned 2 things, we have learned in this chapter that we had learned power dissipation, as well as the concept of delay and what is the meaning of PDP and EDP. With these word let me finish off today's lecture and when we meet next time we will do something else regarding the logic design, okay thank you very much!!!