Microelectronics: Devices to Circuits
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Lecture 18 - CMOS Inverter Basics - I

Hello everybody, and welcome again to the NPTEL online certification course in Microelectronics: Devices and Circuits. We will start with today's lecture on CMOS Inverter Basics Part 1, so that will be the lecture module which is supposed to be delivered now, the CMOS Inverter Basics 1. In our previous interactions we have understood the basic principle or a functioning of a MOSFET, MOSFET is the current source and MOSFET is a switch. We also understood the basic concept of threshold voltage, which means that the gate voltage above which for an N channel depletion in enhanced mode MOSFET, the device is in the on state and below which it goes to the off state.

We have also understood the region of operation of the MOS device in saturation as well as in the cut-off region and we have therefore also appreciated on the second-order effects which are available in MOSFETs which come out because of certain, under certain conditions of structural or electrical inputs. What we will be doing is we will be stepping off from a device perspective to the circuit prospectives and we will start with today's lecture on CMOS which is CMOS technology, also known as complementary metal oxide semiconductor technology right, so it is basically C stands for complementary, complementary metal oxide. We will see why it is known as complementary as we move along.

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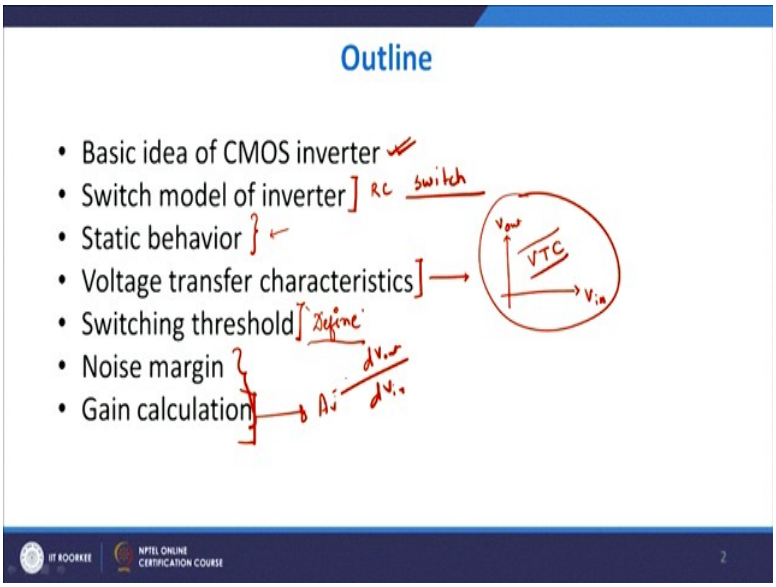

So let us just give you the basic outline which we are supposed to deal with it within this interaction. The first thing is basically the basic idea of a CMOS inverter right, so we will see what is the meaning of an inverter because this is the basic building block for any digital or even analog VLSI design. So for any of the chip or any of the circuit which you want to design the prime notification or the prime building block is basically a CMOS inverter, so we will understand what is the basic idea of CMOS inverter, how it looks like, how it functions.

We will look into the switch model of inverter also known as RC switch model, so we will be taking these resistances, so this MOS devices as resistances, how these MOS devices tend to store a charge in the capacitance. X is a current source and then in a cut-off, X is open circuit and therefore we will be looking at the static behaviour of the device, which means that static behaviour primary means that you give a DC bias to the gate side of the MOS transistor and then see how does a current flow in the output of a MOS transistor, that is known as static right. Whereas dynamic behaviour, you see behaviour is when you start giving a voltage and you vary the voltage from low to high value and that is known as dynamic behaviour.

We will also look at voltage transfer characteristics, voltage transfer characteristics is basically the transfer or the profile between V_{out} and V_{in}, so if I vary V_{in}, how does my V_{out} vary in a CMOS inverter is defined as a voltage transfer characteristics right and it gives us any idea about how switching or how is the MOSFET is getting switched from on to off and off to on and how is it helping me to charge and discharge a battery or external capacitor in the output volt.

With this when we have understood what is a VTC and we have seen how VTC works, we will be actually coming to what is known as a switching threshold. We will define switching threshold with perspective to digital logic as well as to analog logic and see what is the meaning of threshold and what factors switching threshold depend.

Finally, we will be ending with noise margin and gain calculation. And noise margin primarily, basically we will understand that how much amount of noise can be inserted onto CMOS inverter without flipping of the data. So if 1 is there, it is still read as 1, so let me see how much amount on noise can I introduce into it, and that much amount of noise and inverter will easily reject and the data will not be corrupted. So we will be actually looking at noise margins of the inverter and then finally, from analog perspective or view we will be actually doing a gain calculation, which means that we will try to find out ∂V out right, ∂V in, that is what we find out A_V. So ∂V out, ∂V in we will try to find out and this is basically your voltage gain which we will be seeing as we move along.

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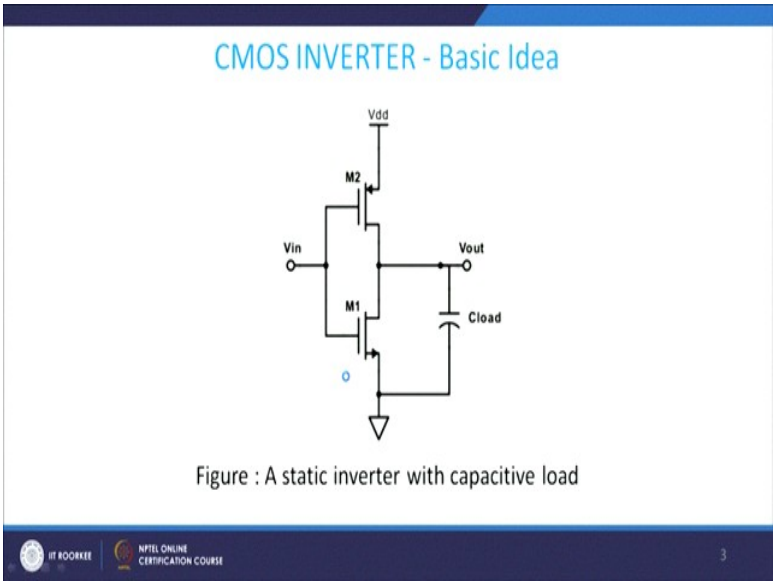

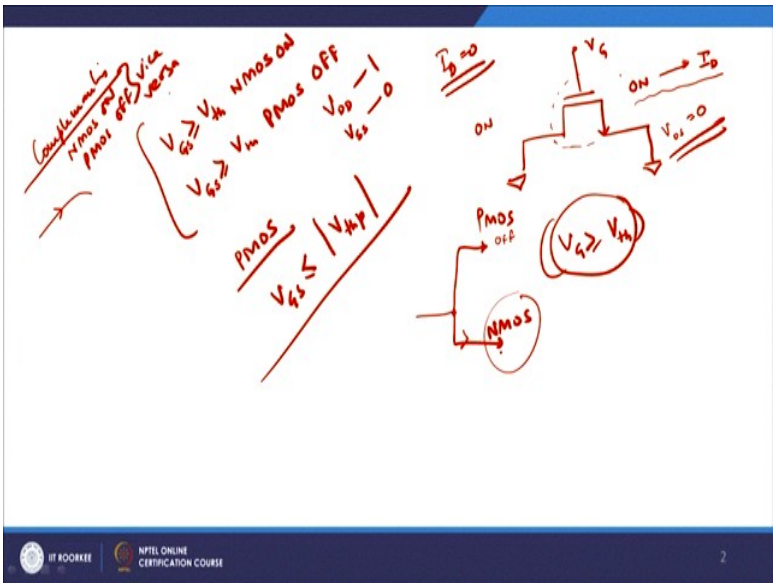

So this is the outline or the basic outline of the talk and let me come therefore to a CMOS, basic CMOS inverter. Before we go to basic CMOS let me give you the brief idea of what we have done earlier so that it becomes easier if you do appreciate this point, if you remember in my NMOS transistor, if I had a gate voltage with me V_G, if my source was grounded and even if your drain is grounded, then V_G should be greater than equals to V_{TH} of this device, for this device to be on. It primarily means that for the device to be in the inverted state or in the on state my V_G should be greater than or equal to threshold voltage of the device.

In that case only my device will be in on state, but in the on state it is not necessarily that there will be an I_D. As you can see since your drain is grounded you do not have any chance of any drain current flowing right and therefore I_D can only happen, provided you have a V_{DS} right. But at this stage V_{DS} equals to 0 and therefore I think I_D equals to 0 and therefore even if I_D is equal to 0, the devices is in the on state.

So whenever, let me recapitulate for a n channel device when V_{GS}, V_G is greater than equals to V_{TH}, NMOS is on right and when let us look at PMOS, whenever V_G is greater than V_{TH} PMOS will be always off, because for PMOS I require that, this condition should be V_{GS} gate to source, a gate to source and for PMOS the condition is that my V_{GS} should be less than equals to $|V_{THP}|$ right, that is very, very important.

So you see for a same input signal right, if my NMOS device is on, and I give the same input to my NMOS, PMOS device and NMOS device, let us suppose this is my PMOS and this is my NMOS and my NMOS is switched on by the virtue of the fact that this gate voltage at this point is larger than threshold voltage of the device, this will automatically ensure that my

PMOS will be off, why? Because PMOS you require a lower threshold voltage or threshold voltage to below in order to switch on the device.

So the primary difference between NMOS and PMOS is the very basic fact that for the same amount of gate voltage given to NMOS and PMOS, if means like in digital logic, if which means that if V_{DD} corresponds to 1 and V_{SS} or V ground corresponds to 0, then when apply V_{DD} to both the gate terminal of NMOS and PMOS, the NMOS is switched on and the PMOS goes to cut-off mode and whenever V_{SS} equals to 0 or my input is equal to V_{SS}, then my PMOS switches on and NMOS switches off.

And hence the name complementary, which means that both NMOS and PMOS will never be on together at, they will be on for a small duration of time, but for most of the voltage range I will always get this to be as a complementary switch, complementary, the complementary right, what is reason of complementary? Because both NMOS when it is on, PMOS is off right and vice versa, this will be vice versa right. So this is very, very important idea, which you should always keep in mind, that you always have a switching of threshold taking place in this manner.

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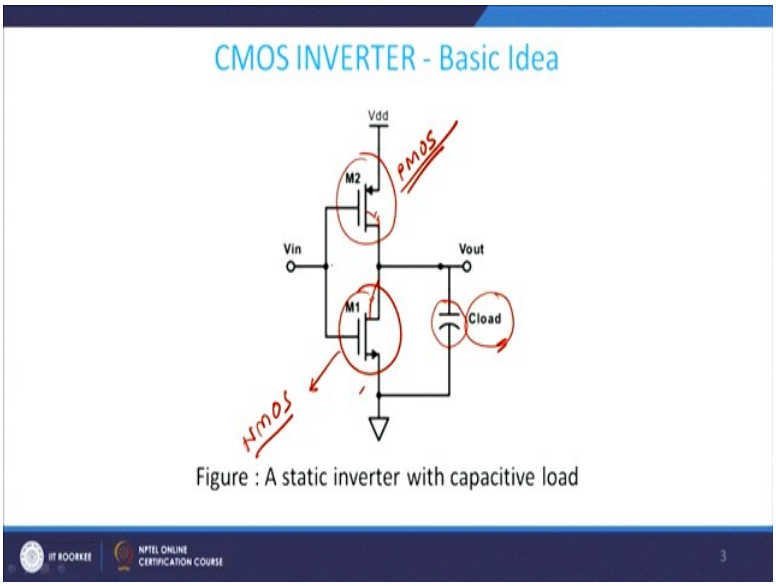

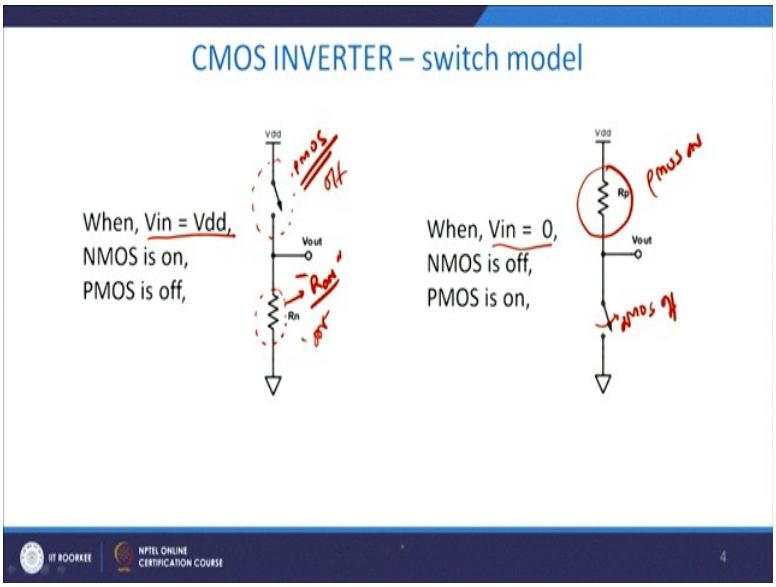

Now to come into that fact as you can see here, this M2 is basically my PMOS, this is my PMOS, this is my PMOS and this is my NMOS, this is my NMOS and this my PMOS which you see here. Now whenever my, we obviously have a load capacitance here, this load capacitance is nothing but the overall capacitance of this part here right or this part between these two points and so on and so forth. So all the capacitances in this PMOS and NMOS if you add together, I get C load available to you, also C load can be the load capacitance which you are putting in the external volt or the load capacitance subsequence stage of the CMOS inverter right, that you plug it and place it here right. So therefore it basically means that the inverter at one point of time will be charging the C load and another point discharging let me see how it works out.

So when V in maybe I just show in the next slide right, now when V in equals to V_{DD} right, when V in equals to V_{DD}, when my input voltage is equals to V_{DD} at that point of time, my NMOS is switched on right, but my PMOS is switched off because my input is high, so as you can see in the switch model, if you look here this my PMOS, PMOS is basically open circuited whereas NMOS is closed circuited with resistance equals to R on right. R on is the transient resistance between source and read of the MOS device, and that is the reason it is complementary, means both are not together on.

Similarly, when V in equals to 0, my PMOS becomes on and therefore I have a resistance offered in this manner and I have my switch model shows me an NMOS to be off, so this NMOS is off, whereas PMOS is on right. In this case, the PMOS is off, and NMOS is on, so that is pretty simple and straightforward way of looking at inverter switch model.

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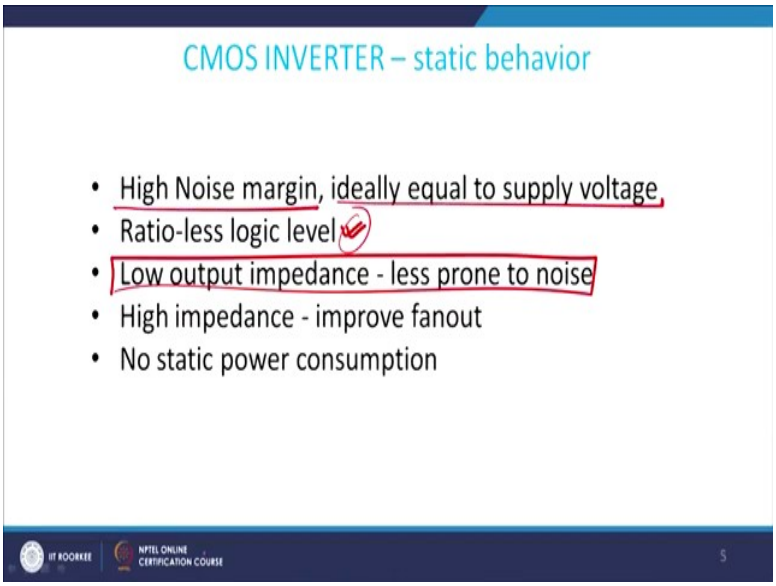

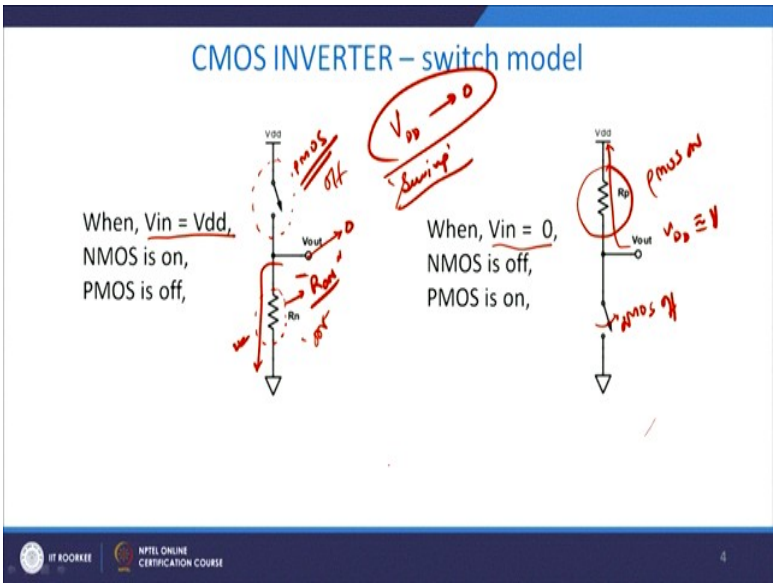

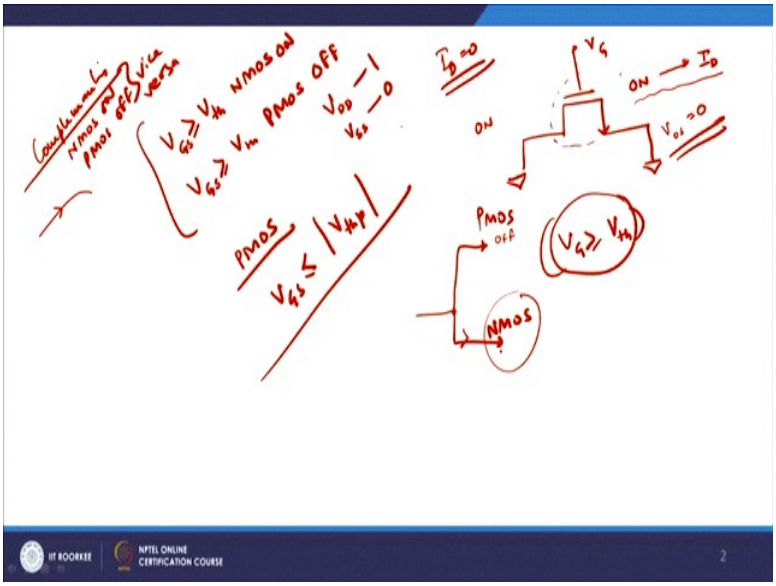

If you therefore come to the basic fact that the idea here is therefore if you, let us go back to the slide, if you look very carefully when your NMOS is switched on right, this V out will have a path and this will be grounded here, so the output voltage will be 0. When my PMOS is on and my NMOS is off, then this will be, voltage will be plugged to V_{DD} and the output will be equals to V_{DD} which is effectively equals to 1volt, which means that this inverter allows you to do a peak to peak swing, peak to peak basically means it is actually swinging from V_{DD} output to 0 output, such a large range it is allowing it to do.

So we have large swings associated with CMOS inverter switch model right and the reason being that you have now large amount of, you allow the voltages or the output to go till V_{DD} when my PMOS is on and go to ground when my NMOS is on right and that is the reason you get such type of circuit and that is the reason you therefore have a very high noise margin

available with you and ideally equal to the supply voltage. So whatever is supply voltage you get noise margin which means that a static CMOS inverter right, since it is able to pull your output voltage to logic one which is equals to V_{DD} right, it is utilising the full support from V_{DD} to ground rail, so the whole range is being utilised by the input level right.

This is also referred to as a ratio-less logic level, which means that independent of the dimensions of these devices, W by L ratio of PMOS or NMOS I am 100 percent sure that the threshold voltage will always remain the same it is, which means that once you have fabricated your PMOS and NMOS and attached it as a CMOS inverter using a twin tub process, you will see that, we will see that your logic is basically a ratio-less logic, which means that, I do not have to change my W by L of my PMOS or NMOS in order to have different sets of behaviour.

So for a same set of behaviour as a switch the same W by L which you are using earlier, you can use it and gives you a very good result here. So if you go back to your previous case, the ratio-less logic is there, which means that it is independent of W by L. Since the output impedance is the low impedance node, it is less prone to noise and this is a very standard way of looking at it, that whenever an output source is connected to high impedance you have less noise immunity. When it is connected to low impedance node the noise immunity is higher and therefore you have less noise at the output node.

The impedance is high, the output impedance, the output the input impedance is high because I am inserting my signal onto the gate side of those devices. Now gate is always terminating through oxide layer or a dielectic layer and as a result, if you look from the gate side the resistance offered by the device to input signals are typically very large right and therefore it is high impedance and therefore improve fanout. There is no static power consumption or even if it is there it is very small static power consumption is there between CMOS right.

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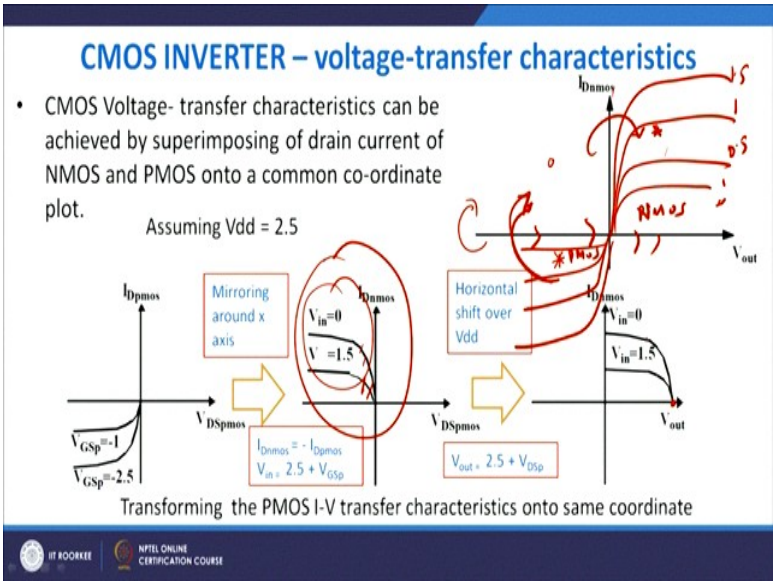

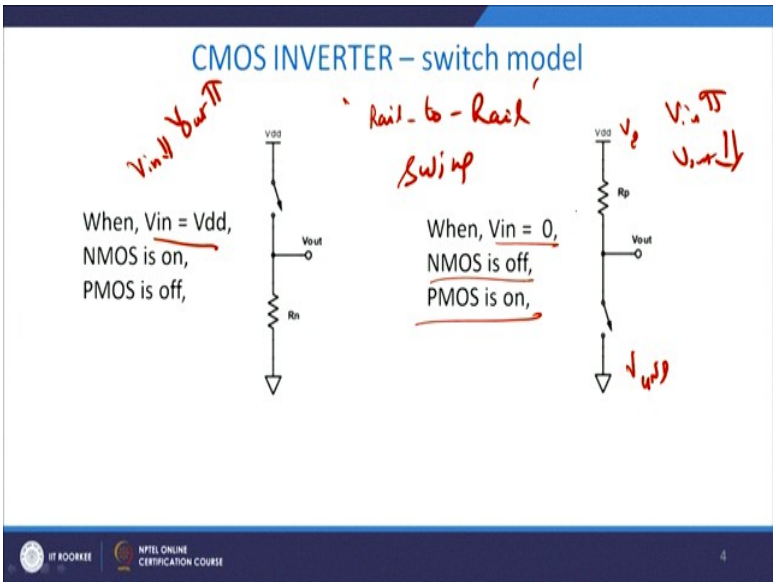

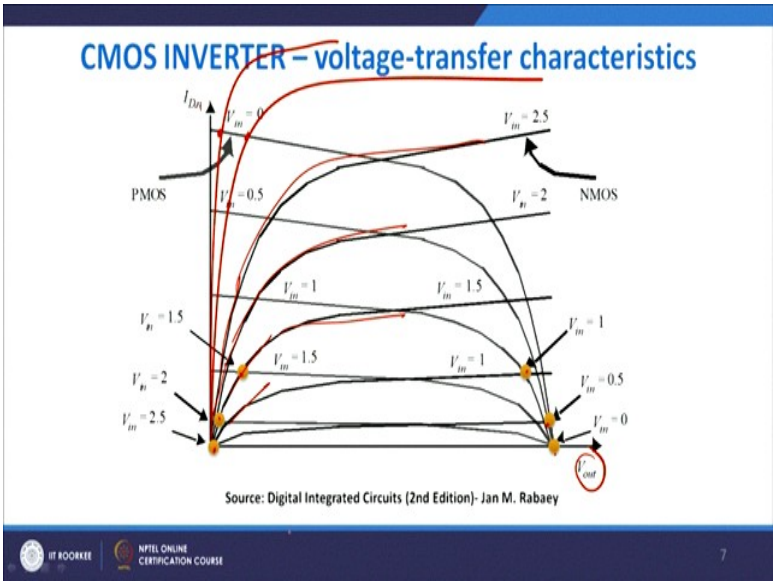

So we have therefore understood one basic idea, let me clarify before we move forward therefore, that two things are very, very important as far as this structure is concerned and the two things which are very important are the first thing is that this CMOS inverter gives you a rail to rail swing fine, what does it mean rail to rail swing? It gives me ride from V_{DD} to V_{GND} the whole signal can be used as directly right. So when my V in is lower, when my V in is low right, my V out is high, high and when my V in is high, V out is low, fine and exactly it behaves like a inverter, it may mix a behaviour of the inverter right and so on and so forth.

So if you look very carefully when V in equals to 0 NMOS is off and PMOS is on right and we are able to achieve a much better design in this case as compared to the previous cases. With the knowledge therefore you have gained till now, let us formulate the voltage transfer characteristics of CMOS, voltage transfer basically means on the x-axis you will have V out and on the y-axis you will have V in, so if I vary V in, how does my V out vary? That supposed to be seen in the VTC of a CMOS inverter.

So what do we do is, it is very simple and straightforward, we try to find out the drain current characteristics of both PMOS and NMOS and then invert it to get the values right. If you look very carefully NMOS has got a profiling in this manner right and if you look very carefully NMOS is always on the this quadrant right, this quadrant it is there. In PMOS, PMOS will be always in the negative and the current will be also negative, so this is my PMOS quadrant device right, this is my NMOS quadrant device right. Then what you do is that you fold it across this spirit in such that you fold it in this manner right, once you fold in this and then you fold to this, let us see how it works out.

So I have got something like this, this is NMOS right and from here I get PMOS is fine. Now if you fold this to this side and then fold this to this side, you finally get something which is very close to the voltage transfer, where they cut they will get voltage transfer characteristics. Now this is NMOS, V in 0, we get to 1.5 and if you solve it on right hand side, I get something like this. So this is 1.5, 1 volt, this is 0.5 and so on and so forth right.

When you have PMOS is you are in third quadrant, you push it across this x-axis, go to this point and then push it across the y-axis to go to this point right which is this one, so I get this. Now if I shift it to the right inside, I get something like this, fine and therefore what we get from all this discussion is, therefore if my this module or this module and this module right, they superimpose on each other, I will start getting a set of points, a set of intersection points in this case right, a set of intersection points.

So how do I do? This is my NMOS, so as you can see it is I versus V and this is the curve which you get right, this is a curve which you get, fine and this is a curve which you get. Now when you plot PMOS versus NMOS, PMOS I_{DN} versus or I_{DP} versus V out, I get something like this right, this is the profiling which you get right. This is the profiling which you get, now wherever these two cut each other, for example, it cuts each other at this point, at this point and at this point, similarly at this point, this point and this point, so these are the points where the currents from both NMOS and PMOS will be equal and they will be sufficiently important to run the at the CMOS inverter right.

So with this knowledge, we can safely therefore say, safely say that these points which are not available to you will still, so if you have an NMOS which goes something like this, you will still have one point here, if it goes something like this then you still have another point here and this will be all your PMOS points. NMOS points will be directly scaled at this particularly limit, so that is what you get out of these differential equations.

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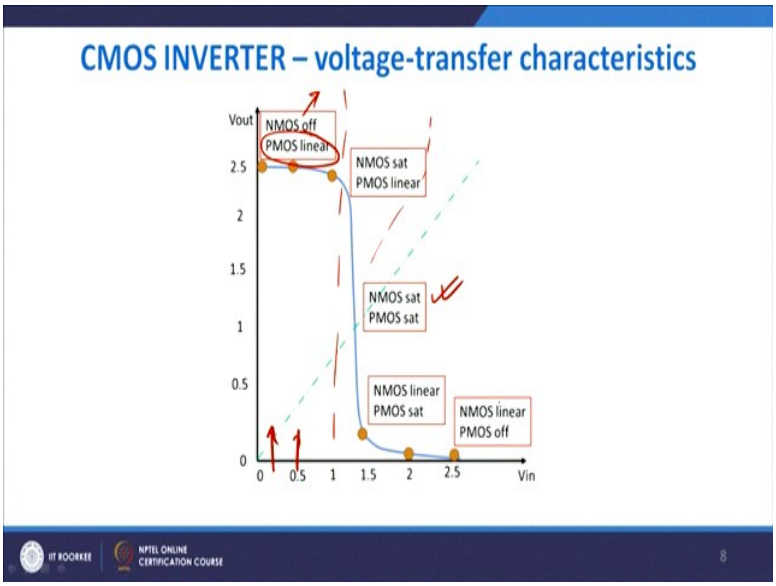

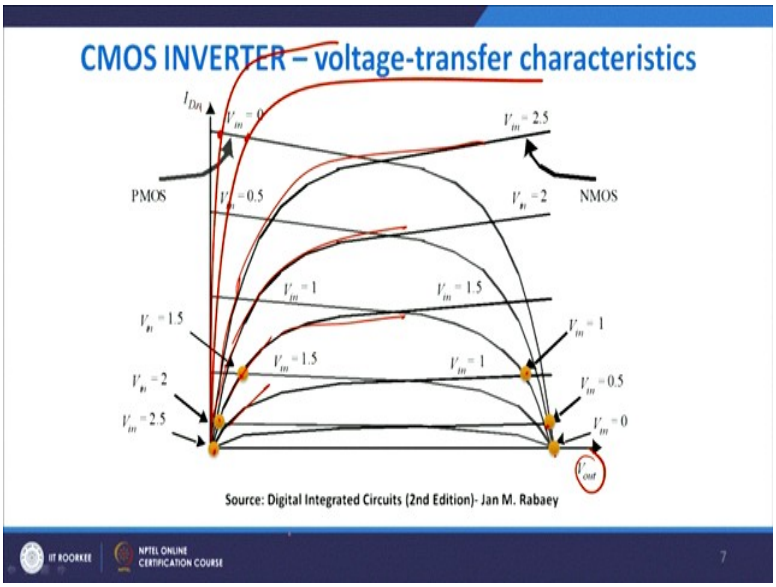

Once you have done that, now you are in a position to explain the various factors which are there with us right. Let me therefore come to the previous case, let me therefore explain to you what the issues are. So now we have done what? We have done the voltage transfer characteristics we have drawn, anything larger than the voltage transfer characteristics will drive PMOS to heavy saturation as well as if you do heavy on the N side, N side will be driven into cut-off region right and that is what you get from here.

Now if you look at CMOS inverter, you see when my input was low, which is this one right, my NMOS was off and my PMOS was in the linear region of operation. So let us be very clear about this particular point, that during the point when your input was very, very low less than 1 volt, then we saw that NMOS was off, of course, because is low than threshold voltage and PMOS is in the linear region of operation right.

If you increase your V in and you reach to a region where your input is there, but the output is not there, then we define NMOS to be saturated and PMOS to be in the non-linear region, so the first was NMOS off, the second is NMOS saturation and PMOS in the linear region and then what we do is, in the third one both NMOS and PMOS in saturation and then just the reverse happens here. Now NMOS is in the linear and PMOS is in saturation, here NMOS is off, so here NMOS will be on and linear and this is linear and off. So you will have off PMOS available with you, so all the five notations which are there at a voltage transfer characteristics of a CMOS appears here as well right, that is very, very important to be careful about.

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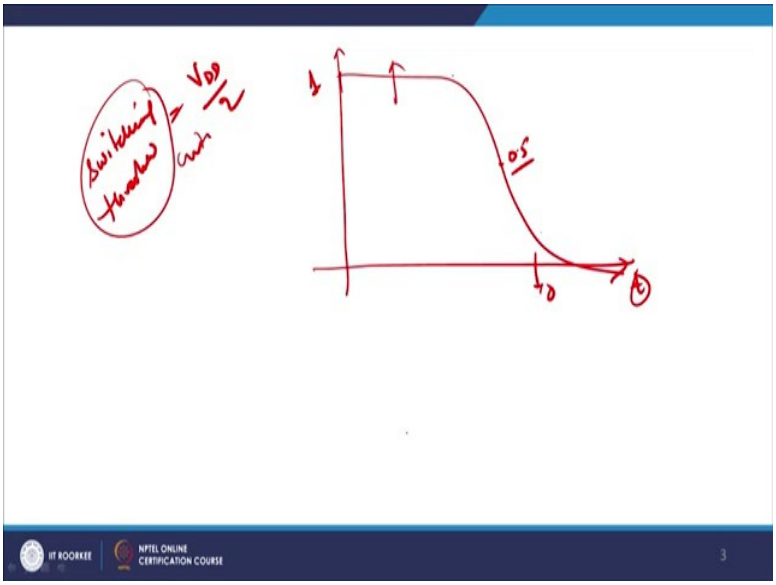

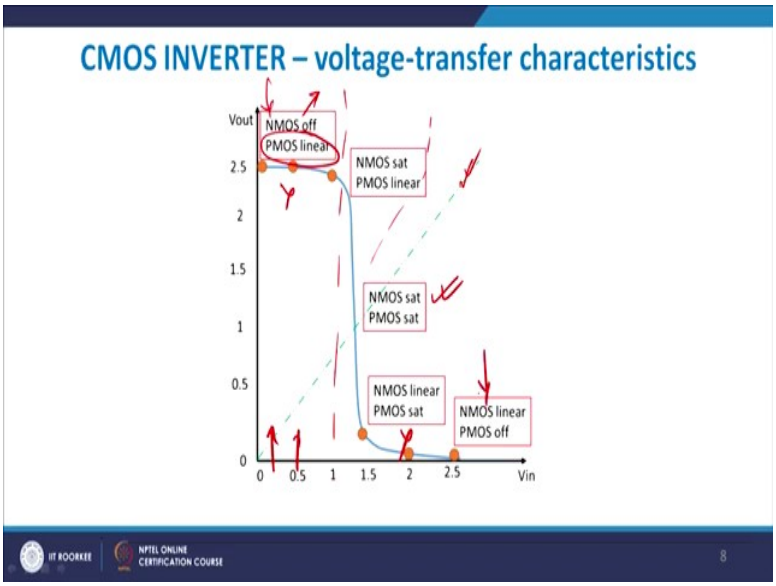

Now how I define a switching threshold? A very important point switching threshold and it is something like this that if you have threshold then it is something like this, suppose let us suppose this is how I get right, this is time and this is your profile. Then we say that switching threshold is that value of input voltage at which you would expect to see a change of state in the output side, typically the ideal value of switching threshold is, switching threshold is basically V_{DD} by 2. So if you apply V_{DD} of 1 volt typically switching threshold critical can be written as 0.5, so if your input voltage is just below 0.5, please read it as 0, if it is greater than 0.5 please read it as 1, right.

So we have understood what is the difference between the switching threshold and positive switching threshold. In this case to be switching threshold right, so we have understood

CMOS inverter, working principle, CMOS switching threshold, what is the meaning of switching threshold? And CMOS inverter noise analysis, you have also understood basic fundamental principles that dV out and dV in should be 1, which means the amplification should be 1 for finding out the values of other variables.

Now let me explain to you the basic, as I discussed with you the MOSFET inverter principles and therefore they are divided into five regions, the middle region which is the green one which you see here is basically the region which is highly unstable, because a small shift in the input will result the Q point to shift either to the top or to the bottom. Top, bottom means this point or at this point right.

So you have to be very careful when dealing with analog or mix signal blocks because they force output to either go to the V_{DD} or go to ground right, whereas your job in this stage is yes, you need to go to high V_{DD} and low V_{DD}, but then you have to be very cautious in the terms that you are stable also in that value of voltages right. So when V_{DD} goes to NMOS of linear region and in my this case NMOS to be in the linear region, whereas here PMOS was linear region, so this is PMOS linear region, this is NMOS linear region right and it works fine for any of a circuitry which you see.

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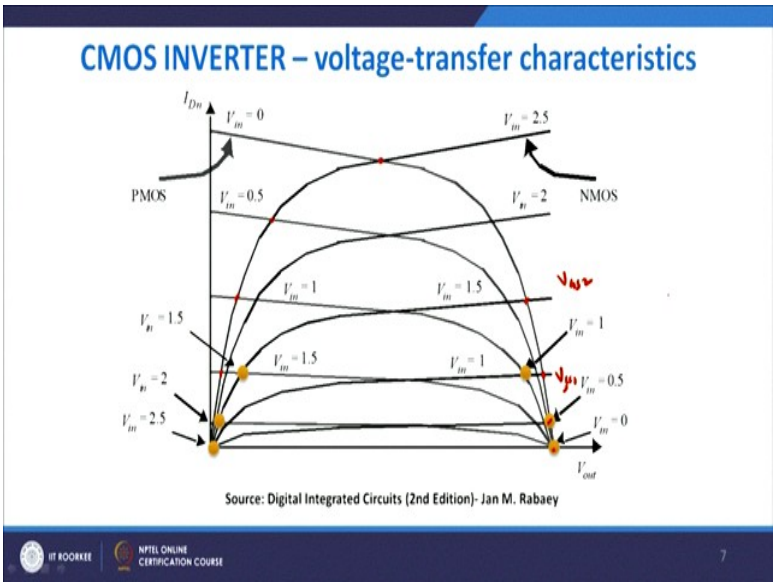

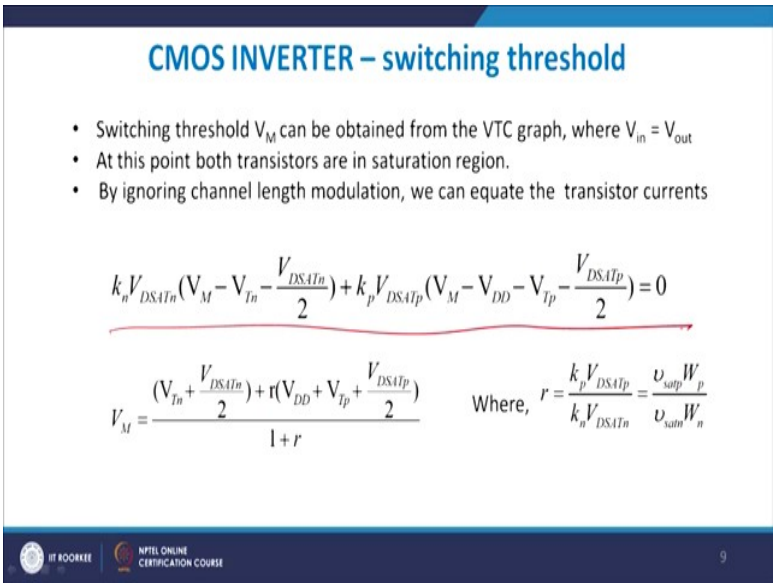

As I discussed with you just beforehand that when you plot this graph, so what I was trying to tell you is that this is being cut, so this is NMOS and this is PMOS, they are cut at various points, the first point is this one NMOS and PMOS, then you this point available with you, then you have got, so this point, this point and so on and so forth and on this side you will have this, and then you will have this, this and so on and so forth right. And therefore for various gate voltages, V in is gate voltages, I start getting a new value of input voltage and this input voltage are strong functions of the output voltage.

As you can see here, therefore this is for V, so for the same V_{GS}, so this is my $V_{GS\,1}$ right, $V_{GS\,1}$, $V_{GS\,2}$ and so on and so forth and these voltages are same for both NMOS and PMOS right. Now we have understood therefore the various regions of operation, let me see how we obtained switching threshold from the VTC of the graph right, Now the VTC is given of switching threshold. Please understand your devices will be in linear region of operation, whenever you are in either region A or region C or region E of the major issue or maybe I will just show you.

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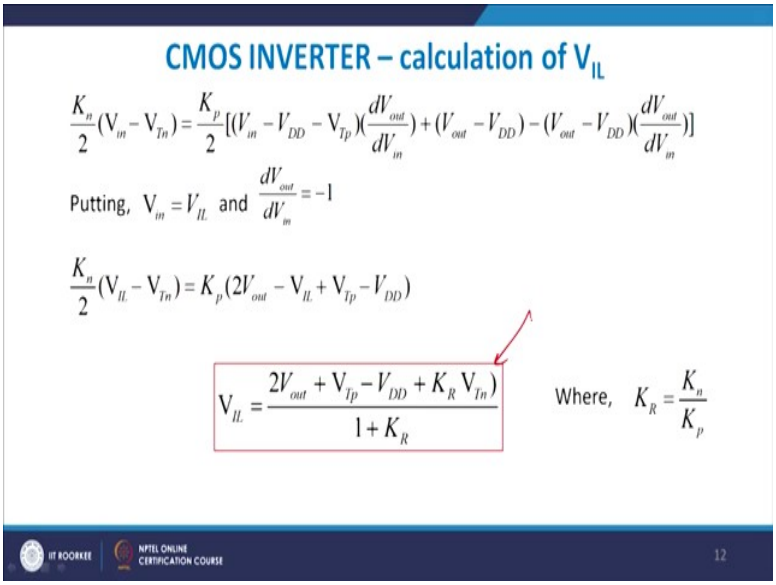

Okay, I will just tell you that, so what I will show to you is that my V_{IL} is nothing but this whole quantity which you see in front of you. How did you find out V_{IL} and we will show you that, doing that but let me come to therefore….

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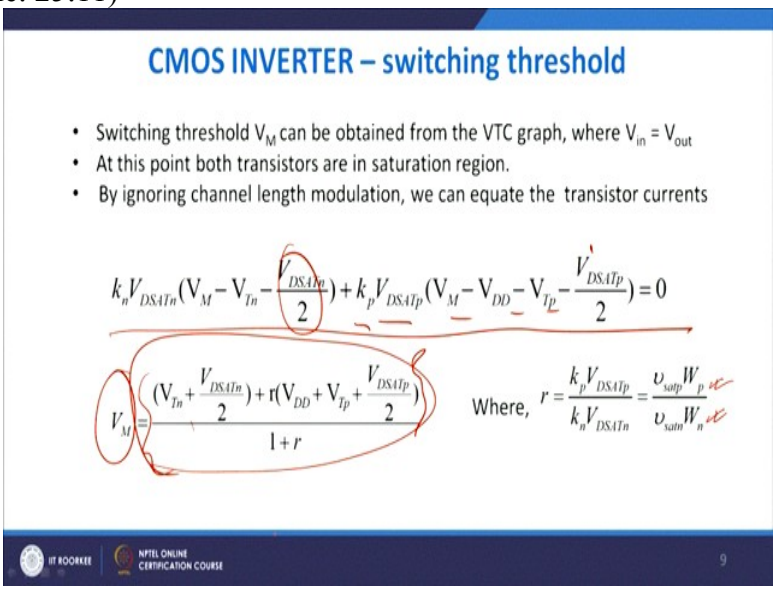

So understand that VM is given by this quantity, where r is basically the ratio of K_P to K_n, $V_{D\ SAT\ P}$, to $V_{D\ SAT\ n}$ and that is also equals to $V_{SAT\ P}$ WP and $V_{SAT\ n}$ W n, so these are the four parameters which are there and we should appreciate the fact that all the transistors if you want to find out both the transistors in saturation right and therefore we say that $K_n V_{D\ SAT\ n}$ into $V_M - V_{TH}$, V_M is nothing but the applied gate voltage, minus V_{TH} - $V_{D\ SAT\ n}$ by 2 right, so this $V_{D\ SAT\ n}$ by 2 is a fixed quantity available with you.

Similarly this, this are all fixed quantities and from here you can obtain the value of V_M or switching threshold right and the given by this formula for the switching threshold $V_{T n} + 2 V_{D SAT n} + R$ and so on and so forth. So as you can see higher the value of $V_{D SAT}$, higher will be my switching threshold.

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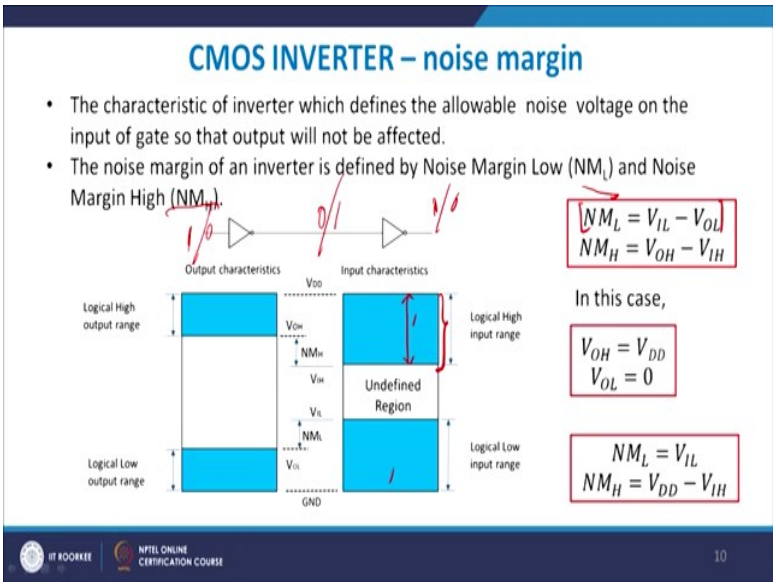

Now let me come to the CMOS inverter, inverter is very simple and straightforward, if there are two inverters connected in this manner right, they connected in this manner then if you apply a 1 voltage here, here I will get 0, I will get also 1 here but let us suppose by mistake I emit 0, then this will be 1, this will be 0. So this is my VDD, output characteristics input and this is logical high range as I discussed with you, this is logical high, which means that any particle or issue with voltage range in this value will be unstable and therefore it will not be available to you in the literature. Whereas if you take care of low noise margin we assume that N_{ML} equals to N_{MH} which means the low noise margin N_{ML} is exactly equals to N_{MH} which is high noise margin. And you do have this and this region effectively available to you. Now we define therefore the N_{ML} is equals to V_{IL} - V_{OL}.

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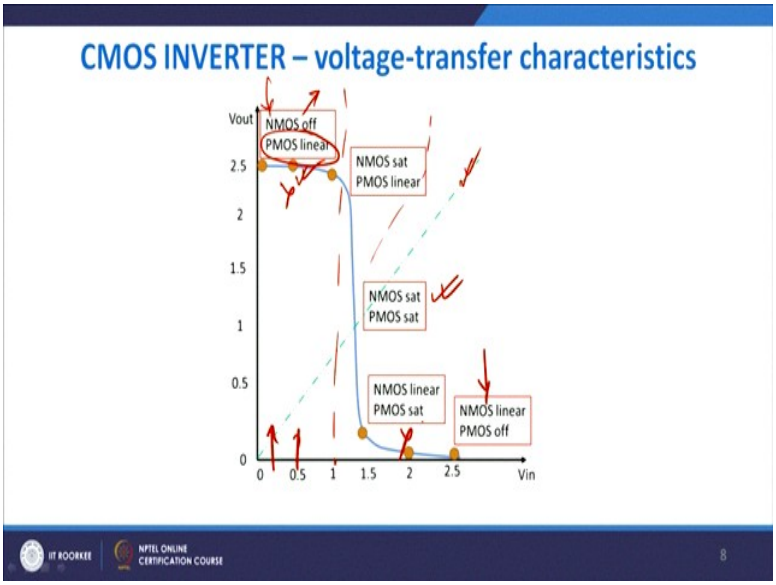

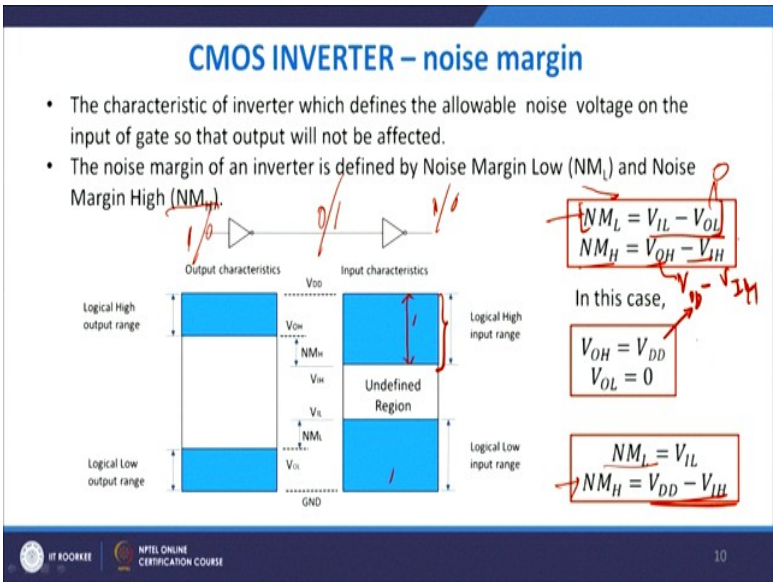

What is V_{IL}? Right, let us see what is V_{IL}. Right, let me explain to you what is V_{IL}. V_{IL} is basically meaning, as the name suggest it is V_{IL} is V input low right. Whenever my input is low, so if you look very carefully here when my input is low, output is high, when my input is high output is low. So when my input is low, I would expect to see that my output is high and similarly when my input is high my output is low.

With this knowledge we define, so we define low noise margin N_{ML} as V_{IL} - V_{OL} and this is input low minus output low and N_{MH} basically is output high minus input high right and therefore this N_{MH} takes care of the higher values, one higher probability of values. Whereas N_{ML} takes care of zeros and lower probability values, right and so on and so forth. Now, as I discussed with you since V_{OH} equals to V_{DD}, so I get, so N_{MH} will V_{DD}, V_{DD} - V_{IH}, V_{IH} is

basically equals to V, let us suppose V_{IH}. So my N_{MH} is equals to V_{DD} - V_{IH} and my N_{ML} is just equals to V_{IL} because V_{OL} indicates 0.

So I get N_{ML} equals to V_{OL}, so I get N_{ML} equals to 0 or equals to V_{OL} and the second case, I get N_{MH} equals to V_{DD} - V_{IH}, and that is what we have understood or given process and idea.

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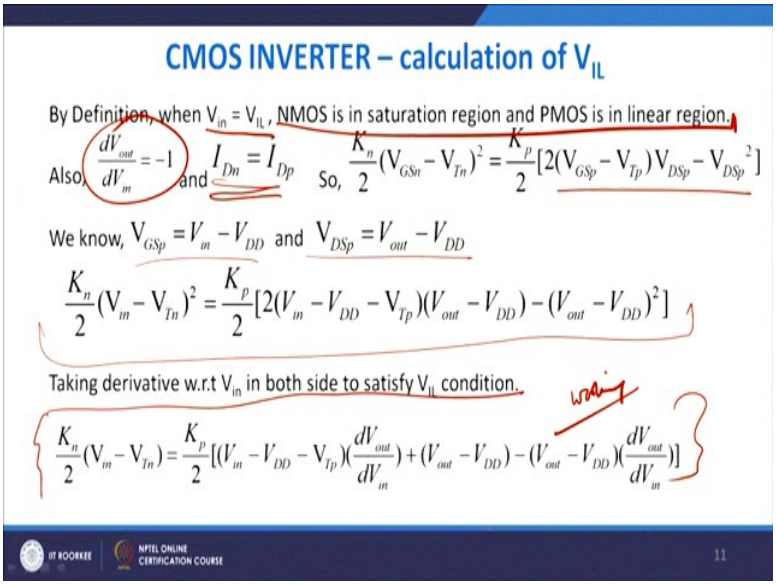

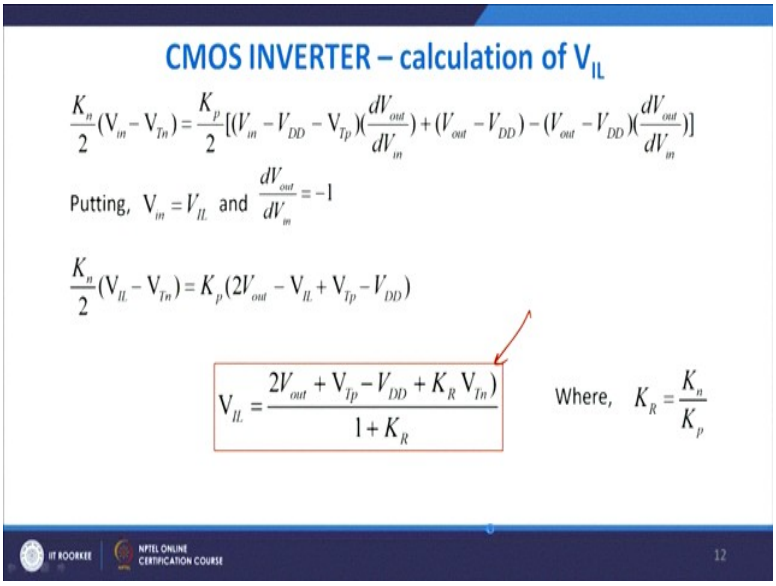

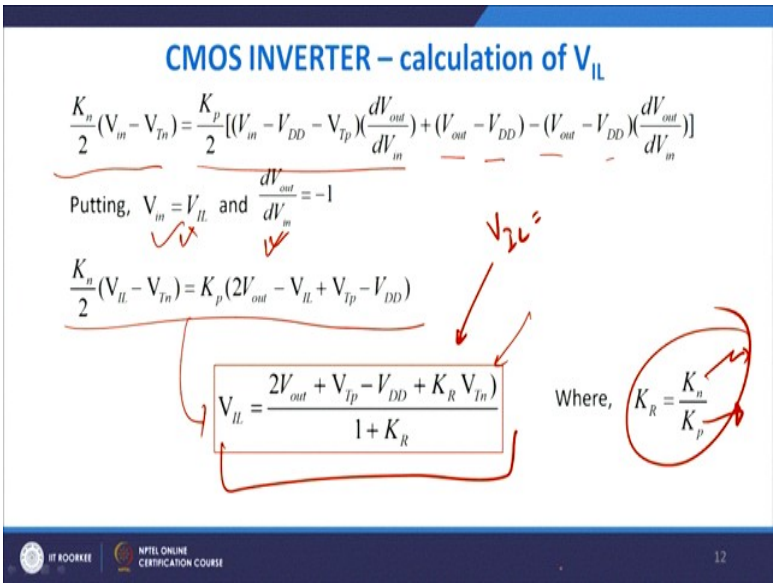

So how to calculate V_{IL}? Well, by definition when V_{IN} equals to V_{IL}, NMOS transistor is in saturation and PMOS is in linear region right, so just the onset of saturation for NMOS and for PMOS it is a linear region of operation and we also know and this is quite interesting. I like you to appreciate this point that dV out, dV in is equals to always minus 1. So you have to be very cautious that when you are calculating V_{IL}, you have to assume that my input and output are exactly equal, if they are not you have to first make it equal in order to find out the value of current, which is in this case $I_{D\,n}$ equals to I_{DP} right.

So therefore, in saturation mode I know K_n by 2, V_{GSn} - V_{Sn} whole square must be equals to K_P by 2, then this is a non-linear region of operation. If you remember, I think it is clear to you. So in this problem or in the solution to the problem is that you do have a fixed value of gate voltages and your applied voltages but the input signal will tend to change it slightly whenever the output signal is above, when the output signal is above V_{DSP}. So we know V_{GSP} is equal to V_{IN} - V_{DD} and V_{DSP} is equal to V_{out} - V_{DD}. If you solve it I get this big equation, it is available to me. If you take derivative with respect to V_{IN} then both sides will satisfy V_{IL} conditions, so I get this equals to this, into this plus this plus this. So I get this as the workable solution for this V_{IL} input low.

So we have learned two things, what is input low? Input low is the voltage at which the output is high right. CMOS inverter calculate V_{IL}, V_{IL} is basically this point. So what I say is that this equals to K_P by 2, this whole thing plus this minus this minus this minus this dV out dV in right and if I place dV out, dV in equals to minus 1, V_{IN} equals to be V_{IL}, I get a big equation like this, which can be actually downtrodden to V_{IL} to be equals to this much. So relatively K_R is basically K_n by K_P parameter for n and P. But if these are okay, if these are

fine, the values of parameters are extracted fine manner, you can say that V_{IL} is given by this equation, fine and it depends on the value of K_R, it also depends upon the value of V out and V_{DD}.

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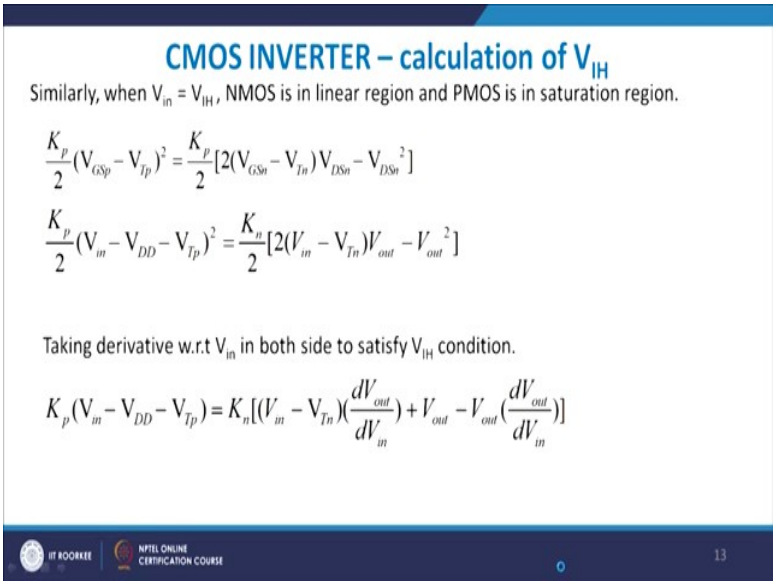

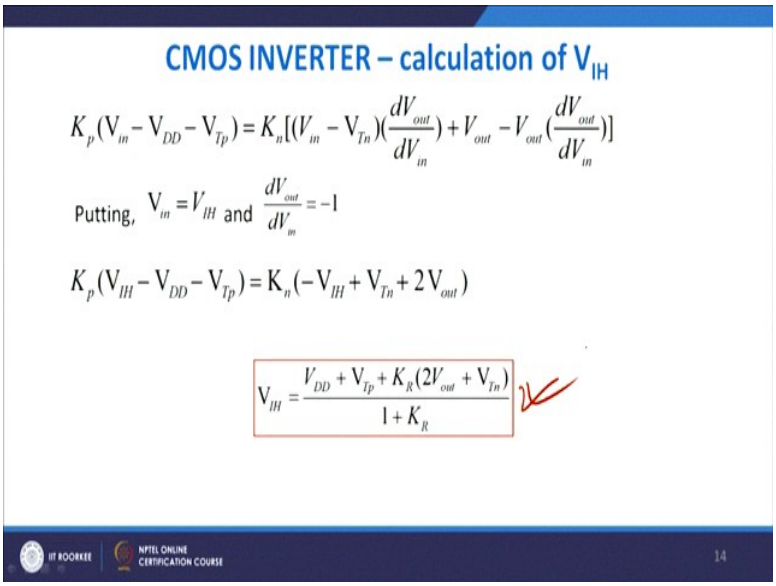

If you want to calculate the value of V_{IH}, then V_{IH} is input high, which means that whenever my input is high and output is low anything larger than that it is not expected from you. So if I solve it that grade is exactly the same, V_{GSP} - V_{TP} whole square is equal to this whole quantity. Similarly, for a β value or a breakdown value I get this into consideration and if you take the derivative of both sides, I get V_{IH} as some value V_{IN} equal to V_{IH} and dV out equals to dV in. If you solve it I get V_{IH} equals to this quantity which you see in front of you. This is

the value here, but this would not have come out if you did not do the derivation properly in your previous case.

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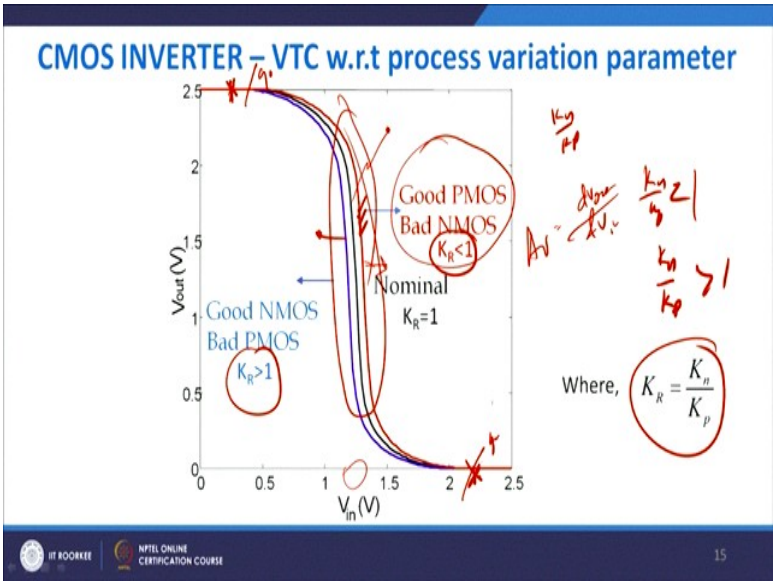

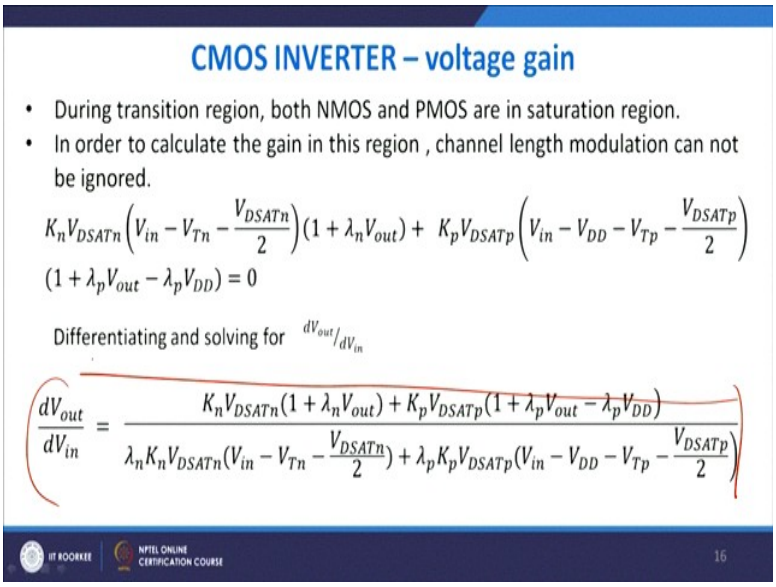

The voltage transfer characteristics varies in this manner that for nominal when K_R equals to 1, I get this, the black one is the nominal 1 and it is almost giving a fall but if you take good NMOS or good PMOS and bad NMOS then the transfer characteristics shifts to your right, whereas if you take good NMOS and bad PMOS shifts to the left, good, bad variably means that when you say good PMOS, does it have, I say it is good if and only if it has got a pull up capability to VDD.

Similarly an NMOS can be said to be good provided it is able to push down or pull down the voltage to ground right, so none of them we are able to do and therefore I can safely say that

this is a good PMOS right and therefore shifted to the right with high switching threshold and this is good NMOS and lower switching threshold right. So this is K_R less than 1 and K_R greater than 1, K_R is basically K_n by K_P, so when the K_n by K_P is greater than 1 I shift to the left and when this is less than 1, I shift to the right. And the nominal value is K_R equals 1 means K_n equals to K_P, which primary means that PMOS and NMOS have equal pulling capacitor.

From the same graph, see then, If I say, from this graph, you can see that I can switch from this point to this point and I can go from logic 1 to logic 0 right, this is output logic 0 and this is output logic 1 which you see. But then somewhere in the middle, obviously the gain here will be 0 and the gain here will also be equals to 0. But somewhere in the middle your gain will be a strong function of your V_{IN} because if you remember A_V equals to dV out right, dV in, and that is what you get here. So dV out dV in right down and you get this big expression which is important in front of you.

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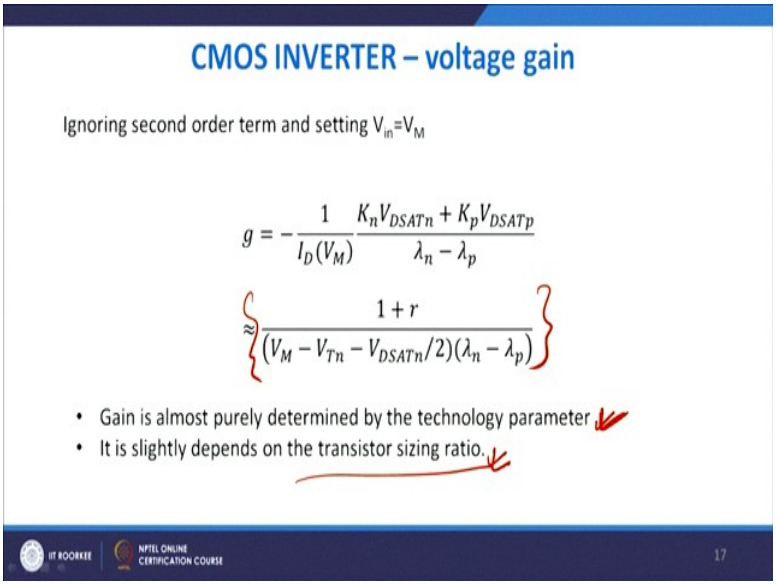

Now if you ignore the second-order term and putting V_{IN} equals to V_M, V_M is switching threshold, then I get g or the gain to be equals to this big quantity which you see in front of you and it is given by this quantity which you see here. It depends upon all these factors and so on and so forth, so therefore gain is purely determined by the technology parameter and it slightly depends upon the transistor sizing ratio right. So it depends very, very small on the sizing ratio and it is mostly determined by the technology parameters and not by the structural parameters of the device right.

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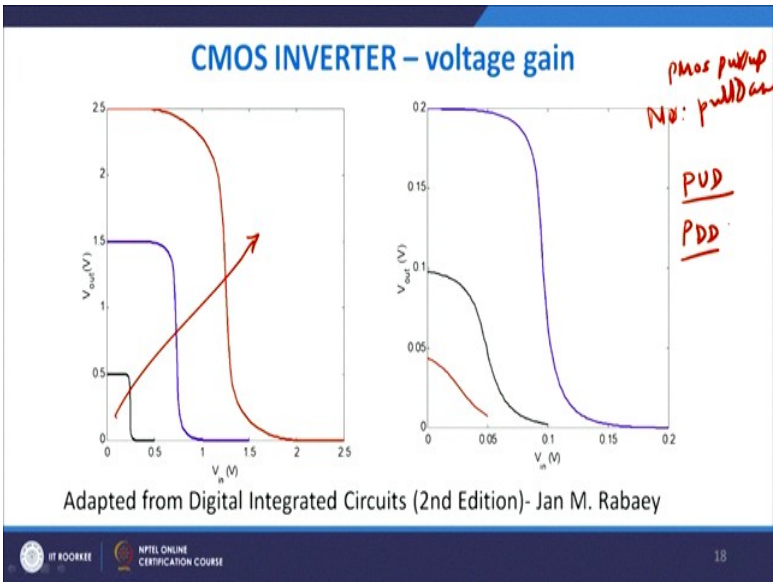

As you can see here, therefore for varying values of V_{DD} I would expect to see, so which means that the V_{DD} is moving in this direction, higher the value of V_{DD}, higher will be the switching threshold and lower the value of V_{DD} lower will be the switching threshold. I hope you have understood why is it. Similarly, if you do a plotting of the graph between various values of V_{IN}, then automatically those values of V_{IN} which has got higher values of V out will be shifted to the right and vice versa will be for the blue and black, black and red onto the left and that gives me good idea. It gives me therefore the, by making my inverter pull up and pull down, so why we define?

So my PMOS is referred to as pull up and my NMOS is referred to as pull down fine, pull up and pull down, why pull up? Because PMOS is pulling the voltage to the V_{DD} and NMOS is pulling that to ground and therefore there is a pull up device and, so we define the PMOS to be as pull of device and below one we define as pull down device and we get this substrate configuration here.

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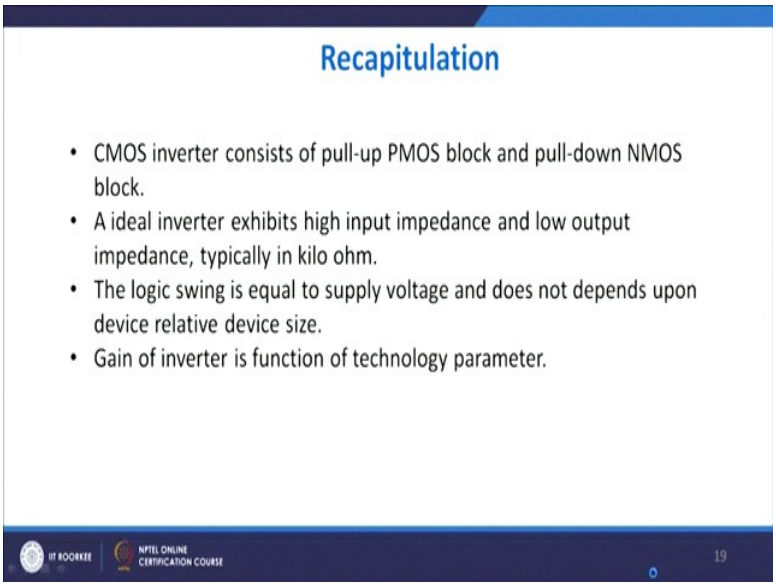

So let me recapitulate what we did. CMOS consists of PMOS block and NMOS block, an ideal inverter has got a high impedance and 0 output impedance. The logic swing is equal to supply voltage, it does not depend upon the device relative size and the gain the inverter is mostly a function of the technology.

I hope you have understood what we have discussed in this lecture; we will come back with another series of lecture on the CMOS basic inverter part II right. Thank you, thanks a lot, thank you very much.