Microelectronics: Devices to Circuits
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Lecture 17 - MOS Parasitics and SPICE Model

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Hello and welcome to the NPTEL online course on Microelectronics: Devices to Circuit, today we will take up what is known as the MOS parasitics and SPICE model, the name of the today's module is MOS parasitics and SPICE module or SPICE model. In our previous discussion or interaction we had seen the second-order effects which are related to MOS devices, which primary means that what do you mean by drain induced barrier lowering, punch through. We have also seen the substrate effect or a body bias effect. We have also understood what is the meaning of velocity saturation, under what limits of operation do we have second-order effects coming into picture, what is the reason why the second-order effects coming into picture, what are short channel effects, how does threshold voltage gets affected by the short channel effects.

Why this is important to study? Because we move ahead in our course we will see that these influence the output electrical characteristics of the device, and as a result, the circuit get influenced by these variations. Now another important variation of a device or important parameter of the device is its parasitic, which means that those parasitic resistances and capacitances which the device has already inbuilt into it, but they appeared to you at certain frequencies of operation, thereby limiting the usage of the MOS devices at those frequencies.

So in order to incorporate all those things and understand the basic concepts of MOS device and therefore give you a basic feel of basic SPICE models which are available to us, let me explain to you therefore the outline of this current talk as far as MOS device is concerned.

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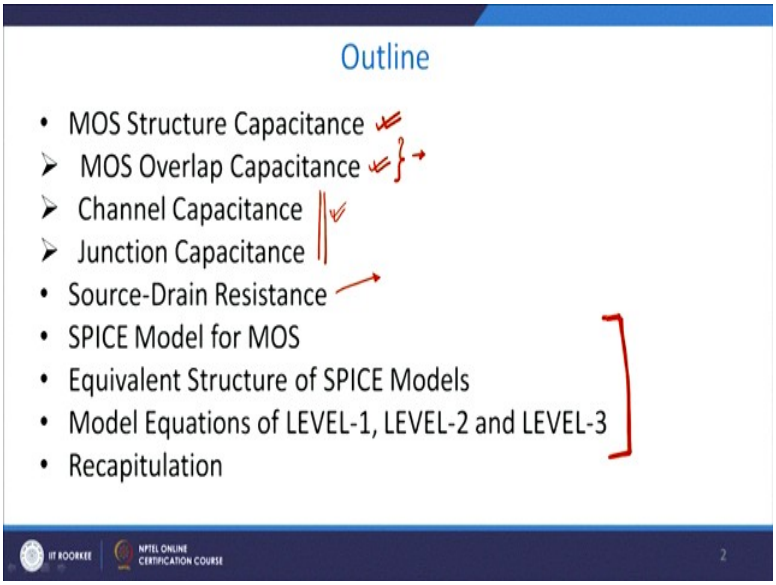

We will look at the MOS structural capacitance, which means that we will look into the fact that how a MOSFET structure, the very fact that it is structurally designed will give me various capacitance values associated with it, those things will be clear to you. We will look at MOS therefore overlap capacitances, various overlap capacitances, we will be looking at junction capacitance and channel capacitance right, these capacitances which is basically MOS overlap is primarily because of problems with fabrication and so on and so forth, but channel capacitance and junction capacitances will always arise even with one of the best fabrication facilities.

The meaning of source-drain resistance should be clear to you as a designer and then we will be entering into what is known as the SPICE model for MOS devices right, SPICE is basically a circuit simulator, which is being used quite often by large number of people across the world, most of the versions of SPICE are open source and can be downloaded from the Net and can be used by you and therefore understanding that within the SPICE how does the MOS work, what is the equivalent circuit model for a MOS device within the SPICE should be understood. And that is what we will be taking up at these MOS devices, equivalent circuit models and then we will look at level 1, 2 and 3 of model equations of MOS device right and

see how, so each level will actually refine the drain-current characteristics, so you should be able to understand the various level and how it works in terms of its working principles.

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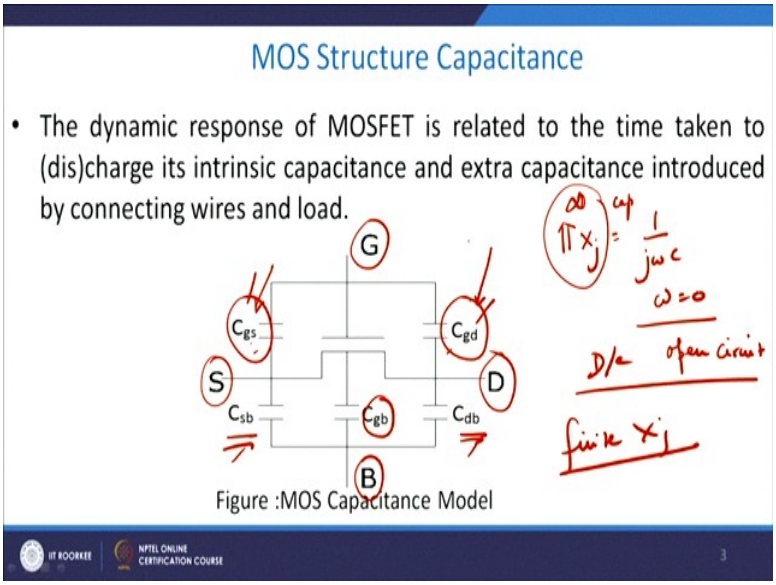

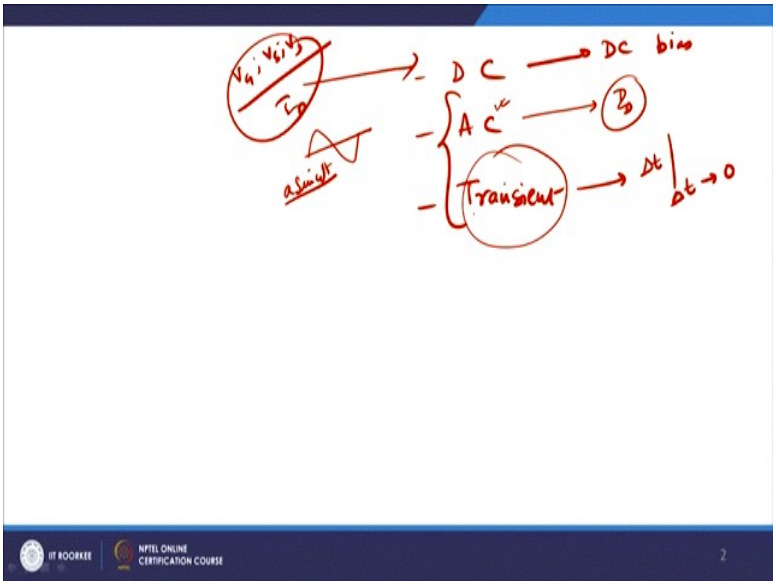

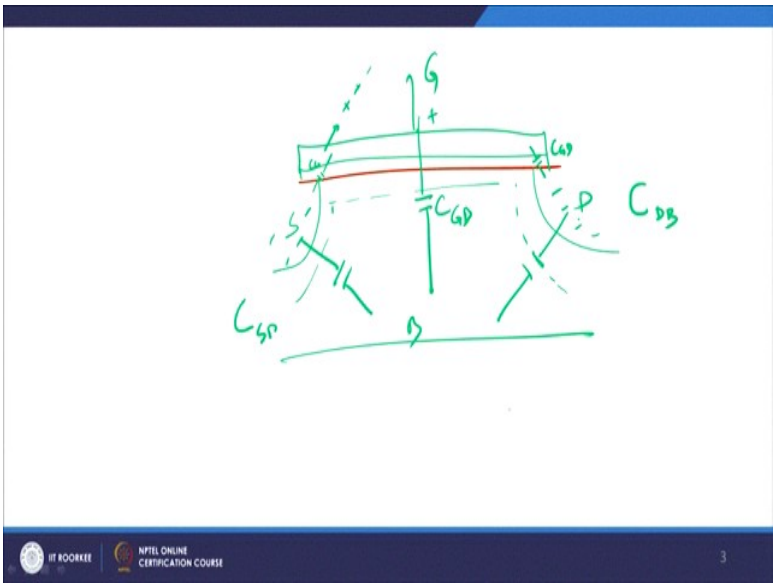

Let me now come to MOS, MOS structure and its capacitance. Now please understand when you are working with a DC bias or when you have applied a fixed value of voltage either to the gauge, drain or source terminal then of course w is equal to 0, and therefore or the frequency operation is 0, and X_J if you remember for a capacitance is 1 upon JwC and therefore X_J is infinitely large for w equals to 0. So for a DC bias, for a DC I can afford to basically let them behave like open circuit right, like an open circuit. So when you are dealing with DC biases any capacitances within any other networks right, any electrical network can be made as open circuit because the concerned impedances are infinitely large and therefore you open it right.

When you open it fine then you do not have any other place to go and therefore there will be a current flow and this current flow will depend upon the network parameters. Whereas when you have a variable in the frequency which means you are working in the AC domain and the frequency of the AC signal is varied from some X to Y value it is varied, then this X_J which is the capacitive impedance right and assuming it to be infinity when you are applying a DC that does not hold good.

So you will have now a finite right, X_J or a finite impedance and as a result, we have to replace this by sort of a resistive element which is basically frequency dependent resistive element and that is the problem area for MOS transistor, so when MOS device you are working in a DC domain and try to find out the I V characteristics, well does not matter because you are buying the value of DC and for all DC this is open circuitry and all the discussion which we had for the previous few interactions will hold good.

But let us suppose that you are taking AC analysis or you are doing a transient analysis right, there are three types of analysis which we generally follow: one is known as the DC analysis, we have a AC analysis and we have got transient analysis right. DC is when you apply a DC biases, so which means that is not a time varying bias, it is a fixed bias and you give a bias, and try to find out a current at those fixed biases. So you fix the value of V_G, V_S, V_D and then try to find out the value of I_D and that is what is known as the DC bias.

What is AC bias or AC analysis? AC analysis means you give an input signal, which is not DC but suppose a sine wave, let us suppose a sinwT and for these values of a sinwT, you try to find out the I_D value at the output side right and you try to find out what the I_D value is that is what is AC analysis.

What is transient analysis? Transient analysis is when you do the analysis for ΔT and T tending to, ΔT tending to 0, which means that for very short interval of time you try to find out the value of voltage or current provided the applied biases are varying from, you know in a very, very fast sense and you are able to calculate the variations in the value of drain current for those small values right. So for all these, for last these, for these two we will actually will be doing a large amount of capacitive analysis.

So you see here that, if you look at the MOS device right and if you have the, these are basically known as this and this are basically C_{GS} gate to source and C_{GD}, so you have gate terminal here, you have bulk, you have drain and you have source, so this a four terminal device. Now as we, so if you go back to your previous discussion, from a previous discussion knowledge you will understand that if you have a, sorry let me help you out in the sense that, let me say that you have a device and your device is something like this that your source is here and drain is here, so I have a source, drain right. I have a gate here and then I have a metal gate here right and I have bulk here and this is gate.

So you see this is high charge, this is also negatively charged capacitance, this is negatively charged, so which means that between these two I can have a C_{GS}, C gate to source, similarly between this two I will have C_{GD} gate to drain, these are the overlap capacitances right. You also have a capacitance which is, so this is C_{GS} right and this is C_{GD}, gate to source and gate to drain, you also have a drain to bulk which means that let me see, so drain right, you will have a depletion region here and you will have a depletion region here right, so you will always have a drain to bulk capacitance here and source to bulk capacitance here. So this is C_{DB} and this is C_{SB} or BS right, whatever you want to say, so this is C_{SB} and C_{DB} which you see.

So this is overlap capacitances, these are structural capacitances, which is available to you. You also have gate to bulk capacitances, what is gate to bulk? Because you will have gate potential here and bulk potential here, so the capacitance available at this point is given by C_{GB}, so effectively there are five capacitances which influence the AC or the transient analysis of a MOS device right and these 5 capacitances are mentioned in this figure.

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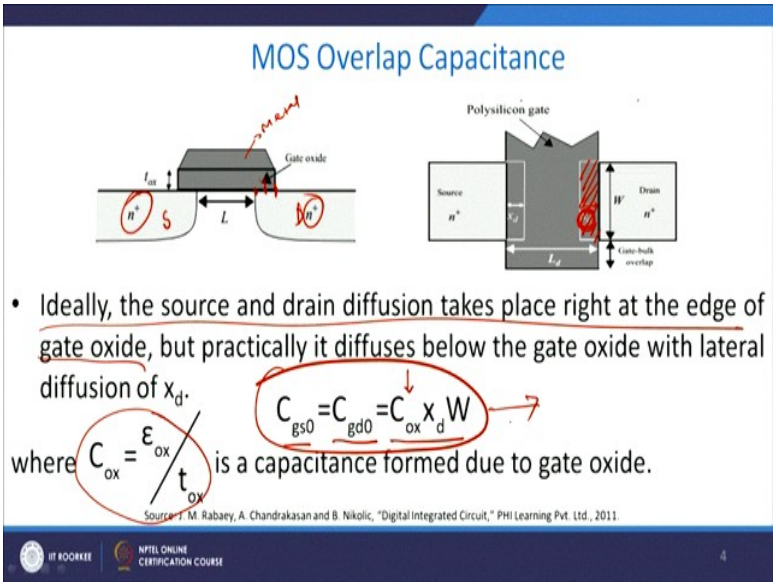

As I discussed with you earlier, so when you have source and drain and they are overlapping through the gate oxide, so this the metal gate right, this is the metal gate and this is the gate oxide. This is channel length and this is the t oxide value. As I discussed with you ideally, the source and drain takes place at the edge of the gate oxide, ideally this should be at this edge right, but practically there is some diffusion right, why? Because see you do this doping here N^+ region and N^+ region by a diffusion phenomena.

So you have a diffusion phenomenna and diffusion is, if you remember is by the by very nature, you cannot stop at a particular point it will have some amount of out diffusivity, so the diffusion will result in what? The diffusion layer being extended towards the each other right, and as a result, you are supposed to stop somewhere here, you added up, you ended up somewhere here. Fine, and as a result, you will have some capacitance which is available at this particular point.

So if there is lateral diffusion and because of this, you have an extra X_D as the diffusion, lateral diffusion length, then we define C_{GSO} and C_{GDO} as C oxide into X_D into W, I suppose you can understand why. Because X_D is this, W is basically this, this dimension W, so W into

X_D is the area under the overlap region, this multiplied by area per unit capacitance of C oxide which is over it will give you the value of C_{GSO} and C_{GDO} right, C_{GSO} and C_{GDO} means gate to drain and gate to source voltage and this is known as gate to bulk overlap and this is gate sorry, and this is gate to drain overlap and this is gate to source overlap right.

C oxide is given by Epsilon oxide by t oxide which you see and therefore this is the gate oxide with lateral diffusion when X_D is available. So, as you can see higher the value of lateral diffusion more will be the value of X_D and as a result your C_{GSO} and C_{GDO} will be also larger in that case, which means that their influence over the transient analysis will also be pretty heavy in nature or pretty large in number.

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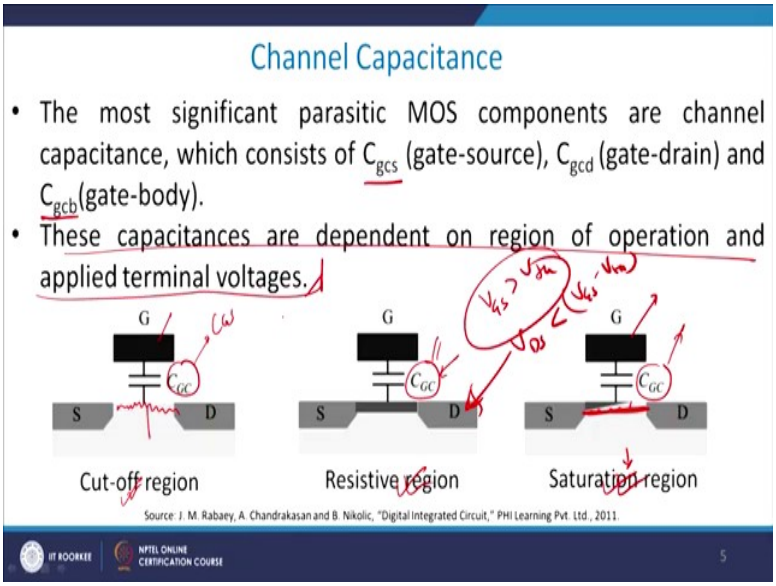

Now let us come to the channel capacitances, now channel capacitance as I told to you will have again two components primarily. We have understood C_{GS}, so it is basically gate to source, so it is gate to sorry, this is C_G gate, channel source, you have gate drain, so gate drain and then gate body, so this is gate to channel, this is gate to channel and this is also gate to channel for three regions of operation for cut-off, for resistive region and for saturation region right.

As we discussed cut-off means when gate voltage is almost 0, gate voltage is almost less than threshold voltage. At that point of time you do not have any inversion layer available with you right, you do not have any inversion layer at this particular point right, but you might have some charges here and, so this charge and this charge separated by an oxide layer will give rise to C_{GC}, C_{GC} which is basically your C_{GC} this one and then you get C_{GC} because when

you go to resistive region and your gate voltage is just greater than V_{GS} but V_{DS} is less than V_{GS} -V_{TH}, this is this region on operation right.

So you will have thin-layer available to me, but it is still not inverted and fully inverted. In that case you will have C_{GC} and now when you have saturation when drain to source voltage is so large that it eats away into the channel and therefore your affected channel reduces, you will have a new value C_{GC}. Now what people have done over the years is just for the sake of making it easy to understand they have divided this C_{GC} into two parts, one is towards the source end, one is towards the drain end and then they say that if the doping concentrations in the source and the source and the drain is almost the same I would expect to see that the C_{GC} on the source side and C_{GC} on the drain side to be almost equal to each other.

One important point which you should take care of is that when you have inversions, strong inversion, then in saturation region, for example you have a large number of charge carriers here right and they act as a screening, sort of a screening charge screening mechanism, so they tend to screen the charge of the gate from the bulk region right, so that is quite interesting and therefore you will see that the gate to bulk actually falls down, capacitance falls down at a very, very high value of V_{DS} because the inversion layer which is there in the middle between at the silicon-silicon dioxide interface, they tend to screen out the gate and the bulk charge and therefore you do have a drop in the value of C_{GS} right.

As I discussed with you therefore these capacitances are dependent on the region of operation and also of the applied potential terminals right, so how much potential you are applying at various points, they are depending on that and then whether your operating in the cut-off region, whether you are operating in the resistive region or whether you operate in saturation region will also be important right.

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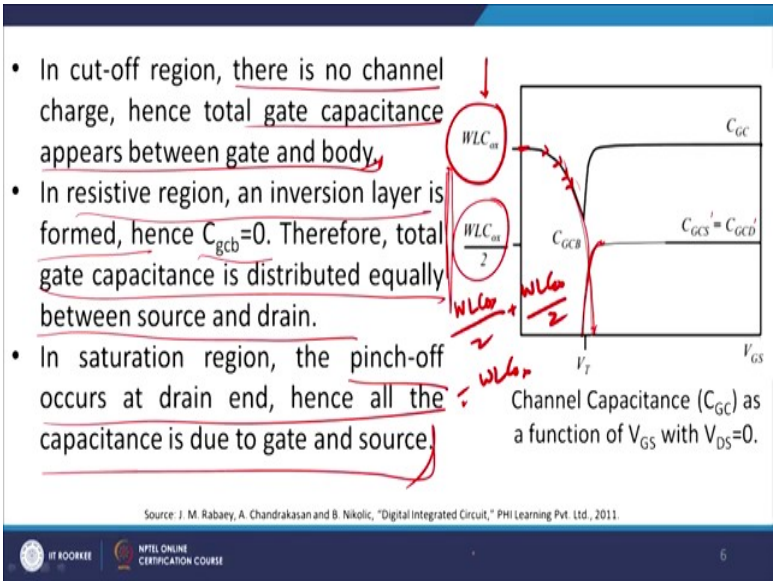

Okay, in the cut-off region as I was discussing there is no channel charge right, hence the total gate capacitance appears between gate and body, I thought this is perfectly clear and very easy to understand but when you do not apply any, when you cut-off there is no inversion layer and gate to body and gate to channel are exactly the same because channel in any case you do not have any free charge carriers right.

Now if you therefore plot VGS versus capacitance here and we will see how it works out, when your gate voltage is very, very low or in a cut-off region you WLCox, Cox is basically oxide capacitance per unit area multiplied by area gives you the total capacitance, so the total capacitance is something like this. As you go on increasing the value of gate voltage, since more and more charge carriers starts to form, the screening takes place and the capacitance starts to fall down, so you have a reduction in capacitance at this particular point.

In the resistive region, an inversion layer is formed right, hence C_{GCB} or bulk is 0. Therefore the total gate capacitance is distributed equally between source and drain right. So let us suppose you had 10 femtofarad as a total gate to bulk, bulk was to 0 and therefore this breaks down into 5 femtofarad, one goes to the source side another goes to the drain side and that is what is basically found out in this region, that you will have equal distribution between source and drain right. You will have equal distribution between source and drain and this will result in equal charging on the source and drain side right and they will be almost equal to each other.

Now in saturation, since the pinch off occurs at the drain end, hence all the capacitance is due to gate and source, I think this is pretty clear because when you pinch off on the drain side and there are no charge carriers there because it all depleted, all depleted of free charge carriers, so again, the all, it is being shared by the gate and the source, so it goes, if you look very carefully the total charge we will see later on. But, if you look very carefully below V_T the contribution is gate to channel bulk as I discussed with you, but it falls down, see its falls down and it goes something like this right, because screening effect is there.

Beyond V_T gate to channel for source and gate to channel for drain it looks something like this, it becomes larger and larger right, but as the gate voltage becomes larger and almost fixed, for a fixed value of a gate voltage, I get that the gate to source voltage and gate to, gate to channel for source contribution and drain contribution is equal and therefore you see it is given as WLCox by 2, so half, so half is supported by, so you are initially starting with WLC oxide, you ended, in saturation region you ended having the maximum value of each one of them to be WLCox by 2. Since they are in parallel, therefore I can safely write down plus WLCox by 2 as the total capacitance which comes out to be WLC oxide.

So you see, which was initially the value, which was here? So which means that when the devices were switched off, the whole capacitance was taken care of by gate to channel, as it switches on and goes to saturation the same capacitance get distributed between the source end and the drain end right. So that is what we have learned from all discussion so far, as far as this device is concerned.

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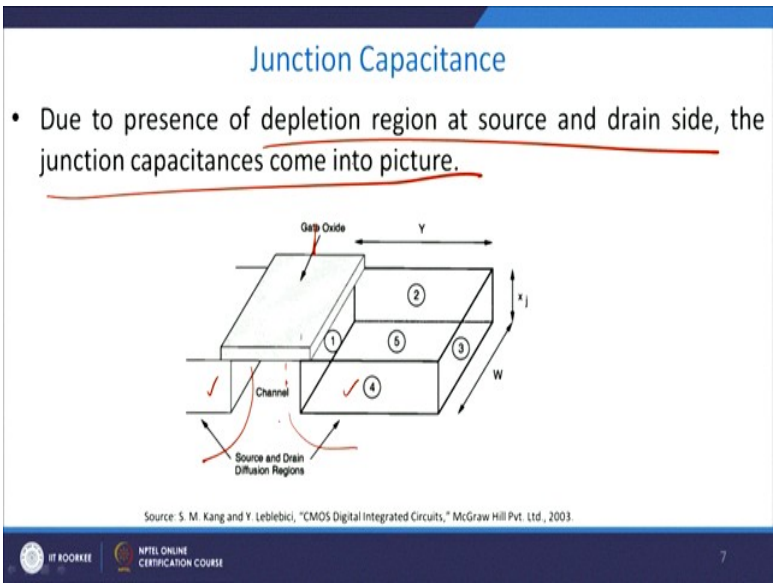

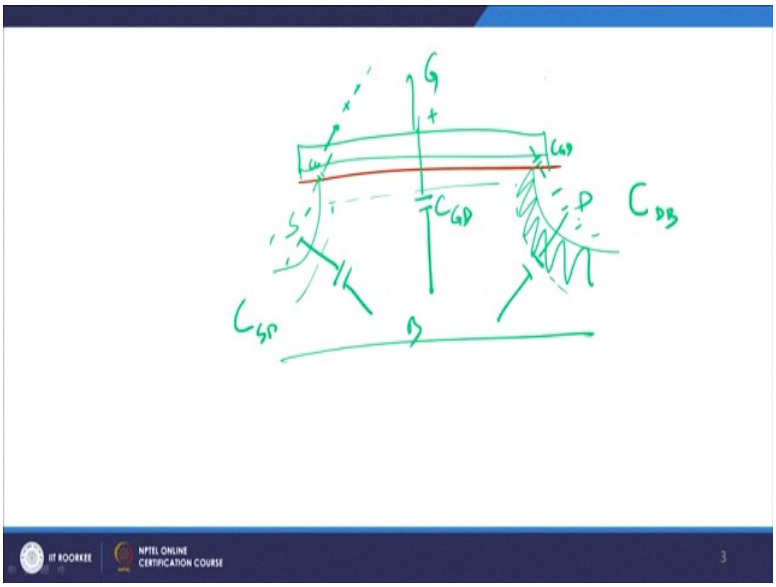

Now what is the junction capacitance? Now due to the presence of depletion region at the source and drain end, the junction capacitance comes into picture; this is very straightforward and simple way of looking at it. So, you remember there was a depletion region here, this will give rise to junction capacitance, so I think that is very fair story which you see. So if you look very carefully this is the source and this is the drain diffusion region and you have a gate region here and so you will have a depletion region somewhere here and a depletion region somewhere here, this will give rise to a junction capacitance.

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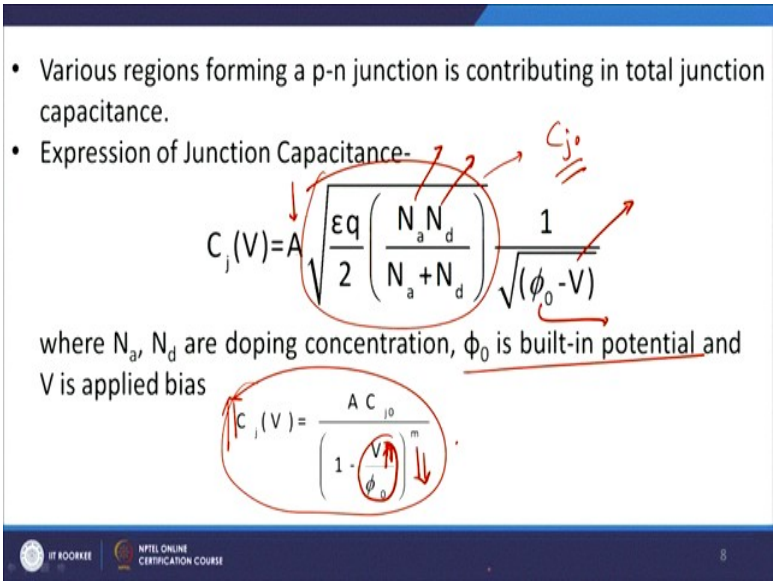

Of course, maybe I can show you to is, so it is basically a p-n junction which is formed, a p-n junction depletion region right, so if you remember your basic p-n junction theory, we can come to know that the expression for the junction capacitance C_J is given as A times epsilon

Q by 2, Na, Nd upon Na + Nd root over upon 1 upon this value, where A is the area of the cross-section between the source and the drain side, Na, Nd the acceptor and the donor concentration and V is the applied voltage which you see and Phi_0 is basically known as built-in voltage right and V is the applied bias.

So C_{JV} is basically A times, this factor is basically my C_{J0}, C_{J0}, which means that under 0 bias the junction capacitance, why? Because even if you do not apply any bias right and you have a differential in doping concentration, there will be always a depletion region formed, howsoever big or small right, that capacitance because of that is basically my C_{J0}. Now that gets effected by an external bias when we apply a voltage V, so you can very well see that when you apply a voltage V if you go on increasing this V, this quantity becomes larger and larger, so 1 upon this quantity goes on reducing right, and as a result this whole quantity becomes larger and larger.

So when you increase the value of voltage right and you reverse bias it the depletion thickness becomes larger and larger and you end up having a larger capacitance, which is there with you in case of a p-n junction diode theory as well as for the MOSFET theory right.

Let me come to source and drain resistance, very important part in a parasitic part, so we learned four capacitances with us, actually five, one is gate to source, gate to drain overlap, one is channel, bulk to source, bulk to drain channel, another is gate to channel right. But the point is that all of them do not show their effectiveness at each bias right, as the bias changes the weight of each of the capacitance goes on changing right and therefore it is fair to say that the capacitances are not equal and they are not, they do not show their effect equally for all the conditions of operation of the device, right. So this is what you learned from till now and this is basic learning from a capacitance point of view and these are parasitic capacitance mind you, and therefore they restrict your high-frequency operation of MOS device.

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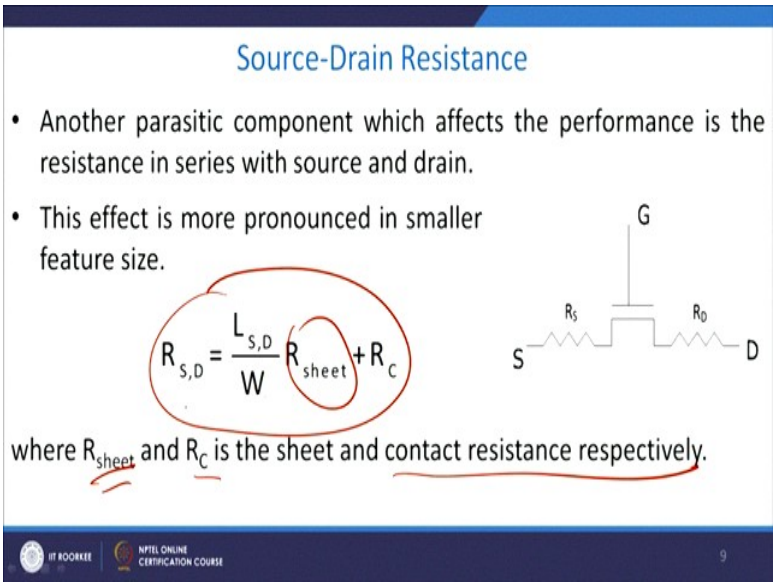

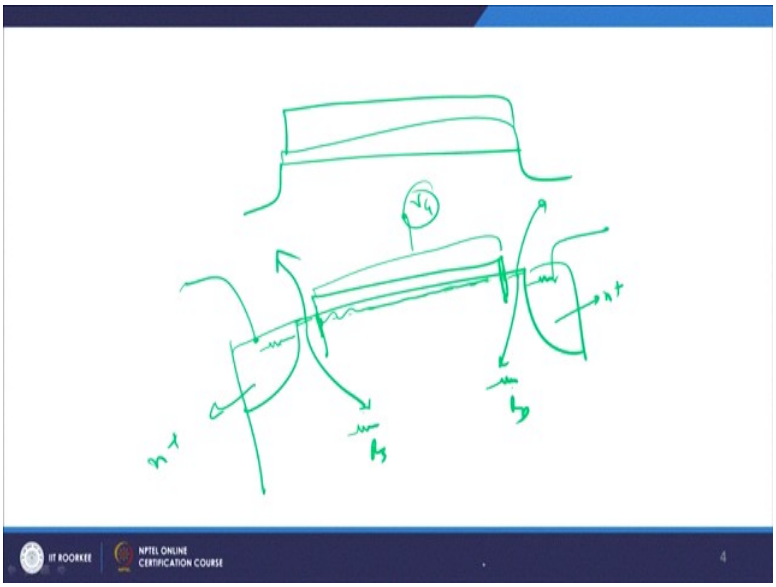

Now what happens is that when you have a MOS device and you do have a source and gate region and you have a source and drain region available with you and this is your source and, let us suppose these are not overlap devices and I have got source and drain, now then what happens is that or let me make it something like this, something like this, so you will have electric field or channel will be very largely from below these two points, which means that these two points will be still left.

So this is known as source resistance, this is also source resistance, drain resistance R_D and this is R_S, this assuming that you will have a contact here and assuming that you will also have a contact here, there will be some finite resistance here, some finite resistance here, even though this is N^+ and this is N^+, I can safely assume that there will be some finite resistance

howsoever small it is. That plus the C_B resistance gives you the value of R_S, this plus this series resistance on the drain side gives you the value of this thing and the reason you get R_S, R_D is that prima facia if you look very carefully here is the point where you apply gate voltage.

So the electric field is very large in the transverse direction between these two points, so the number of charge carriers are very large here, but the number of charge carriers here and here are very small because you do not have transverse direction electric field here and therefore the resistance offered by this arm and this arm is relatively very high. And that the reason you will see that you have R_S R_D which is the basically given by this thing.

So R_S R_D is given by L_S R_D and divided by W into R sheet + R_C, where R_C is defined as the contact resistances which is basically the resistances between the contact and the semiconductor and R sheet is the sheet resistance of the device that multiplied by L_{SD} by W gives you the total value of R_{SD}. You need not worry from where we are getting this formula or how this formula will be used. At this stage, it will be enough for you to understand that there will be some finite resistance between source and drain when the devices working either in saturation or in the non-linear region of operation.

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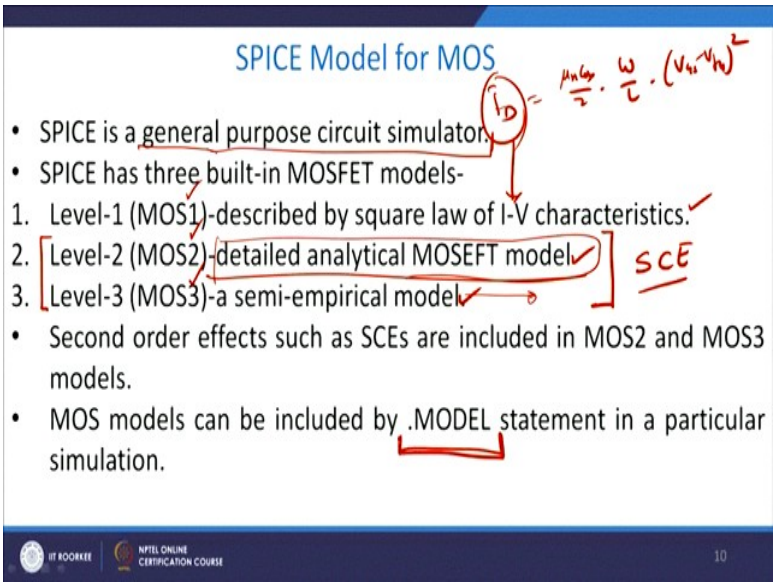

Let me come to the last part of our talk this time and this is basically the SPICE model for MOS devices and SPICE is basically a general purpose circuit simulator right. It is basically a general-purpose circuit simulator, it was built way back and it is still being used by many

colleges and in many industries also SPICE is being used by, for the purpose of circuit simulation purposes.

So it is basically a plug and play sort of a schematic entry, which means that you have these devices available with you, you just have to click it and place it on the schematic, schematic is the place, we will discuss this later on, but schematic is the place where you draw the circuit perse. So when you draw, drag-and-drop you actually are picking up the library of the device right, so all the equations related to the device are pulled from the library and placed with the device on the schematic and that is what is an important issue which you should keep in mind.

There are three models or the three levels of models which are available to us and this is level 1, level 2 and level 3 also referred to as MOS1, MOS2 and MOS3 respectively. The MOS1 is basically is on the I-V characteristics of the MOS device, so remember that square law term, where you had got V_{GS} - V_{TH} whole square, so μ_n, Coxide by 2 into W by L into $(V_{GS} - V_{TH})^2$, this is the square law for I_D, this is used as first law or MOS1.

A much more detailed analytical model of MOSFET is when used is MOS2 right, MOS2 model or level 2 model right. Another model which is being extracted from experimental data, also referred to semi-empirical model is used as model 3 or MOS3, now 2^{nd} and 3^{rd}, level 2 and level 3 takes care of short channel effects, level 1 is basically a long channel effect and therefore long channel model, which means you have applied gradual channel approximations and you do not have any short channel effect in level 1, but in level 2 and level 3 you have a large amount of short channel effects here right.

The MOS model, when you write a statement in the SPICE, the MOS model is included by putting a .MODEL statement in a particular simulation, so when you put .MODEL and then nMOS, then you write down its values and so on and so forth, you effectively bringing or the model file associated with a particular MOS device onto the schematic level and that is what we are actually looking into as far as SPICE model for MOS is concerned.

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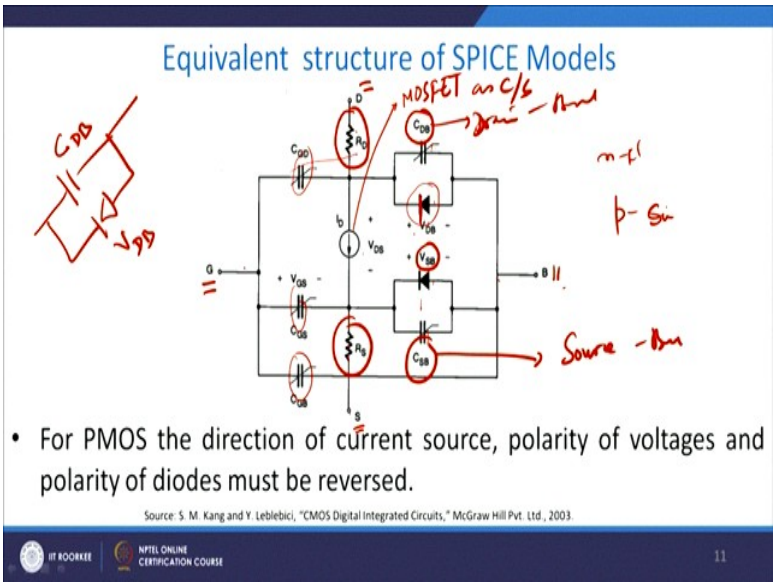

Now if you look at the equivalent circuit of a SPICE model, which means that how a SPICE looks at the MOS device then this is how it looks like its MOS device right and it looks something like this that you will have a drain resistance remember R_D, you also have a source resistance R_S. Again you have got four terminals: gate, drain, you have bulk and you have source right, so there are four terminals out of which these two takes care of R_S R_D, this I_D is nothing but MOSFET behaving like a current source as current source remember.

MOSFET is actually a current source, it is a basically a voltage controlled current source and therefore the voltage, where voltage, the gate side voltage is my voltage control current source and this gives you that resistance available here. If you remember C_{GD} gate to drain overlap, you have gate to bulk overlap and gate to source, so gate to source right, gate to bulk right, this is bulk and you have got gate to drain, so gate to drain overlap here right. If you look back on this side bulk and the gate side, remember you were saying that as I was discussing with you, you will always have a junction capacitance between the substrate and the base and that is what is happening right. You also I have between source and bulk sorry, this is source and bulk capacitance, source and bulk capacitance and this is basically a drain and bulk capacitance right.

Remember, please understand that it is basically a p-n junction diode. If you remembered it is basically a p-n junction diode and p-n junction will have P side towards the bulk side, if it is an N channel MOSFET right, if it is an N channel MOSFET because the bulk side is basically P type or P substrate and therefore you will have P side coming to bulk side and you

have this towards the N side, so this model of this and this takes care of the V_{DB}. This takes care of the reverse bias drain to bulk and this takes care of the reverse bias source to bulk right and therefore you see that you do have two diodes and you have two capacitances, which are variable capacitances in these cases and this is drain current and the drain voltage which is in front of you.

Of course, if you change the polarity or the type of bias the polarity of the diodes will also be reversed right. So for PMOS the direction of the current source, polarity of the voltages and the polarity of diodes must be reversed right.

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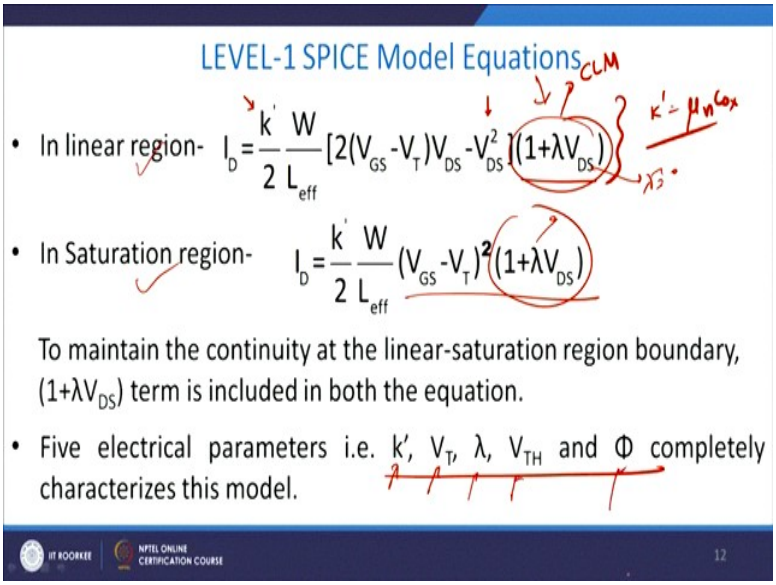

Let me come to model 1 SPICE model equations again, it is a linear model, we have already discuss this point, it is $1 + \lambda V_{DS}$, where λ is basically my CLM parameter and it also depends upon the value of V_{DS} K', K' is basically μ_n, K' in this case is basically μ_n Coxide, also referred to as a process trans-conductance parameter. In saturation we have already discussed it is K' by 2 W by L effective this much value, where λ is the now this thing. Now to include the continuity between linear and saturation region this $1 + \lambda V_{DS}$ is kept common right, in the linear region, maybe it will be true that λ will be approximately equals to 0 and therefore this will not play a role right. But this will play a role in the saturation region, so we have got five electrical characteristics and this completely characterises the model. So if I give you the value of this K', V_T, λ, V_{TH} and Phi, you will automatically be able to formulate this level 1 SPICE model in a much better manner right.

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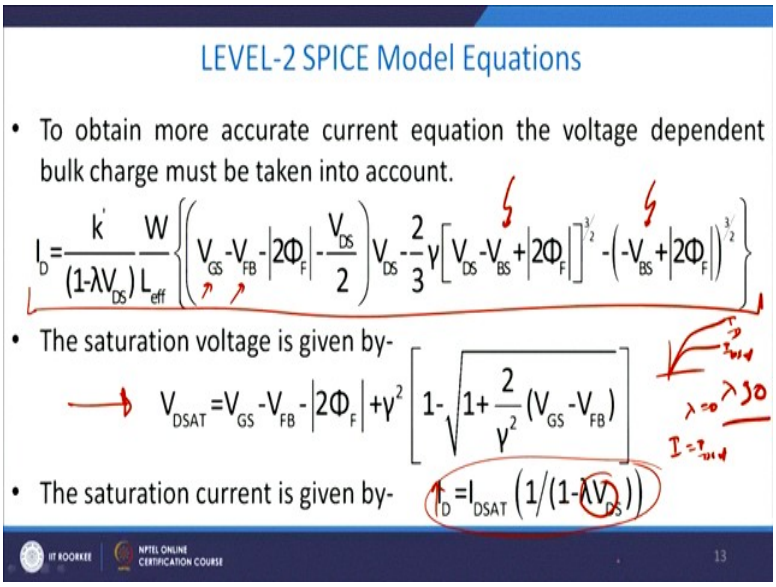

Let me come to SPICE level 2 model, where in this case, the voltage dependent bulk charge must also be taken into account right, because please understand the bulk charge varies with the applied voltages and depending on that people have found out a new equation given by this, big equation which is used in SPICE, do not worry but more importantly that you can see here is that you have V_{BS} coming into picture, which means that the substrate effect is being taken care of in SPICE level 2 model right. And you do have gate to source voltage, flat band voltage and so on and so forth.

The saturation voltage is given by this formula and I_D equals to $I_{D\,SAT}$ upon **1 - λV_{DS}**, **1 - λV_{DS}** equals to the saturation current. So if you see if **λ** equals to 0 that I get ID equals to $I_{D\,SAT}$ right, if **λ** is high-value, relatively high-value this quantity is high, 1 minus that quantity will be low and therefore I_D will be relatively high as compared to $I_{D\,SAT}$. And that is the reason you will always get a current which is something like this, so this is I_D and this is I_{DSAT}, I_D will be always larger than $I_{D\,SAT}$ for **λ** greater than 0, right and that is how it behaves like as a non-ideal current source.

Level 3 is basically empirical model, which means that I extract I-V from my data from experimental model and when try to fit the linear and nonlinear equations with those experimental model, we change it and see which is the line of best fit and that equation is basically known as the level 3 SPICE model.

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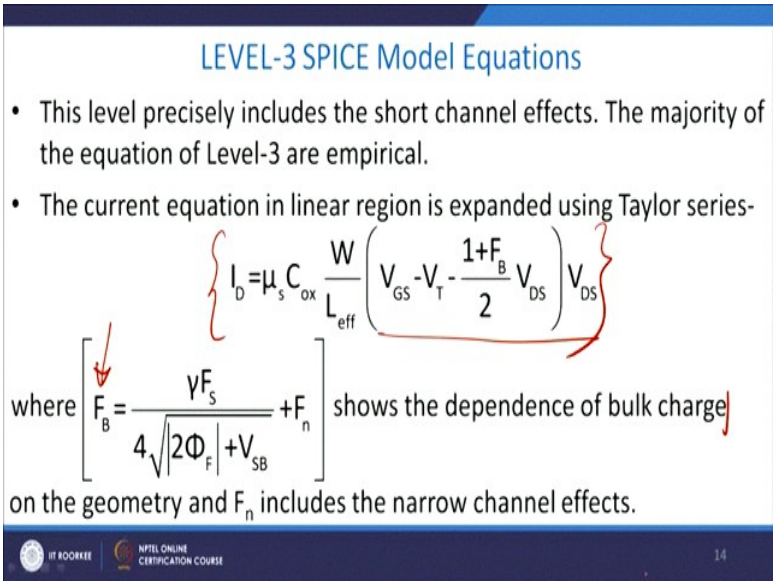

And it is given by this formula here, I_D equals to μ_SCoxide, W by L, this F_B is basically my geometry dependent idea and that varies with the level which is there. Most of the time we do not use level 3, most of the time for our practical purposes level I and level II is the most seldom used SPICE model file for our practical applications.

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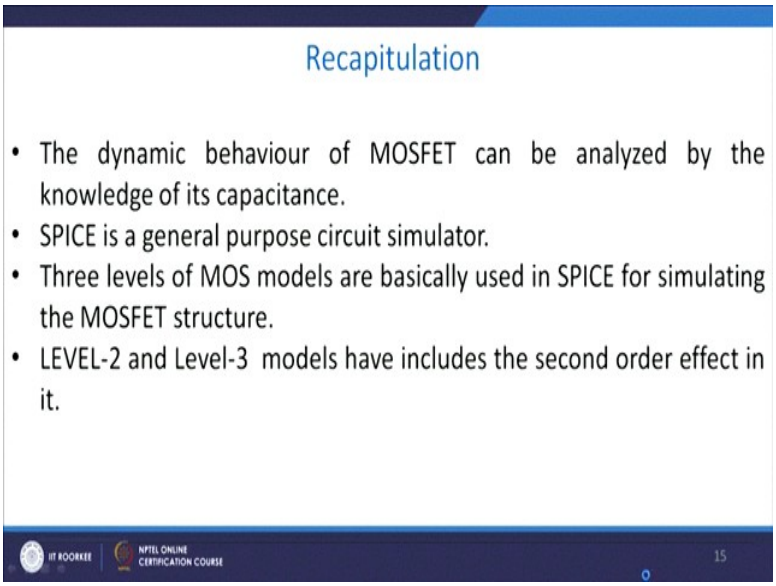

We come to the last part of our talk and let me recapitulate what we have done till now. We have understood that we have three types of analysis DC, AC and transient. When you do DC analysis capacitance do not play a role because they are open circuited, when they play a role when you have a AC analysis or transient analysis coming into picture. SPICE has been quite useful as a general purpose schematic simulator for a long time and we should therefore

know what MOS model files are used in the SPICE in order to simulate the current versus voltage characteristics. We saw there were three basic level files, there are many but for your understanding at the basics level, you have level 1, level 2, level 3, level 3 is much more of an empirical model, based on empirical model.

Level 1 is primarily a large your gradual channel approximation which means your lengths are typically large, level 2 takes care of V_{SB} which is a source to bulk and therefore substrate bulk mechanism and therefore short channel effects into consideration.

So level 2 and 3 takes care of short channel effects, level 1 may not take care of it. So with this, we have understood the basic fundamental principles of, basic ideas of SPICE model files at least and understood the requirement of capacitances and parasitic capacitances in this formula. I hope I have made much clear. Thank you very much and for your patient hearing.