Microelectronics: Devices to Circuits
Prof. Sudeb Dasgupta
Department of Electronics and Communication Engineering
Indian Institute of Technology Roorkee
Module 3
Lecture 15
MOS Transistor Basics-II

Alright, welcome to the NPTEL online certification course on Microelectronics: Devices to Circuits. We will be covering in this module as basic MOS transistor basics part 2. So in part 1, what we had looked into was how a MOS, what is basically a MOS device or a MOSFET and we have seen that in a MOSFET, we have it is basically a four terminal device but typically even if it is in three terminal, the source is generally grounded. We apply a drain bias, we also apply a gate bias and when the gate bias is above a threshold voltage, the channel is formed and the if you apply a drain bias, a current will flow.

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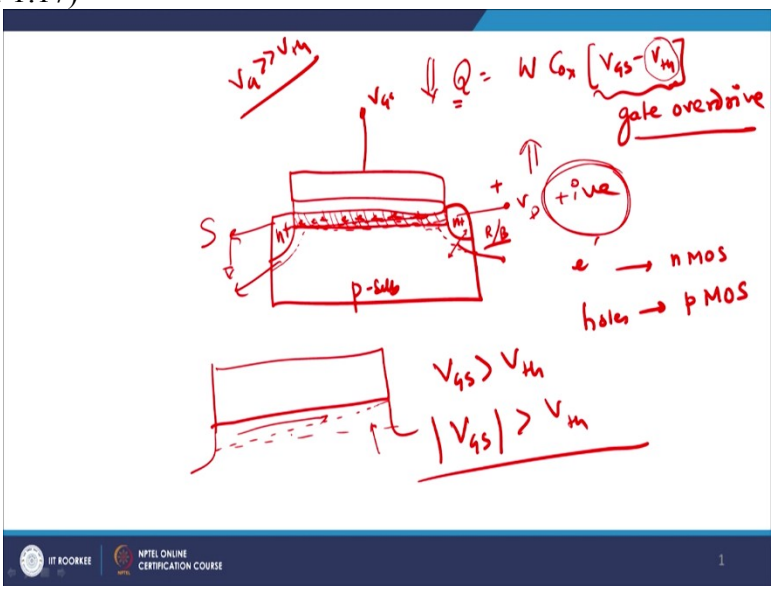

We have also seen that the width, that the total charge which is available is equals to W into C_{OX} into V_{GS} -V_{TH} which is, this is known as gate overdrive, right? So higher is the gate overdrive, larger is the charge accumulated which makes sense also because higher the value of V_{GS}, we have to subtract the threshold because that much amount of minimum voltage will be required to form the channel and excess of that will give you large amount of charge carriers.

We have also seen that when you have, when you have a gate voltage larger than the threshold voltage and your drain bias is 0, means you do not apply any drain bias, let us suppose I have N^+, N^+ and I have P type substrate right? I apply a gate bias here and this gate bias is getting larger than the threshold voltage of the device, so I told to you that there will be a charge carriers which will be coming here, right? So you have a large number of electrons which will be free electrons, which will be available here and there will be a depletion thickness here.

And there will be also a depletion region here. Fine? We have discussed this point earlier also that there will be a depletion region here and here. You will ask me from where these electrons are coming? They are being either supplied by the source side which is generally grounded or by drain which is generally, we apply a positive bias in case of an N channel MOSFET. Now if the charge carriers here are electron, we define this to be as an NMOSFET right? And if it is a holes, which is basically there, then we define that to be a pMOS right? PMOSFET or a pMOS.

So in case of N MOSFET as I discussed with you, gate voltage should be greater than threshold to achieve it whereas when you are applying a pMOS, gate voltage, mod of that should be greater than equals to threshold voltage of the device. Right? Which means that this is what we get from the basic configuration or idea. So but you see that when you do not apply any gate bias, this is perfectly like this. Right? It is exactly like straight line which means that the number of charge carriers per unit area is almost or the total number of charge carrier is almost constant as we move from source to drain.

It is perfectly symmetrical in nature. But as you go on increasing the positive bias, let us suppose you apply a positive bias and you go on increasing it, then you are actually increasing the depletion thickness because this is, this drain to substrate bias here is basically reverse bias and (there), because you are apply a positive voltage here. So when you go on increasing the positive voltage, the depletion thickness here becomes more and more. So it is becoming more and more. As a result, the thickness of the charge carriers right from source to drain, which was initially like this right, now becomes like this. Right? And this becomes like this.

So your depletion eats away into the channel and you have a reduced, and you have carriers which are just moving towards the source drain region. We will see its implications later on but

that is what we see from here. So what assumptions we take as far as this MOS device is concerned.

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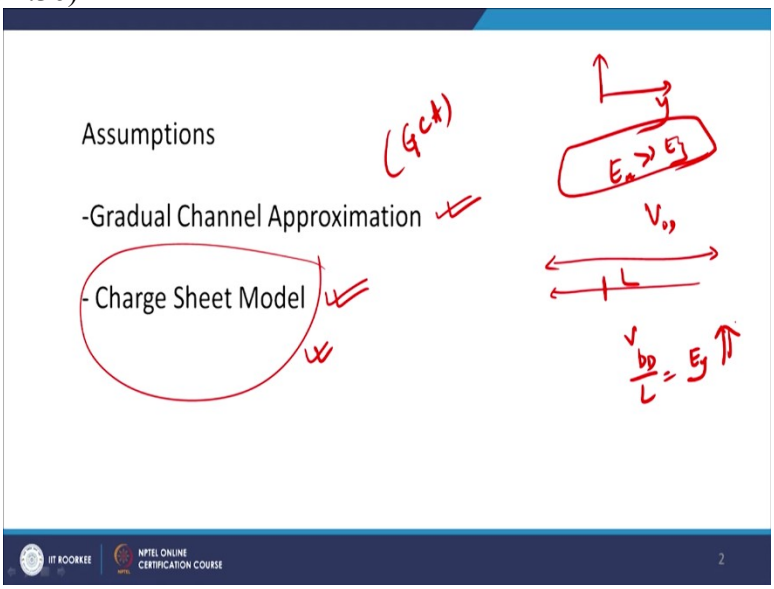

We assume that it is a, first of all we assume that it is a gradual channel approximation and then we assume that charge sheet model. What is gradual channel approximation? Gradual channel approximation tells me that the electric field in the transverse direction is slightly larger as compared to that in the longitudinal direction, right? So that is one. So basically a 1D Poisson equation will be enough to solve the gradual channel approximation based design. So all your long channel devices, MOS devices, you can apply gradual channel approximation wherein, we tell you that the electric field along transverse direction is relatively larger as compared to that along the longitudinal direction.

So if this is X and this is Y, then we say EX is relatively larger as compared to EY, right? And we can do one-dimensional Poisson equation solution to get these values. We also come to what is known as the charge sheet model which basically tells me that we assume that it is basically a sheet of charge near a silicon-silicon dioxide interface and therefore what is referred to as a charge sheet model. Right? Which means that it is basically a model which is assuming that it is a sheet of charge and therefore rather than per unit volume, it is basically per unit area that the charge will be collected with.

So we have two approximation, major approximations and the, one is known as gradual channel approximation, also referred to as GCA. Right and we have a charge sheet model here. Now please understand that you might not have gradual channel approximation when your channel dimensions are very very small. So if your lengths are very very small right, so it is okay to have if your length is very large, electric fields might be low. But if you reduce your channel lengths to very low values, then with the same value of V_{DD}, V_{DD} by L which is electric field in let us suppose the Y direction, is very high.

Then my basic assumption that EY, EX is much larger as compared to EY will not hold good and therefore, both will be approximately equal to each other and therefore GCA will not hold good. So GCAs are always holding good or always good when your channel lengths are typically very large in dimensions, right? Fine. And that is what we define as channel length saturation.

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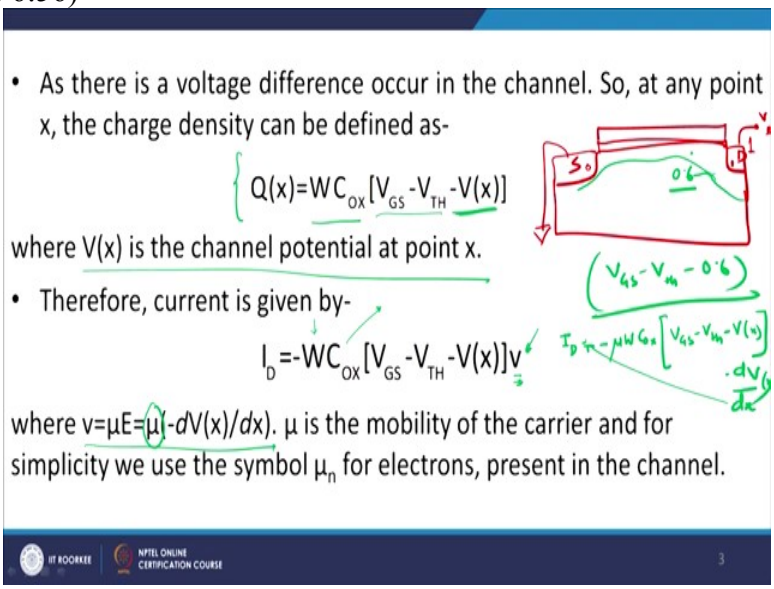

As there is a voltage, now what I do is, we have seen that when we do not apply any drain bias, the length of my or the thickness of my charge sheet of electron which is in this case the charge carriers are almost constant, is exactly constant from source to drain side, this is a thin layer which you see. Now if I apply a bias, let us see how does the whole scenario change. Now at any point, so let us suppose I apply a bias V_{DS}, so I have got this, I have got this, I have got a drain, I have got a source, V_G right, I have got a this and this.

I apply a drain bias here right, V_{DS}. What it will do is, since you apply 1 volts, so there will be a potential profile from 0 to 1. So somewhere here will be 0.5, here will be 0.6, here will be 0.2, here will be 0.4, so on and so forth. As a result, at this edge, you will have the most reverse bias. Is it okay? And as you move towards the source end, the reverse bias starts to reduce because the value of voltage starts to fall down right? And therefore reverse bias increases and therefore the depletion thickness also goes on reducing.

So you will have the maximum voltage thickness potential depletion thickness near the drain end and as a result I will just draw for you. So you will have the maximum voltage thickness, depletion thickness near the drain end and you will have let us see. You will have sorry, so you will have what? You will have largest depletion thickness here and then as you move towards the drain end, it will become thinner and thinner. So you will have a largest depletion region here because the voltage is maximum here.

Then we define Q of X. Q of X is minding the charge at any point X is equals to W into C_{OX} right for obvious reasons, into V_{GS} - V_{TH} - V_X. Why minus V_X? Because this is the voltage which is formed because of the charge carriers. So that has to be subtracted. So where V_X is the channel potential at any point X. So let us suppose that this point X, you have 0.6, 0.6. So you have to subtract V_{GS} - V_{TH} - 0.6. Why 0.6? Because 0.6 is just required to form the depletion region.

So subtract that to get the charge right? And therefore the current is given by minus W. Minus W into C oxide into voltage, applied voltage is V. Why minus W? Because of the simple reason that if the reason being that it is an electron. So the charge will be opposite in nature to the flow of electrons right. Alright, C oxide is the oxide capacitance per unit area of the device. Right? And as you can see here from this discussion that as the value of V_X goes on reducing, the current goes on increasing and so on and so forth.

So as you make a V larger, where V is the velocity of the charge carriers and is given as μ into E where μ is the mobility of the charge carriers and electric field is minus DV_X/DX, where V is the voltage at any particular point at this point. So I can replace this by what? I can replace this by I_D equals to this μ which you see from here, can be brought forward. So I can write down minus μ W C_{OX} right V_{GS} - V_{TH} - V_X right into DV_X/DX. Fine? Then what do you do? Then let us see how you go about it. You can then transfer DX on this side and let us see how it works out.

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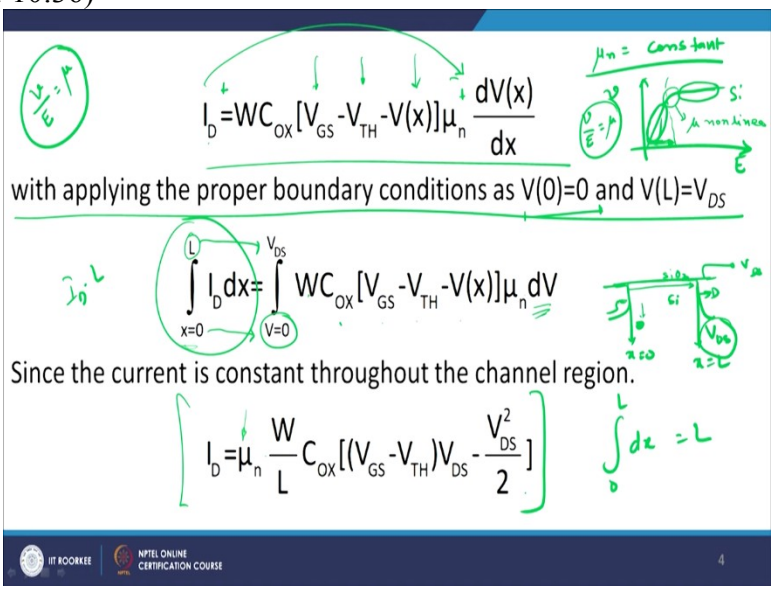

Now what you do? So you get I_D equals to therefore minus this thing. So this there was a minus sign here initially and there was a minus sign here, so there, that is the reason this become plus now. Right? So you see I_D therefore is equals to W into C_{OX} which is the oxide capacitance per unit area multiplied by V_{GS}, Gate to source voltage minus the threshold voltage of the device, V_{TH} minus V_X right because V_X is the channel potential multiplied by mobility or the charge carriers and we write DV_X/DX. Now we are assuming here, for all practical purposes, mobility of charge carriers to be constant. Right?

Now this is a bit, slightly over assumptions but for, at this stage of your understanding, assuming mobility to be constant is the right approach to find out the current. Now as you can see from this discussion, that how do you define mobility is basically velocity per unit electric field. That is how you define mobility right? So constant primarily means that and if you plot for silicon, if you plot for silicon velocity versus electric field for silicon, it looks something like this. Right? So this is the region where V by E is constant.

Similarly here is the region where V by E is constant. Right? Somewhere here, you have a non-linear mobility profile. So here it is non-linear. Right? But let us assume we are not going to that high electric field. You are restricting yourself to low electric fields and velocities are small and therefore I can safely assume that V by E is constant which is equals to the mobility. You also

should know at this stage before we move forward that mobility can also be of 2 types. One is known as the bulk mobility, another is known as surface mobility.

What is surface mobility? See, it is pretty simple to understand. Bulk mobility is when you have silicon right and you apply a bias, silicon is doped with say N type material, phosphorus, and you apply a bias and electron is moving through the bulk of silicon right. It is scattered by the atoms of silicon and so on and so forth. And it reaches to the drain end, and that is known as the bulk mobility. That velocity by electric field will be the bulk mobility. What is surface mobility?

Well, in reality when you talk about MOSFET, as I discussed with you in your previous discussions that in a MOSFET, the electrons will be moving if it is drain source and you apply a drain bias V_{DS}, then the electrons will be moving through this region right where this is basically your silicon dioxide and this is your silicon. So they will be moving across silicon-silicon dioxide interface. This interface is not very good because you will have large amount of traps, there will be some oxygen atoms which will be dangling and so on and so forth.

So there will be heavy scattering, unlike when the electron move through the bulk, as it moves through the surface, the scattering is very heavy. So when the electrons are very close to the interface of silicon-silicon dioxide, the mobility still falls down lower and therefore the current falls down because current is directly proportional to the mobility of the charge carriers right, as you can see from here. It is directly proportional to mobility. And the mobility falls down.

When the mobility falls down, the current also falls down but that is a second-order effect which will come later on. At this stage, it is sufficient to know that mobility is constant and this is how you can find the total current going through it. Now by applying the proper boundary conditions, so this is basically a differential equation and we require one, two boundary conditions to solve it. The first boundary condition is that we assume that at X equals to 0, V_0 equals to 0 and V_L is equals to L which means that at this point, this is X equals to 0 right and this is X equals to L.

At X equals to 0, the potential is assumed to be 0 and at this point, it is assumed to be V_{DS}. Right? Obviously because I am assuming that the potential drops within the source and the drain region is almost equals to 0. Because it is heavily doped, it is having $N^+ N^+$ region typically within it. It has got N^+ region typically within it and therefore I would not expect to see a large

potential drop in the source and drain region right. And therefore it is safe to assume that at X equal to 0, you will have a potential equals to 0 and at X equals to L, you will have potential equals to V_{DS} or drain to source voltage, whatever drain to source voltage you have applied.

Now what you do, you may take D_X, cross multiply. So I_D D_X and you integrate it from 0 to L right, where L is the length of the transistor. And similarly, V is from 0, so when X equals to 0, V was equals to 0. When X equals to L, V was equals to V_{DS} and you get W into $C_{OX}V_{GS}$ - V_{TH} - V_X μ_n into D_V. Fine. So when you integrate this one, this is straightforward. This becomes, so when you integrate this left-hand side, this becomes I_D into L right? Because 0 to L is nothing, so integral D_X 0 to L is nothing but L right and therefore that L is going to the denominator.

So I get W by L and this μ is already there, I bring it mu outside. This is C_{OX} and then what I do is, this μ L also comes in the front side because it is constant one independent of the value of V_{DS} and then if you solve integral D_V if you do with respect to V_{GS} - V_{TH} - V_X and from 0 to V_{DS} if you solve this, I get this equation here, right and it is equals to I_D equals to μ_n W by L C_{OX} V_{GS} - V_{TH} into V_{DS} into V_{DS}^2 by 2. Fine.

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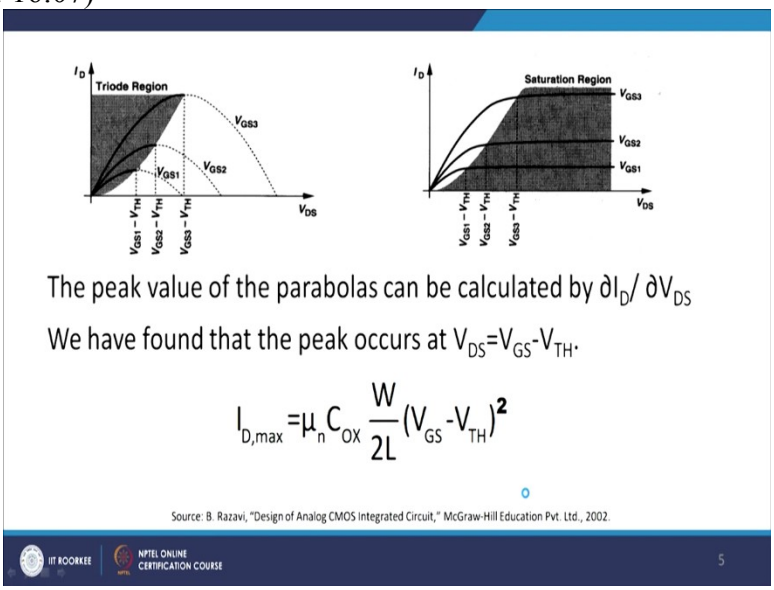

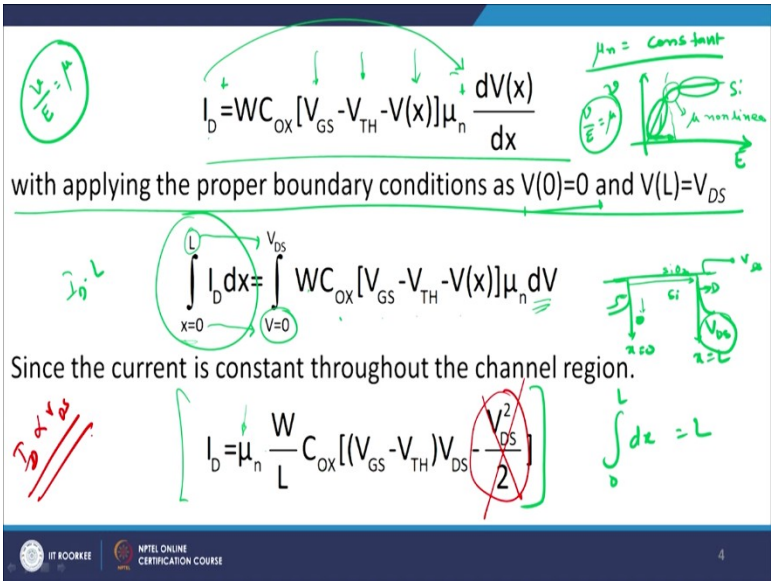

And this is the value of the current which you see in front of you. Now you see here, quite interestingly that now the drain current is not a linear function of I_{DS} right. It would have been so, had had this term would not have been there. Then I would have experienced that I_D is almost proportional to V_{DS} and therefore there would have been almost a linear increase.

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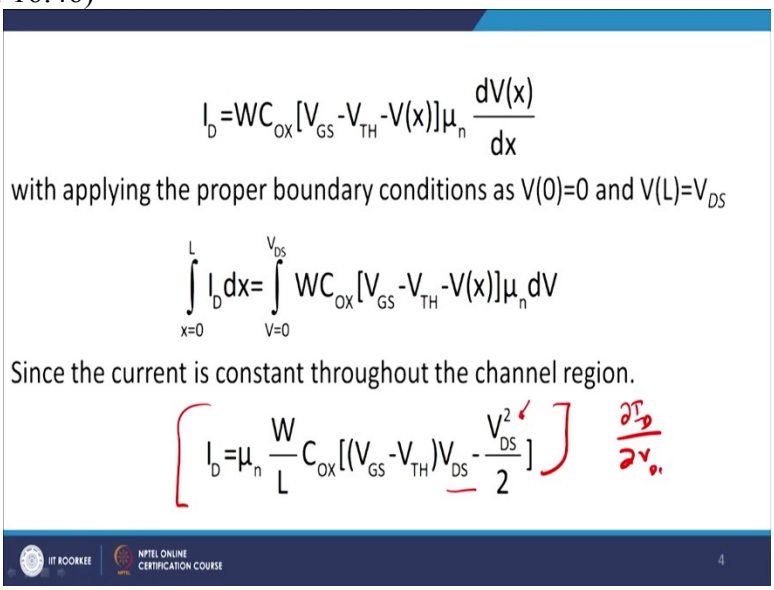

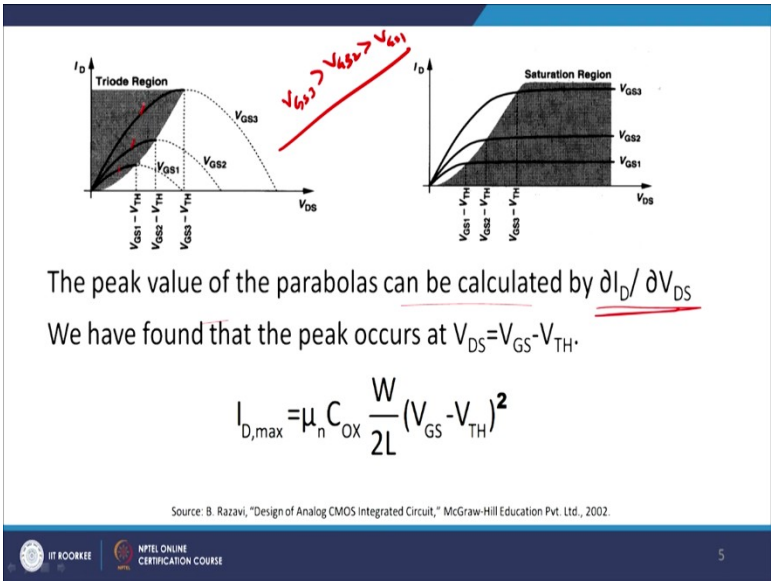

But since there is a presence right, since there is a presence and you do have a V_{DS} term coming into picture right, you do have a V_{DS} term coming into picture which is also V_{DS} here also you have got right and you have V_{DS} here also and this is V_{DS}^2 mind you.

So what I can safely say is that there will be a non-linear profile at smaller values of V_{DS}. Let us see how it works out. Now, so if you look at this basically the previous discussion, this is basically a parabolic equation and then if you find out a ∂I_D ∂V_{DS}, then you can find the peak of the parabola right. And this is what is, it can be calculated ∂I_D ∂V_{DS}. So once you differentiate it

for various values of V_{GS}, now if you plot I_D versus V_{DS} right, for various values of increasing V_{GS}, so V_{GS3} is greater than V_{GS2} is greater than V_{GS1} right.

If this is true, which means that the gate voltage is, as the gate voltage increases, you see the currents are also increasing and this is very simple because your over drives are increasing, see.

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$$I_D = WC_{OX}[V_{GS} - V_{TH} - V(x)]\mu_n \frac{dV(x)}{dx}$$

with applying the proper boundary conditions as V(0)=0 and V(L)=V_{DS}

$$\int_{x=0}^{L} I_D dx = \int_{V=0}^{V_{DS}} WC_{OX}[V_{GS} - V_{TH} - V(x)]\mu_n dV$$

Since the current is constant throughout the channel region.

$$I_D = \mu_n \frac{W}{L} C_{OX}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

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If V_{GS} is higher and higher, this quantity becomes higher and higher and therefore the current also increases.

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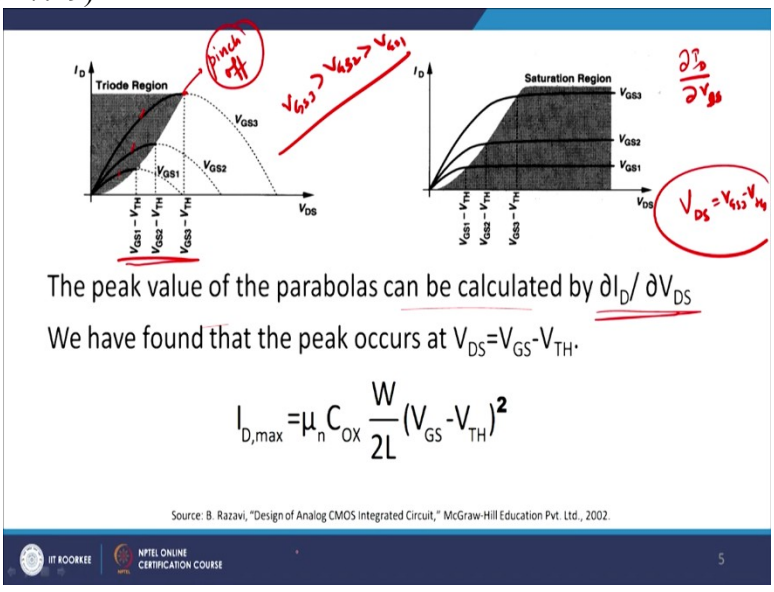

The peak value of the parabolas can be calculated by $\partial I_D / \partial V_{DS}$

We have found that the peak occurs at $V_{DS} = V_{GS} - V_{TH}$.

$$I_{D,max} = \mu_n C_{OX} \frac{W}{2L}(V_{GS} - V_{TH})^2$$

Source: B. Razavi, "Design of Analog CMOS Integrated Circuit," McGraw-Hill Education Pvt. Ltd., 2002.

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As you can see, therefore as the gate voltage increases, your, this value also increases. Not only that, your $\partial I_D \partial V_{GS}$ $\partial I_D \partial V_{GS}$ will, well $\partial I_D \partial V_{DS}$, sorry, will get drain to source voltage will also show a shift towards right for a higher gate voltage, which means that I will explain to you physically why is it. Mathematically, let us understand first. That once the drain to source, once the gate voltage is higher, you require a larger drain voltage to sort of, if you look very carefully from this region, this is the maximum value of current.

After this, either the current will fall, according to this equation the current will fall or it will remain constant. It will never increase for sure. Which means that charge carriers have attained its constant value. If this is true, then let us see why is it like physically. Physically, when you have reached the maximum value here, it primarily means that higher the value of V_{GS}, more is the transverse direction electric field, larger will be the number of carriers and therefore to deplete it, you require a larger drain to source voltage.

You are getting my point? And therefore this pinch off, this is also referred to as a pinch off point let us suppose. This is pinch off point let us, let me give a term here. This pinch off point goes on increasing right as the value of V_{GS} goes on increasing. So higher the value of V_{GS}, more will be the pinch off point, which means that if you see, if you look very carefully, this is the pinch off point which you get. That when you have V_{GS3} the pinch off, the value of V_{DS} right must be equals to V_{GS3} -V_{TH} at which it becomes maximum.

And the reason is very simple. I suppose you have understood by this time why is it very simple. The reason is being simple is that as you make the gate voltage higher and higher, you have now larger number of carriers available, that is the reason the current is higher but then, you therefore have to give a larger drain to source voltage to reverse bias the region and therefore make it depleted. And therefore the value of V_{DS} is also higher.

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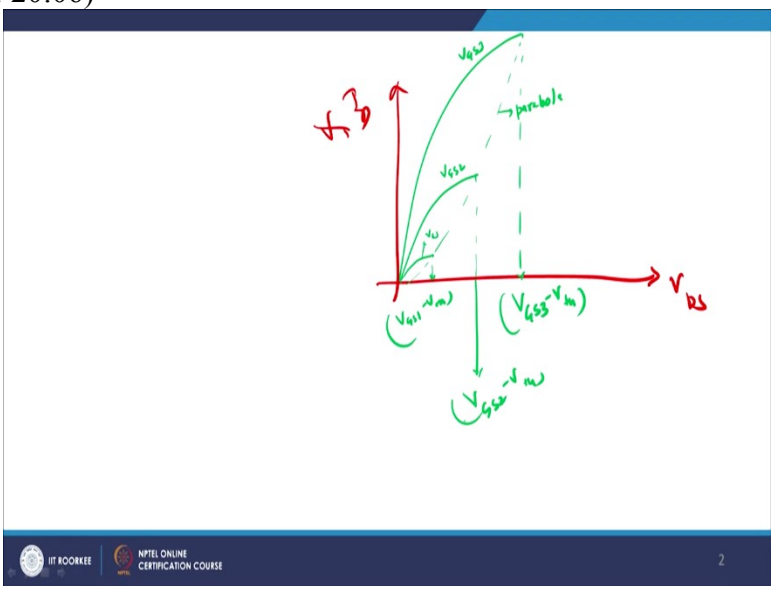

So what we finally get from this overall understanding is that if you plot I_D versus V_{DS} right at least till the point when you have reached it, you will get something like this. We will discuss this point, let me not draw at this stage, anything think like this but let me draw it. So let me draw like this and we keep it like this right? As we move V_{GS} higher right and when we move V_{GS} lower, it will be like. So if you plot it, this will be parabola. This will be V_{GS3} - V_{DS}, this will be V_{GS2} - V_{TH} and this will be V_{GS1} - V_{TH}, where this is the value of V_{GS1}, V_{GS2} and this is V_{GS3}. Fine. So higher the overdrive, more is the pinch off value of voltage which you see.

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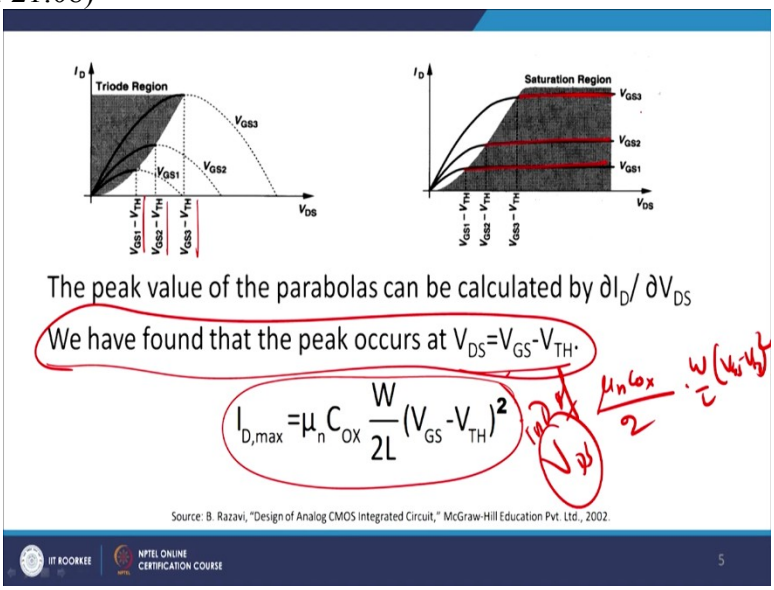

And that is what you see here at this particular point that so as you can see from all this discussion, this is the pinch off point, alright. So now we have found out that the peak occurs at V_{DS} equals to V_{GS} - V_{TH}. Right? So the peak occurs at V_{GS} - V_{TH}. Beyond this particular point right, if your peak occurs at this, you just feed this value into the previous equation and you automatically get I_D to be equals to this much. So I_D Max is μ_n C oxide right by 2 into W by L into $(V_{GS} - V_{TH})^2$.

And as you can see here, this is actually independent of V_{DS}. So this is independent of V_{DS}. As you can see therefore this region is defined as the saturation region. So we have saturated. So current is constant independent of the value of V_{DS} which you see. Right? And therefore it is constant for all larger values of V_{DS}.

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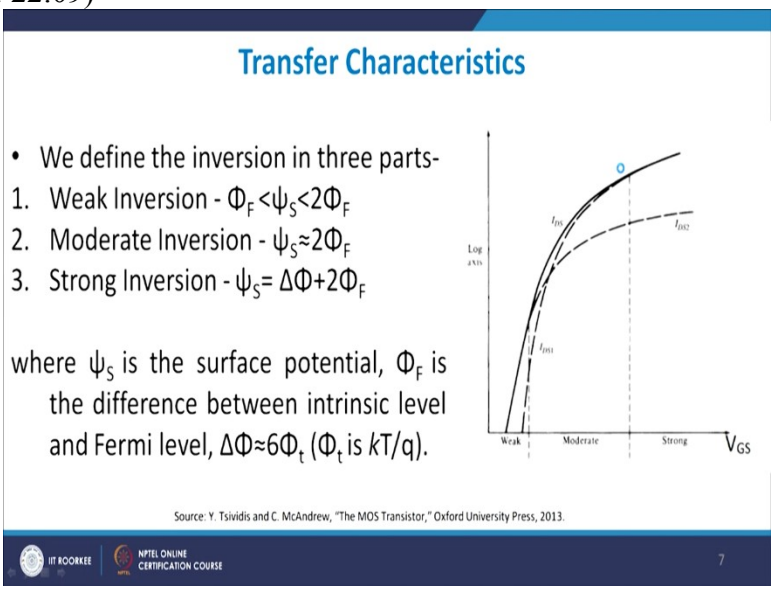

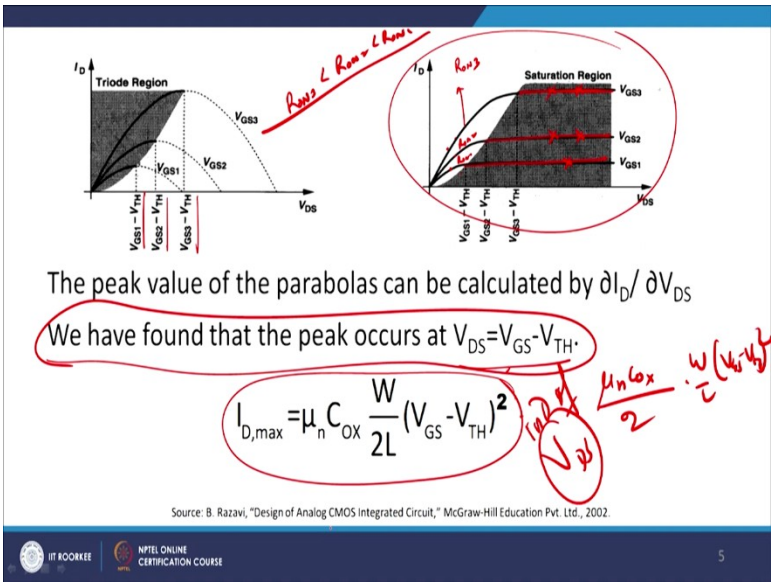

With this knowledge, let me come to three important characteristics of so this gives me, so what we have discussed till now is that we have discussed the IV characteristics of the device. And we have seen that if current versus voltage is plotted for a fixed value of V_G right, if this is what is plotted, then we get almost like this profile with us right. Then we almost get saturation region, this is the saturation region and this is the linear region, and so on and so forth. So at this point, the device behaves as a constant current source, this point it starts to behave like a resistor right and the value of resistance will go on changing as you move from this to this to this.

So higher the overdrive, lower is the resistance. I think it is clear to you why is it like that because higher the value of the overdrive, more will be the charge, more will be the charge, less will be the resistance right. And therefore this, suppose this is on resistance 3, this is R_{on2} and this is R_{on1}, then R_{on3} will be smaller than R_{on2} smaller than R_{on1}. Right? Because the slope is going on increasing as we move ahead and therefore the resistance is falling down because it is inverse of the slope which we are trying to find out.

With this knowledge we have actually understood the IV, or the current versus voltage characteristics of the device and we have understood the basic fundamental principles of current versus voltage. Now what we will do is that we will fix the value of V_{DS} and we will vary V_{GS} and see how does my current change, right? So that is what we are next, we are going to do and that is known as the transfer characteristics right. And that is known as transfer characteristics.

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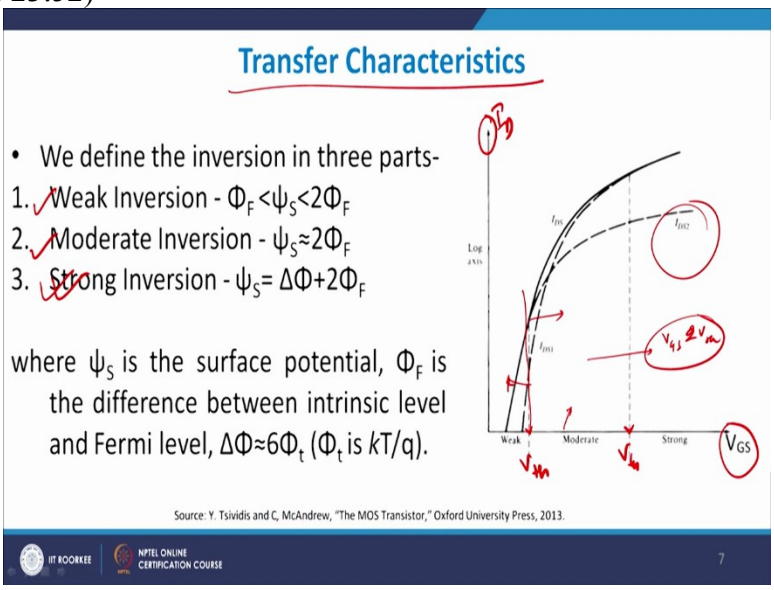

So what is the meaning of transfer? It is basically I_D. This is I_D versus V_{GS}. We will not go into details of this one. I will make it very simple for you to understand and we will discuss further than this. See as I discussed with you that when the gate voltage is much smaller than threshold voltage, the device will be in the off state because the threshold voltage because there are no large number of charge carriers available in the device and as a result device will be considered off state.

When the gate voltage crosses the threshold voltage, you will have large number of charge carriers in the silicon-silicon dioxide interface and as a result, you will have an on state available with you. Now, typically, if you look at this graph here, we define this to be as whenever the gate voltage, so this is my threshold voltage. Whenever my gate voltage crosses the threshold voltage V_{TH} right, I can get, sorry, this is my threshold voltage, I am sorry, this is my threshold voltage. Whenever my gate voltage crosses the threshold voltage on the right-hand side, I get a moderate inversion.

Whenever my gate voltage crosses twice V_{TH} or large values, I get strong inversion and anything smaller than this, we get a anything gate voltage smaller than the threshold voltage, we defined that to be as a weak inversion. So we have three points of notation. One is known as the weak inversion, one is known as moderate inversion and we have a strong inversion. Strong inversion primarily means that, inversion means it has become, it is just becoming N type and it was initially P type.

Strong inversion means, if it is becoming twice the, twice, so let us suppose you had a P type substrate where the number of holes were hundred right. Now what you do? You go on adding, you apply a negative bias, so electrons are being pulled, they are recombining and then holes are fully removed, fully depleted. So there are no holes now. We have only depletion available. Now what you do? You still go on increasing the gate voltage, more number of electrons are pulled there and it crosses equal to hundred. Then we define it to be inversion.

So now what has happened is, as many holes were initially present, that many number of electrons are now present. Right? If it is almost double of that electron, we define that to be as a strong inversion, right? So I have a weak inversion, moderate inversion and strong inversion.

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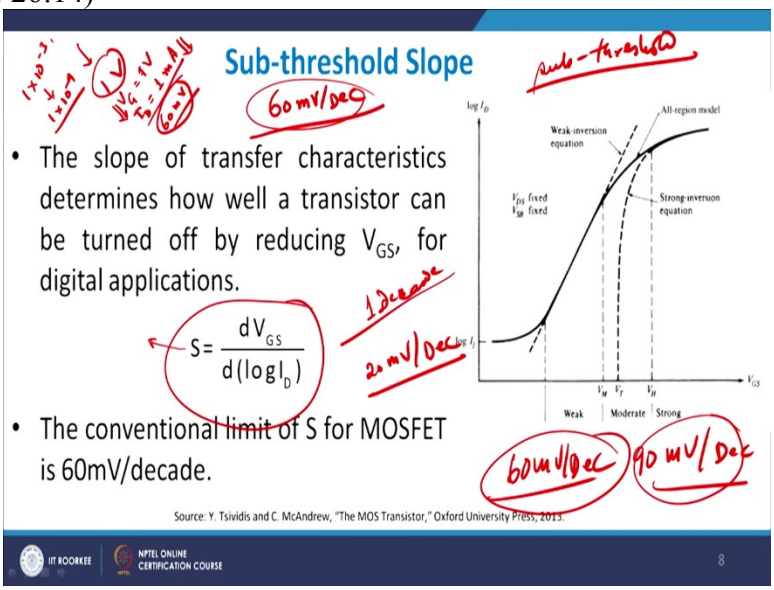

We define a, sorry, we define a new term here and that is known as a sub-threshold slope. A very important term in both analog as well as in digital world, especially in digital world where switching is to be done. See what happens is that though we presume that our gate voltage is equal to threshold voltage is a transition point between on and off state, in reality, this is not true which means that even when the gate voltage is even just smaller than threshold voltage, the device is not fully off right? The device is not fully off which means that there are certain, still some charge carriers left which has not been removed.

And therefore we define that region to be as the sub-threshold region. Means just smaller than threshold. Right? In that case, we define a term known as S, also known as sub-threshold slope as the amount of gate voltage required to change the drain current by at least one decade which means that, let us suppose your threshold voltage was 1 volt, right? You applied the gate voltage and the gate voltage is approximately equals to 1 volt. Now what subthreshold slope tells me is that at 1, when the gate voltage was 1 volt let us suppose right, when the gate 1 volt, the drain current which was flowing was let us suppose 1 milliamp, just for information sake.

Now what I do? I decrease the gate voltage by say 60 millivolts, right? And if then the I_D value, if this gate voltage reduces by 60 millivolts, if I_D drops by one decade, one decade means from one milli, one milli is 1 into 10^{-3} and it drops to 1 into 10^{-4}, 1 decade drop in current and to do that if I

require that let us suppose 60 millivolts of gate voltage change, then we define 60 millivolt to be as the sub-threshold slope. And it is given, and the unit is given as 60 millivolt per decade.

So for one, for every one decade fall in the current, drain current, the amount of gate voltage which is supposed to be changed, in order to bring that change of the drain current is defined as my sub-threshold slope. Smaller the value, faster is your change. I hope you understand. Let us suppose, I have a device which gives me 20 millivolt per decade, it means that I have to only apply a 20 millivolt gate voltage change in order to 1 decade drop. So switching is faster.

So sub-threshold slope is basically means that that it is switching is faster. Lower the value, lower is the switching. So if sub-threshold slope is 90 millivolt per decade and I have a design which is basically 60 millivolt per decade, then 90 millivolt per decade then 60 millivolt per decade is a kind of much faster switching from on to off and off to on as compared to 90 millivolt per decade. Right? The conventional limit for sub-threshold slope is 60 millivolt per decade. That is the conventional limit. At T equals to 300 Kelvin, we define this to be as a conventional voltage.

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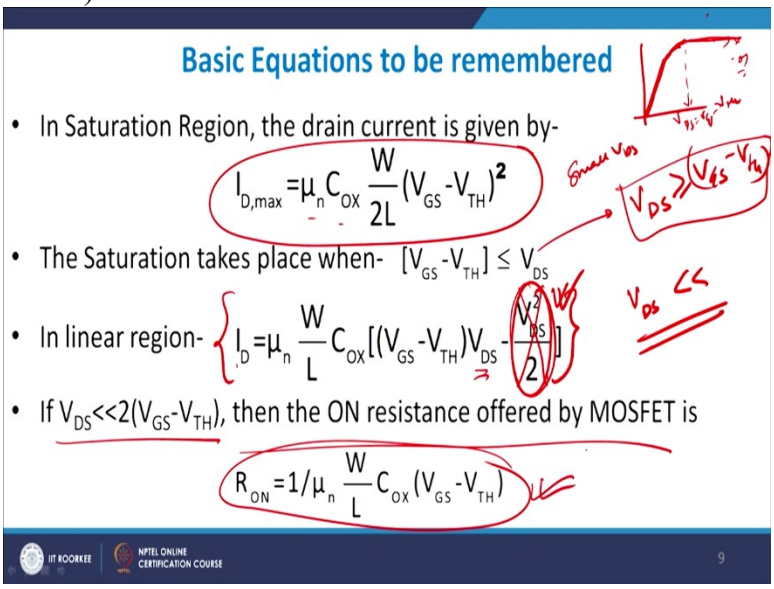

With this knowledge, let me recapitulate the basic equations which is to, which you have to remember from next time onwards to make it easier for you to understand, the first thing in the saturation region, the drain current is given by I_{DMax} and that is a maximum current, is given as μ_n

C oxide W by 2L into $(V_{GS} - V_{TH})^2$ which means that if your $V_{GS} - V_{TH}$ is doubled, your current will be becoming almost 4 times with you and that is one of the major but here if you see clearly, it is independent of V_{DS}.

So I_D is independent of V_{DS} primarily meaning that I_D is almost constant. Right? It is almost constant independent of V_{DS}. What is the condition for saturation? The condition for saturation is this one which is V_{DS} should be greater than equals to $V_{GS} - V_{TH}$. Very very important term from digital as well as analog point of view and we should know what is the condition for the onset of saturation. For onset of saturation, V_{DS} should be greater than equals to $V_{GS} - V_{TH}$, which means that drain to source voltage should be larger than the overdrive of the device.

In the linear region, we define this as my drain current source. As I told to you, if your and let me say that V_{DS} is very very small, a very small value, then V_{DS} square will be still smaller and I can neglect this and then I can have I_D proportional to V_{DS}. That is the linear region of operation, right? So whenever you have linear region of operation is this one right when your V_{DS} is very very small. In that case, V_{DS}^2 will be also must so is V_{DS} is 0.2, 0.2 square is 0.04, right? So 0.04 is very small quantity, I can afford to neglect it.

But anything larger than 1, for example 0.3, say you use 0.3, 0.3 into 0.9, it will be also very small. So for small values of V_{DS}, small V_{DS}, this is almost linear because I_D is directly proportional to V_{DS}. As you move your V_{DS} slightly higher than 1 and makes it, this non-linearity comes into picture. And you do have a non-linear region here. Till how much point? Till V_{DS} equals to $V_{GS} - V_{TH}$, the onset of saturation. After this, it becomes straight, almost straight line.

So I will, I have a saturation, non-linear and exactly linear in dimensions, right? When V_{DS} is much smaller than 2 times $V_{GS} - V_{TH}$, the on resistance offered by the device is given by this formula that R on his equals to 1 by $\mu_n W$ by L C_{OX} $(V_{GS} - V_{TH})$. And this gives you a small R_{on} in this case. So with this, let me recapitulate what we did.

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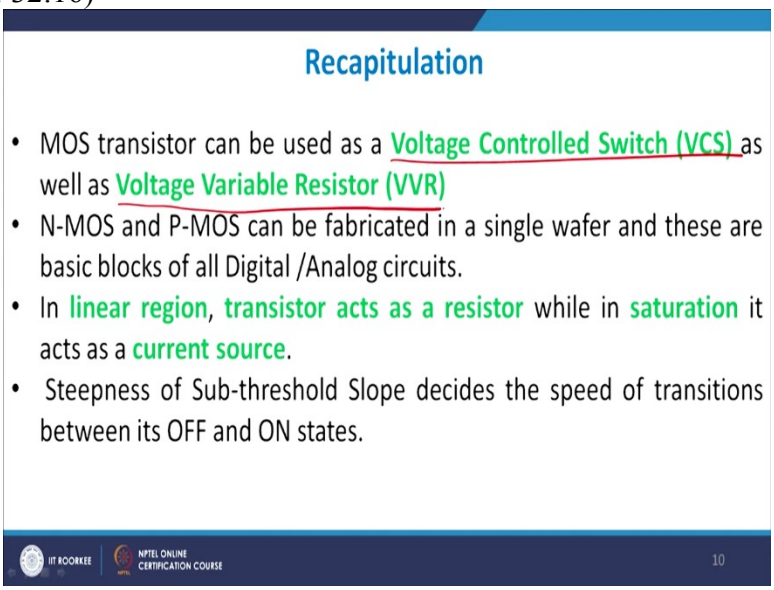

We have also understood that it is basically a voltage controlled switch, MOS device. Who is controlling? The gate voltage is controlling it as a switch. So I can apply a gate voltage rather than threshold to switch it on, less than threshold to switch it off. It is also acting as a voltage variable resistor because if you see, as I discussed with you, for a lower value of V_{GS} in the linear region, when the lower value of V_{GS}, R_{on} is large and as you increase the value of V_{GS}, R_{on} reduces. So I can use it as a voltage variable resistor as in JFET.

Now typically, nMOSFETs and pMOSFETs can be fabricated in a single wafer and these are the basic building blocks of digital and analog circuits which is a very simple one. Of course, as I discussed with you, in linear region, the transistor acts as a resistor while in saturation it acts as a current source. So therefore MOSFETs you can see even without understanding anything, it can act as a resistor as well as a current source right and therefore the lower the, what is the sub-threshold slope? Sub-threshold slope is defined as the amount of change in the gate voltage to change one decade of drain current right. Lower the value, better the speed of the device is in switching right.

So with this, we have finished with the basic concepts of MOS device and we have understood how a MOS device works. We have also understood the basic functionality of a MOS structure and its uses as a current source as well as a voltage variable resistor. We have understood three

regions of operation, linear, non-linear and saturation. We have also appreciated what is the value of V_{DS} at which you will have onset of saturation. Right? And this will be quite interesting and important for our subsequent studies. I thank you for your patient hearing. We will take up the next issue of MOS devices in the later courses. Thank you!