Microelectronics: Devices to Circuits
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Module 3: Microelectronics: Devices to Circuits
Lecture 11: Simple BJT Inverter and Second Order Effects

Hello everybody, and welcome to the NPTEL online certification course on Microelectronics: Devices to Circuits. In our previous interactions, we have actually seen the functioning of BJT, various modes of operation of a bipolar transistor and then we have seen BJT as an amplifier, right? So given a small input signal how can I actually achieve amplification in a voltage domain as well as in current domain of course. We have seen that in our previous discussion.

We have also seen the three modes of operation of BJT which is common emitter, common base and common collector. And we have appreciated what is the utility of these three modes of operations of bipolar transistor. What we will be doing as the last part of the bipolar before we move to CMOS technology is look to BJT as an inverter, because that is the basic logic which we tried to design initially. So we will look at BJT inverter and then we will look into the various second order effects of an inverter right? Second order effects of bipolar transistors, right?

One we have already dealt earlier but in details we will be dealing it now, what is the early effect? But before we move ahead with that, let me first discuss with you a simple BJT inverter, right? So the topic of this slide, the topic of this section is basically your BJT, simple BJT inverter and second order effects, right? So this is the topic of this lecture series talk. So what will we be covering here? We will be covering, covering basic simple BJT inverter. So given a BJT inverter, can we find out the inverter characteristics of a BJT and use it for logic inversion purposes? That is what we will be seeing here.

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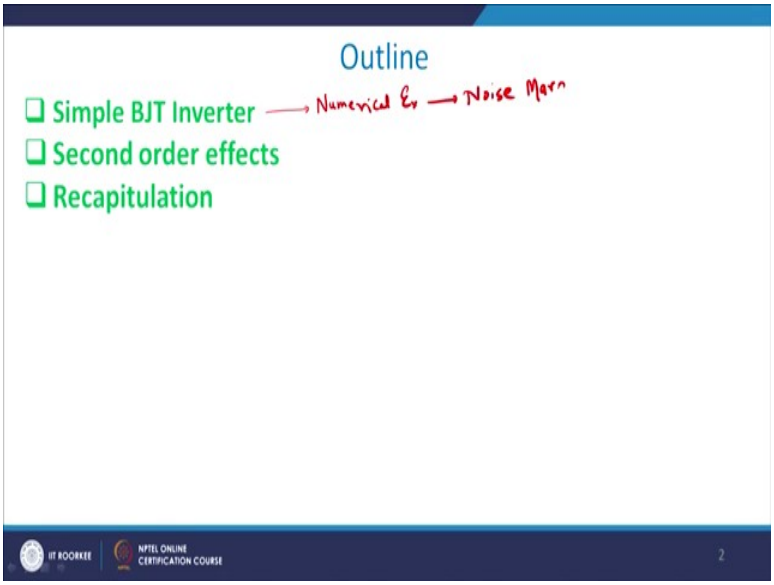

Maybe we will solve a numerical example in this case. I will show you a numerical example right? Numerical example. And we will also concentrate on what are known as noise margins for BJT, right? So, we will also discuss this in detail when we go to CMOS logic. But for BJT logic we will also understand what is noise margin and how do you define noise margin in a BJT. And this will be through a numerical example setup here. Then subsequently we will be going for other second order effects of BJT where we will be looking at base widening, then we will be looking at early effect and so on and so forth. And then how does it influence therefore the *I-V* characteristics of a BJT, right?

That will take care of approximately the major understanding portion of BJT and therefore knowing this, you can actually approach BJT from analog point of view when you use it as an amplifier and you can also approach it from a digital point of view when you use it as an inverter, right? So this is what we will be... So that is the reason or the logic for having this bipolar transistor as the first, first part of this new lecture series on NPTEL.

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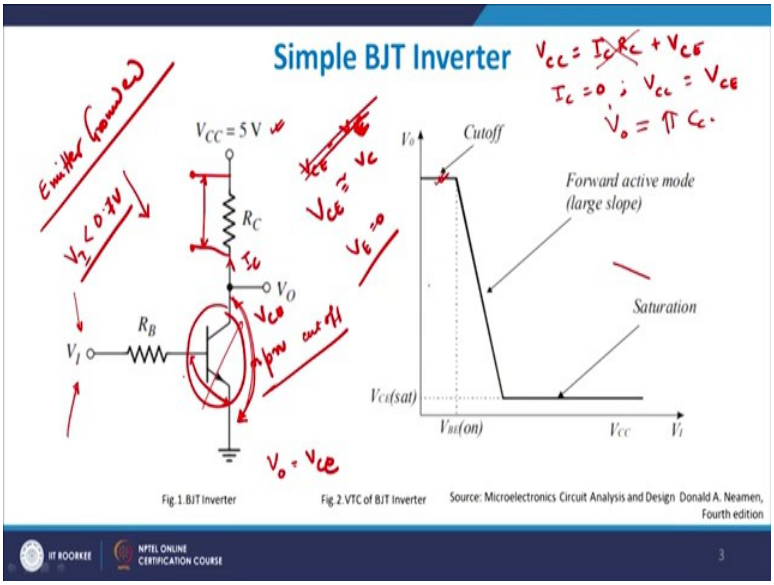

With the knowledge you have gained now, let me just show you a simple BJT inverter. As you can see, the simple BJT inverter is this which you can see here. And this is a BJT which is an NPN transistor, so I have an NPN transistor here whose emitter is grounded. So this is basically an emitter, emitter grounded inverter, inverter. And we apply a voltage input to the base through a base resistance R_B and we try to extract the output voltage from a collector of the BJT. And you apply your voltage V_{CC} which is equal to 5 Volts here, right?

So this is the basic principle. We have already seen it earlier, now we will look into the details from the voltage transfer characteristics point of view. So as you can see therefore, when your input is typically very low, right? It is much smaller than 0.1 then we can, sorry, when V_I is much smaller than 0.7 Volts which is the turn-on voltage for this base emitter junction, right? You would expect to see that, this, this is cut off. NPN will be in cut-off and as a result, what will happen is that this V_O will be exactly equal to 5 Volts, right?

Why? Because if you... we had discussed this earlier also that we can write down V_{CC} to be equal to $I_C R_C$ plus V_{CE}, right? This is V_{CE}. This one is V_{CE}, right? And, this is, I_C is flowing, let us suppose, here. So, $I_C R_C$ is the voltage drop across this resistor. This, this is $I_C R_C$. This voltage drop plus this voltage drop must be equal to V_{CC}. But you see, since your emitter is not through a resistor, it is directly coupled to the ground, V_{CE} can also be written as simply V_C.

So V_{CE} is nothing but the collector, your sorry V_E, I am sorry V_E. I am sorry, I am sorry. V_{CE} can be exactly written as V_C because V_E is actually equals to 0, right, because emitter is grounded. But keeping this in mind therefore, when your device is in the cut-off state, when this is cut-off, NPN is cut off I_C is equal to 0. I_C equals to 0 implies that your V_{CC} is equals to V_{CE}, right? Because I_C equal to 0 means this is 0 and therefore V_{CC} equals to $I_{CE,}$ right?

And therefore, you can safely assume that what you can see from all this discussion is that if you try to find out the value of V_{out}, V_{out} will be equal to, will be nothing but this V_{CE}, right? V_{out} is equal to V_{CC}, right? Now, when my I_C equals to 0, right? V_{CC} equals to I_CR_C plus V_{CE}. When my I_C equals to 0, this goes off, right? And therefore, the voltage across this thing is pretty large, right? It is pretty large because all the voltage drop will be across. So this is cut-off, sorry so this is cut-off and therefore, I will get V_0 to be equal to a high value, equal to V_{CC} and you get a large value here. So when the device is in the cut-off mode, your voltages are all going to 0.

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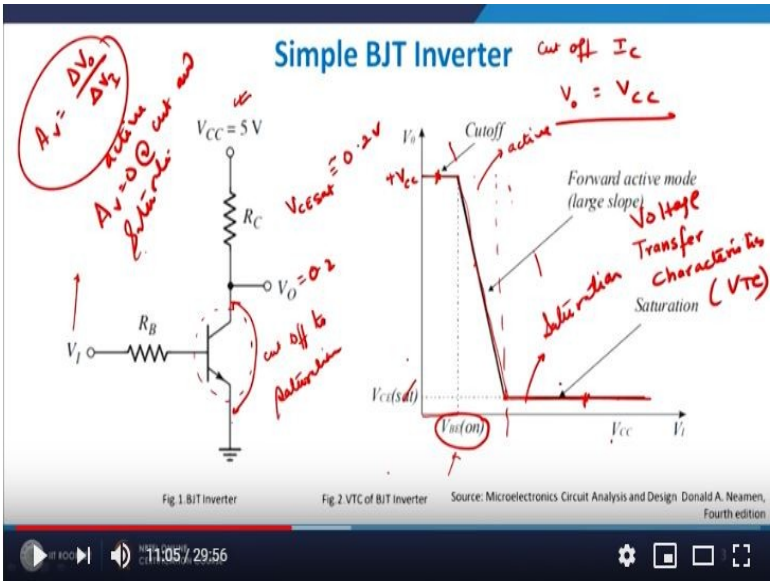

And as a result what will happen is, that therefore when your device is in cut-off mode, right? I_C equals to 0 implying that your output voltage is approximately equal to V_{CC}. So if you are using a plus 5 Volt V_{CC}, I will get this to be as equal to plus 5 Volts, right? Plus V_{CC}. Now as you go on increasing the value of V_I from a low value to a high value, you switch on the device drastically. And when you switch it on, what happens is that this becomes from cut-off to, cut-off to, it goes to saturation.

Why saturation? Because the voltages are not large enough in order to ensure that these have moved fully into. When, this is when it moves to cut-off, this V_{CE} can be written as V_{CE} can be written as V_{CESat}, saturated V_{CE} which is approximately equal to 0.2 Volts which means that this is the value of voltage which you get as 0.2 Volts. At V_{out} equals to 0.2. So we have understood one basic fundamental principle that whenever my input voltage is low, my output voltage is high and vice-versa. So I can use it as an inverter.

As we have also discussed an earlier part that below V_{BE}. So you see if you look at this curve and this is V_I versus V_O. So this is basically your voltage transfer characteristics, right? This is known as *VTC* or characteristics. And this is known as voltage transfer characteristics, voltage transfer also referred to as *VTC*, right? So if you look at the *VTC*, right, it is just behaving like an inverter. Because when your input is V_{BE} (on) till that much point, till that much point your device is cut-off and the voltage is latched to V_{CC}.

Beyond V_{BE} (on), the devices switches and the voltage starts to fall down. It falls down to how much value? Equals to V_{CEsat} and in this region V_{CEsat}. After this if you even increase the value of V_I, it does not affect because the device is fully on. So you see, this region, this region is defined as my active region. And this region is defined as my saturation region, right? So I have got cut-off region, active region and saturation region. The active region is a region where the voltage V_0 is a function of V_I and therefore there is a finite A_V or the voltage gain because A_V will be defined as $\partial V_0 \, \partial V_I$.

Therefore, I will have a finite gain in the active region, right? But I will have A_V equals to 0 at cut-off and saturation. At these two places, my voltage gain will be 0. So if you want to bias my device as an amplifier, you bias it in the active region of the device. If you want to bias it as a switch then make your active region as small as possible and try to shift from cut-off from here to here, right? And you can get a digital 1 and digital 0 in the output and input side, right?

So, basic BJT therefore, we had a problem that the BJT is though it is pretty fast in terms of switching, but the problem is that it has got a high power dissipation because of high leakages. Not only that, BJT also has a problem that to move it from saturation to cut-off, right, you have to actually remove large number of charge carriers from the saturation region, right? To make it to go into cut-off.

So, there is some dead-time also associated with the BJT switching action. Which means that the BJT has to wait minimum amount of that much amount of time before it crosses from saturation to cut-off, right? And therefore the speeds are relatively low for BJT when it acts as a switch, right? So the maximum frequency operations are relatively low in this case as compared to the previous cases, as compared to CMOS technologies per se.

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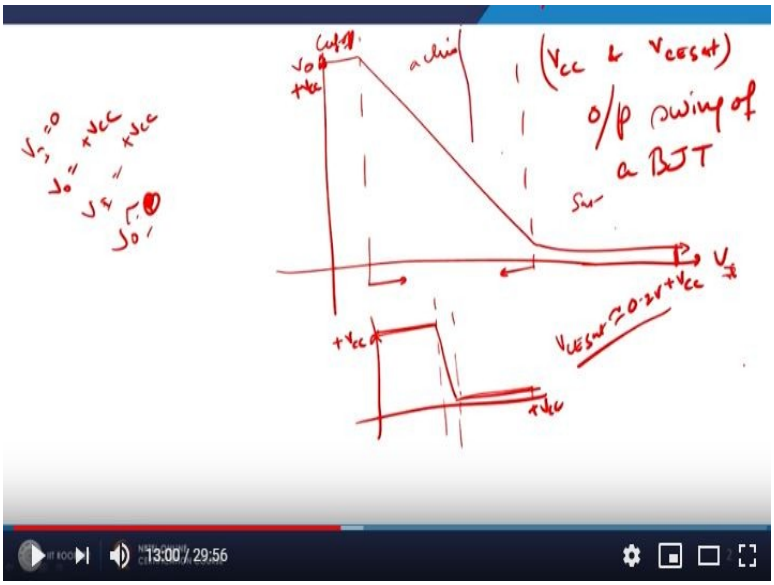

As you can see here, therefore, if I want to therefore make my transistor work in the saturation region, the active region then try to make the active region as large as possible and then this is my active region, right? And this is my active region and this is my saturation and this is my active, right? And this is cut-off, fine? And this is V_O versus V_I. Now if you want to reduce the active region, you need to bring these two points close to each other. Which means that if I want to reduce it, it is something like this, right?

So your active region has drastically reduced here. So the gain which you get is that your cut-off region is now very large and your saturation region is also very large. Because if you remember, this will be actually equal to $+V_{CC}$. This point is $+V_{CC}$. Output will be equal to $+V_{CC}$ approximately if your input is equal to 0. So when your input, so when V_I equals to 0, V_{out} will be equal to $+V_{CC}$ and that is what is written here. And when V_I equals to $+V_{CC}$, V_O will be equal to 0, approximately equal to 0.

So at this point when it is $+V_{CC}$, when V_I equals to $+V_{CC}$. Let us suppose here $+V_{CC}$, then output actually falls to 0 value or very close to 0 value; typically equals to V_{CEsat} actually which is approximately equal to 0.2 Volts. Fine? So we have learnt one important point that though BJT is a good thing but a good switching action but the point is that it cannot go below V_{CEsat} in the lower dimension and the highest one, it can of course go to V_{CC}.

So the swing is restricted between V_{CC} and V_{CEsat}. This is the output swing, output swing of a bipolar junction transistor, right? So this is what you have learnt, what you have learnt here. We will define some important terms here and that will be making it much easier for you to understand or appreciate that.

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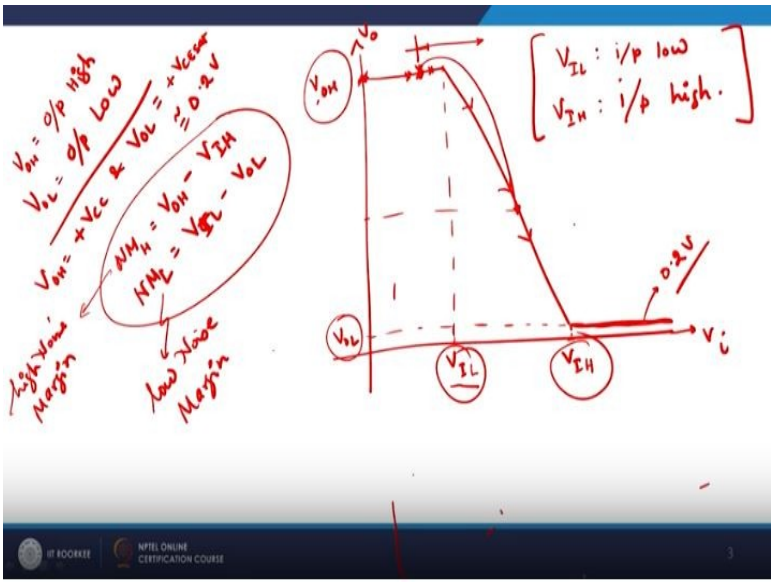

Let us suppose I have got a curve like this and I give like this and I give it like this and then you go like this, right? So we draw this curve, remember V_{BE} (on) and then we get this and then we get this and we of course get this into consideration. We define this to be as V_{OH}. So this point is, V_{OH} is V_{OH} implies output high, right? And this is V_{OL}. So V_{OL} is output low. So V_{OH} is output high and V_{OL} is output low. In our case, V_O in our case, V_{OH} is equal to $+V_{CC}$ and V_{OL} is equal to plus V_{CEsat}, approximately therefore equals to 0.2 Volts. Fine? Is it okay?

We also define two terms in the input side because this is V_I and this is V_O on the input side. And this is when V_{IH} and V_{IL}. This is V_{IL}, this is V_{IL}. This is V_{IL}, right? V_{IL} and this is V_{IH}. So V_{IL} and V_{IH}, why? Because V_{IL} means V_{IL} is meaning that input is low. And V_{IH} is meaning that input is high. So I get four conditions or four biases. V_{OH}, V_{OL}, V_I so I get V_{OH} right?

V_{OH}, V_{OL}, V_{IL} and V_{IH}. V_{IL} and V_{IH} are input high input low. Input low primarily means that that is the maximum value, right? Of your input in the low condition when the output will be actually registered as one. And V_{IH} is the, maximum, the minimum value in the highest condition when the output will be read as 0, right? So you have to be very careful about what is the meaning of V_{IL} and V_{IH}.

So V_{IL} is input low. Input low means this is the maximum value of input at which you will actually get a high. If you exceed, if you exceed this value of V_{IL}, your output will start to drop down. And that is what is happening here. See? Right? Similarly, V_{IH} is the minimum value at which your output will be low. After this, if you look very carefully it might fall down or it might remain constant, right? So this is what you have learnt. So typically it is 0.2 for a silicon diode V_{CEsat} is equal 0.2. We define a new term here and that is how you define your... we define this to be as a noise margin and that is basically my noise margin static noise margin we define, high noise margin.

It is defined as V_{OH} - V_{IH}. And N_{ML} is $V_{O,}$ V_{IL} - V_{OL}. Right? V_{IL} - V_{OL}. So the difference between the voltage of V_{OH}, V_{OH} here and V_{IH} here is defined as my high noise margin. So this is defined as high noise margin (noise margin) and this is referred to as a low noise margin. What does a high and low noise margin mean?

This means that, we will discuss also when we will go to CMOS but make it clear as well, so we can come over it. High noise margin means that, let us suppose we have 1 being entered into the BJT. So my input is 1 right? Now, let us suppose that there is noise in the system. If the noise becomes very large, a 1 can be actually seen as a 0 by the input side, right? Or it can change from 1 to 0. So which means that let us suppose you had biased your device somewhere here, right?

And your input cycle was slightly like this, no problem. So what is happening? The maximum value of the Q-point goes here to here, no problem. Your output is still high. But if you make a very large input, because of noise of some other means, this Q-point will shift from here to somewhere here. And therefore the output starts to fall down. And therefore you are not able to store an information of 1 in the output size because the input is actually going from high to low. Right? Sorry low to high.

So you had an input which was low, right? You inserted, you add noise to it, right? And the (minimum) maximum noise which can be added to the signal without changing the output is defined as my noise margin. So we define the high noise margin for 1 and we define the low noise margin for 0. Fine? So higher this value, better your design is because better it will be rejecting the noise.

So if your noise margin is typically, say, 1.5 Volts it means that till 1.5 Volts you give me any data, it will always be read as output 1. Right? And if the N_{ML} is also very high, it means that you give me a value of input data equal to the N_{ML} value and it will be read as output 0. So we have two noise margins therefore as I discussed with you. We have got a high noise margin and we have got a low noise margin, right? And we try to keep both the noise margins as high as possible.

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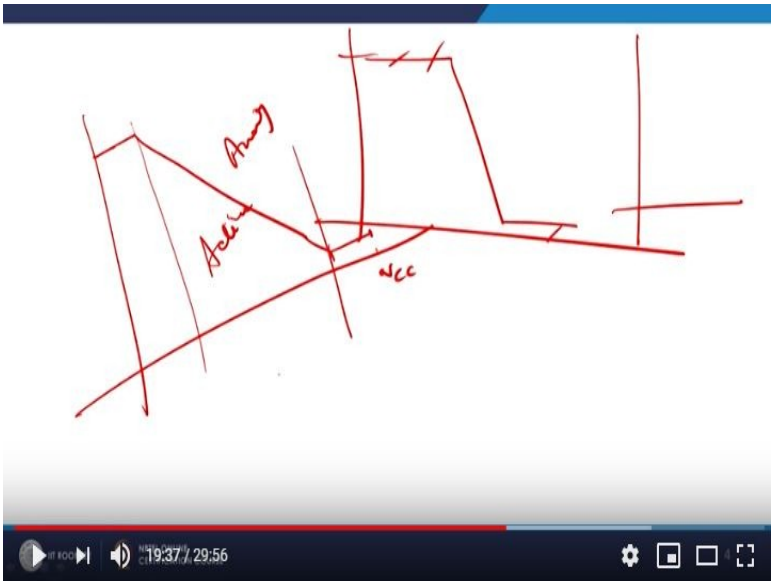

So if you want to use it for the purpose of digital logic then you keep your noise margins relatively high, right? You may keep this relatively high. If you want to use it as an amplifier, then keep this low but increase the value of your... So this is your V_{CC}. Increase the value of this transition active region. Then again use it in an analog domain. But if you want to use it in a digital domain, keep this one as low as possible and try to achieve equal values of input and output noise margins.

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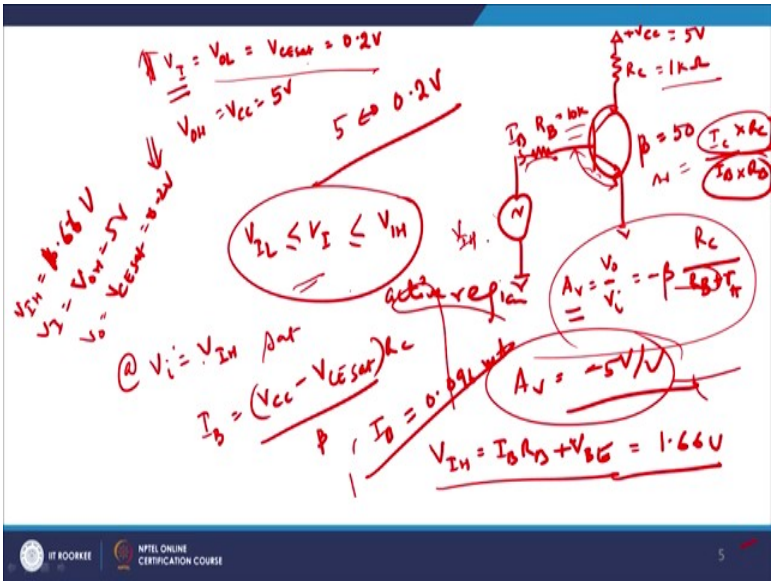

I will take up an example and show it to you how I can follow a noise margin. Say I have got a, I will give you a basic fundamental principle. I have an R_C here, right? I have got resistance here. And I have got R_B here. I am applying an input signal. It has already been biased by a DC bias. This is R_B, R_C and this is (v) $+V_{CC}$. And this is the transistor β whose β is exactly equal to, let us suppose, the β value for this is exactly equal to 50 let us suppose. V_{CC} is equal to 5 Volts. R_C is approximately equal to 1 kilo ohm and R_B is equal to, let us suppose, 10 kilo ohms.

So let us see how does my noise margin and all these things come out. So if you see, V_I is equal to V_{OL} equals to V_{CEsat} equals to 0.2 Volts. So when you apply V_I input, right? And I assume my output to be low. So my input is high (input is high), my output is low, equals to V_{CEsat} equals to 0.2 right? Similarly, when I apply V_{OH}, input is high right? So in this case input is high, in this case input is low. And then I get V_{OH} equals to V_{CC} equals to 5 Volts. Right?

So when you input is low your output is V_{OH} and that is almost equal to V_{CC}. And when your input is high output is low, almost equal to V_{CEsat}. So the swing is from 5 to 0.2 Volts. This is the swing in the voltage domain which you see when you have such type of a system available with you. Now assume, let us (let us) do one thing that I assume that my V_{in} or input is between V_{IL} input low as well as between V_{IH}, right? So I am in the active region of operation.

So in the active region, I can safely write down A_V to be equal to V_0 by V_I, output voltage by input voltage which is minus beta times R_C by $R_B + R_\pi$. We will discuss this time and again. But if you can understand R_C by R_B is the ratio of the collector current to the base current right? So it is the ratio of the collector current and the base current. β is equal to I_C by I_B. So if you multiply it I get a voltage gain A_V and because β is basically output current by input current, right?

If you multiply this with R_C and this if you multiply with R_B, I get output voltage upon input voltage which is exactly equal to A_V value. Fine? Is it okay? So with this concept, if you put the value of R_C as 1 kilo ohm, R_B as 10 kilo ohm and you also put β to be equal to 50, I get A_V to be approximately equal to -5 Volts per Volts. Right? Which means that it is basically negative because obviously you are entering into a (negative) 180 degree phase shift, output is always 180 degree phase shift with respect to input and therefore you get A_V equals to - 5 Volts by 5 Volts right?

Now within the active region therefore, within the active region, I get A_V equals to this much. Now at when your V_I is equal to V_{IH}, because that is what you will get, I will enter into saturation region and I can safely write down I_B to be equals to V_{CC} - V_{CEsat}, right, divided by β divided by R_C. Because if there would not have been β then it should have been I_C.

But you put a β here and then directly convert into I_B. So if you solve it, I get I_B to be approximately equal to 0.096 milliamps. So it is the order of microampere right? Now, if I can write down V_{IH} equal to I_BR_B. I_BR_B means I_B times $R_B + V_{BE}$. Means this voltage which is V_{IH}, let us suppose DC bias is exactly equal to the voltage here and the voltage this one. So if you add these two together, I should get the third voltage.

And therefore I get V_{IH} equals to $I_BR_B + V_{BE}$, right? Put the value of I_BR_B and V_{BE}, I get 1.66 Volts. So input high is 1.66 which we follow right? Now, if this is true, I can write down V_{IH} therefore to be equal to 6.66 ahh,,, 1.66 Volts, right? So therefore V_I equals to V_{OH} equals to 5 Volts, right?

And V_O will be equal to V_{CEsat} and that is equal to 0.2 Volts. Fine? So I get these many definitions available to me, right?

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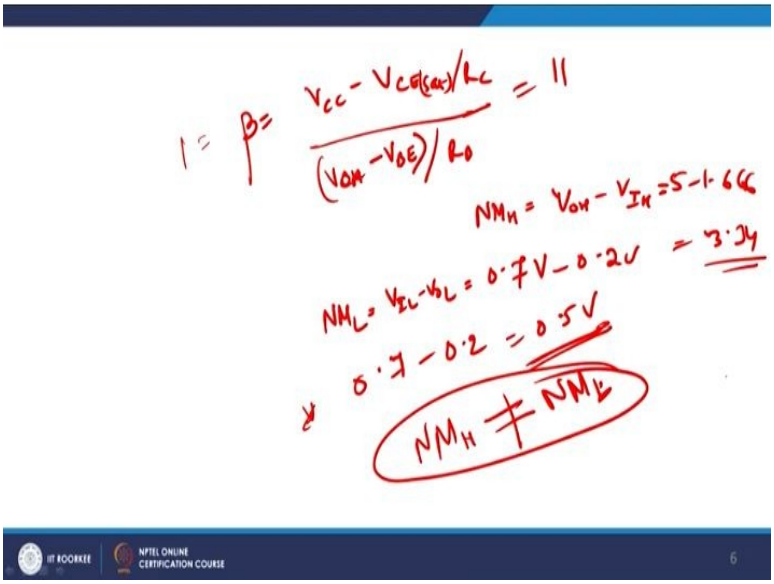

Now, if I assume these definitions are equal then from here, I can get the value of β. β is the current gain to be exactly equal to V_{CC} - V_{CEsat} right, divided by V_{CC} - V_{BE} or V_{OH} - V_{BE}. This divided by R_C, this divided by R_B. If they are exactly equal, β will be equal to 1, right? And that is what you get. But in clear (clearly) this is equal to 11, which you get. Therefore N_{MH} will be equal to V_{OH} - V_{IH} and this comes out to be 5 minus 1.666 and that is equal to 3.34.

In the second case when I find N_{ML}, it is V_{IL} - V_{OL}. So what is the value of V_{IL}? 0.7 Volts - 0.2 Volts and that is equal to 0.5 Volts, right? So we end up having a very interesting discussion on bipolar transistor, that if you don't do any manipulation in terms of doping or circuit changes, you would expect to see β to be approximately of the order of 10 to 15. Once you have that β value, you can achieve a current gain of approximately 10 to 15 within the chip right? Or within the design which you have (which you have) made.

So let me find out N_{MH} and N_{ML}. And that comes out to be 3.34 and if you find out N_{ML}, it is V_{IL} minus V_{OL}. So V_{IL} is 0.7 - 0.2 and this is 0.5 Volts. But you see, your N_{MH} is not equal to L. Which means that there is a problem. That means high to low noise margin is not equal to low noise margin. Which means that 1 can be transmitted very easily even with a noise figure of very high noise figure. Whereas 0 will be stopped or inverted if my output noise is typically small.

So in reality, we should have N_{MH} equal to N_{ML}. But in practical, it says as you can see in this bipolar transistor, N_{ML} is not equal to N_{MH} right? And that is a problem area which people face as far as designing is concerned. So somehow or other you have to make N_{ML} equal to N_{MH} right? And that is what is very important, right? Okay, so with knowledge or this basic criteria, we have therefore understood the basic concept of a simple BJT inverter, how does it works and what are the various features of a BJT inverter.

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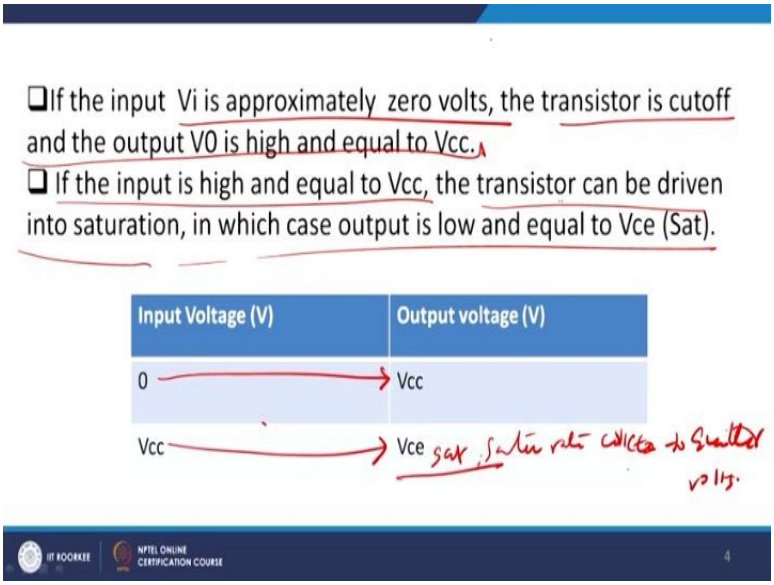

Therefore, as I discussed with you, if the inverter V_I is approximately 0 Volts input, the transistor is cut off and the output voltage V_0 is high and equals to V_{CC}. So when you input is low, output is high. Now if the input is high and equal to V_{CC}, the transistor can be driven to saturation in which case the output is low and equals to V_{CEsat}. So the output is either equal to V_{CC} or equal to V_{CEsat}.

Two extremes which are available for this particular design right? And you can actually switch from one to the other very fast in this case. Right. Now if you therefore see, that takes care of our understanding of your transistor action and you can therefore see that when input is equal to 0, the output is equal to $+V_{CC}$.

When the input voltage is $+V_{CC}$, the output voltage is V_{CEsat} also known as saturated collector to emitter voltage, right? So we will do the subsequent talks the next time. We will look into the second order effects in a detailed manner in the next turn and we will go into the details of each one of them as we move along.

So what have you learnt? BJT as an inverter, what is a noise margin, how we calculate the noise margin from the device characteristics and how noise margin is related to the overall sensitivity and robustness of the inverter design, right? With these words, thank you very much for your patient hearing. Thank you.