CMOS Digital VLSI Design
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Module No # 02
Lecture No # 09
POWER ANALAYSIS – II

Welcome back to CMOS digital VLSI design NPTEL course we were discussing in the previous lectures about dynamic power dissipation and we say that it was equals to alpha times CL VDD square into F where F is the frequency of operation.

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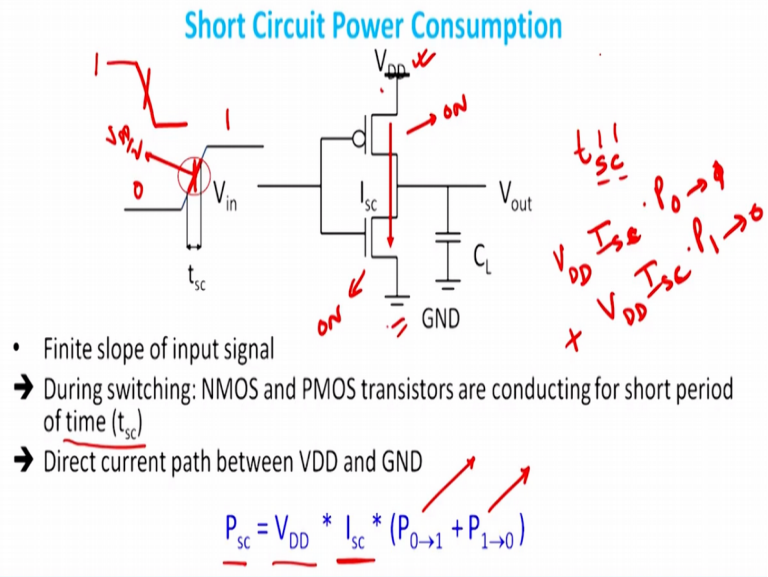

We go to the next one which is basically short circuit power dissipation what happens if you remember that whenever we were discussing the voltage transfer characteristics of the device and we got something like this as the voltage transfer characteristics.

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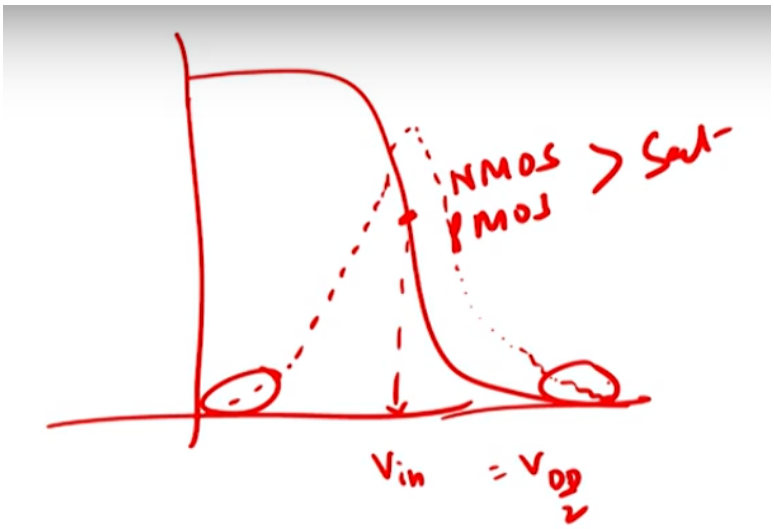

Which is something like this which is like this and becomes like this then what happens in that sometime in the middle where V in was equals to almost equals to VDD / 2 approximately right. You added this place both NMOS and PMOS in saturation region and they were both equally on right so if you get back into that and see here so when the input is going from 0 to when input is going from say 0 to 1 I will have R from 1 to 0 then somewhere in the middle here or here is the point where V in is going from 0 to VDD.

So almost half the VDD will be available here so this will be approximately equals to VDD / 2 at this case this will be on and this will be also on and therefore there will be a short circuit path between VDD and ground and this is the ground and therefore there will be heavy current flowing from this VDD rail to the ground real right and therefore you see for a short period of time defined as tSC, SC stands for example short circuit right.

And therefore we defined this to be as PSC the power dissipation it was to VDD multiplied by ISC. ISC is the short circuit current which is flowing this has to be multiplied with probability of 0 to 1 and to 1 to 0 why? Because every time I go from 0 to 1 or 1 to 0 in input side I will always cross the point of VDD /2. And therefore the probabilities of additive in nature here and therefore the total power will be given as VDD into ISC into P0 to 1 this will be added with VDD ISC +P0 to 1 and this will be 1 to 0.

So this is the total steady power dissipation available to you and therefore if you super impose over this the idea of power current. The current will be maximum here the short circuit power and then we will go will go down why will go down? Here it is like this 0 because one of the device is cut off so there is no direct power between ground and the VDD and here those are direct path and therefore you will see a large amount of short circuit power dissipation here.

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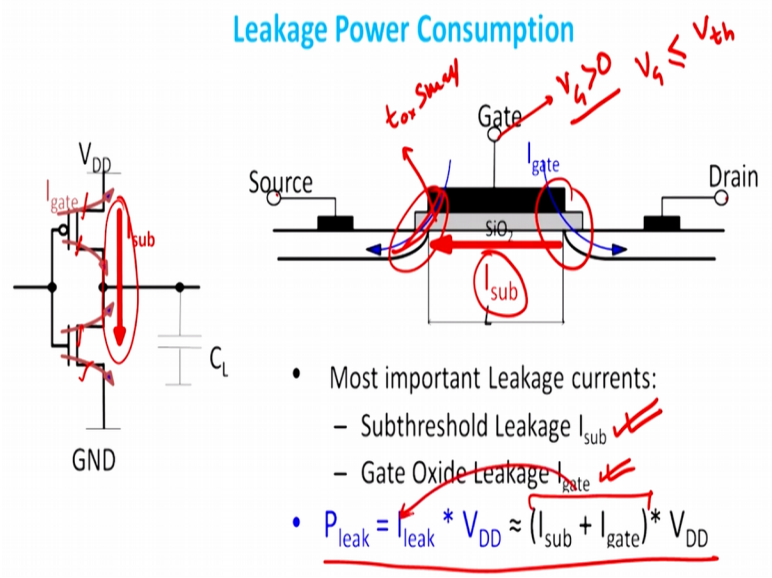

Let me go to the leakage power consumption is the third power consumption available to us and this leakage is primarily because you will have first of all one is the sub-threshold leakage right this happens when the gate voltage is just below threshold which means that VG is just below threshold voltage of the device. You assume that in ideal case there should be off but in reality I am not off.

There are some carrier not available and therefore they will flow from source to drain and therefore that will result in what is known as a sub-threshold current right. So this is known as sub-threshold leakage or Isub there can be also a gate leakage current which is by virtue of the fact that on the gate side remember you are applying the voltage which was greater than 0 So there was heavy electric field along this direction and this source is grounded or even drain is grounded or giving you particular voltage there will be this acts like a this is typically very small tox is small enough.

Then this will direct leakage will be there of electrons from this end to this end and therefore there will be defined as the gate oxide leakage current. So I will have two leakage current available to me one is the sub-threshold current which is this one and you will have 4, 1, 2, 3, 4 why because each transistor will have 1 this side and 1 this side leakage current. So will have 4 leakage current upon inverter right and that is a major concern or major concern available to us.

If you try to find out the value of IPP it is nothing but IP which is Ipeak means is the current flowing through the leakage current which is sum of basically the sub-threshold and the gate leakage current so this one is basically sum of these two multiplied by VDD and this is how it works out. So let me give you a brief idea about the whole equations that the power equation in CMOS is something like this.

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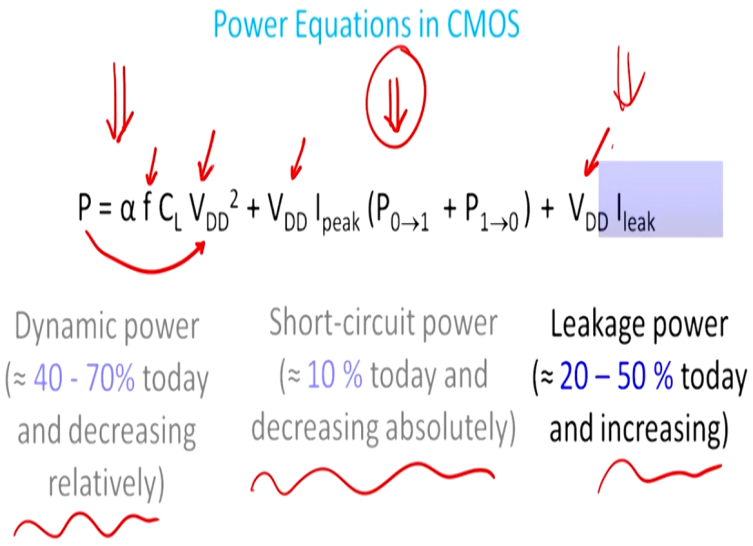

So first power is basically the dynamic power which you see in front of you alpha times f times CL times VDD square right and the dynamic power today is approximately 40 to 70% of the total chip power right and this is a very well-known fact available to us. The second which you see in front of you is basically the short circuit power and we discussed and this approximately 10% today and it is decreasing why because you are what you can do is basically if you can make your rise and fall times right of the input wave very small.

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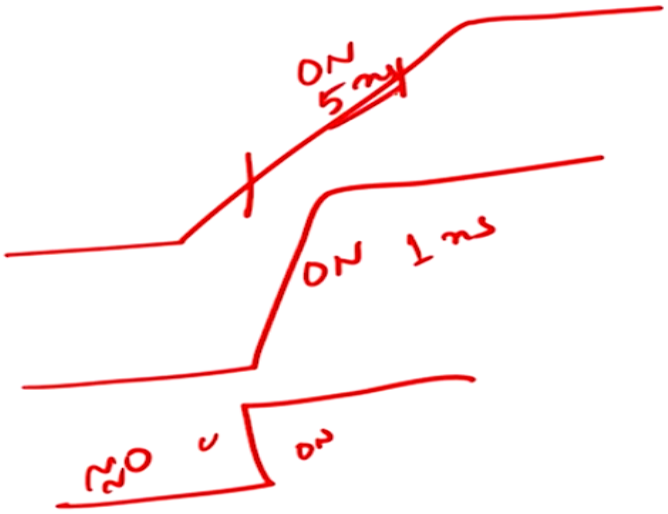

So rather than let me give you an idea so rather than your rising like this if you can rise input rise something like this or ideally something like this then the time till which NMOS and PMOS are ON will be larger in this case as compared to this case this will be almost equals to 0 and this will be let us 1 nano second this will be say 5 nano second. So the time is larger more current will be flowing therefore more power will be there.

So if you reduce the rise and fall time of the input wave form you can actually achieve a lower value of the short circuit power dissipation you also the power leakage power dissipation which you can see here this is the power leakage power dissipation and it is increasing. So who is decreasing the middle one is decreasing which is the leakage power is decreasing but my it is decreasing relatively but my frequency my leakage power because of leakage is going on increasing.

But please understand if you increase the frequency operation which is this one your dynamic power will increase what comes to our help is that please under this power is a quadratic dependent on VDD. So if you are able to load your VDD slightly you will have a quadratic decrease in dynamic power and that is the major issue which come into picture you see if you see again very closely that obviously power will have a VDD term.

So all are having a VDD term which is common to all of them so if you can scale down your VDD even without any knowledge of chip design you can actually lower your power dissipation

to a drastic level. So that is general idea or general scheme of this which we are actually looking into.

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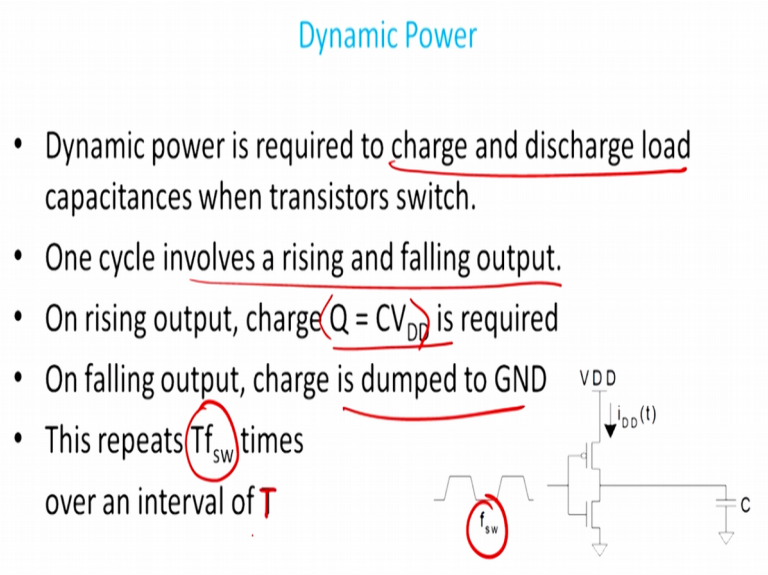

So let me come to the dynamic power here the dynamic power is as I discussed with you is required to charge or discharge the load right and therefore one cycle will involve one rising and one falling output as I discussed with you on rising output when the output is rising it will charge the capacitor to the value Q = CVDD and on falling output the same charge is dumped on to the ground.

So you will have dumping in the ground and this repeats how many times T into fSW which is basically the fSW is the frequency of the input wave form multiplied by capital T. Capital T is the interval which is happening to you so this repeats itself and you will have dynamic power available to in that case.

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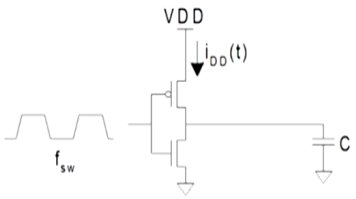
Dynamic Power Cont.

$$P_{dynamic} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}\,dt$$

$$= \frac{V_{DD}}{T}\int_0^T i_{DD}(t)\,dt$$

$$= \frac{V_{DD}}{T}\left[Tf_{sw}CV_{DD}\right]$$

$$= CV_{DD}^{2}f_{sw}$$



Now if you look at the dynamic power I get I am not deriving the whole dynamic power equation but let me give idea about what the dynamic power is all about how I get the dynamic power. So I get 1 / t into IDD into VDD as I discussed with you from where to where should I integrate from 0 to T right because 0 to T is the time that which your input wave from is going from low to high or high to low.

If you take VDD because VDD is obviously constant you can bring it outside the integral and I get VDD / T, 0 to T iDtD and therefore VDD by T iDDt can written as TfSW into C into VDD because this is Q this is basically a Q. Q multiply by T times FSW if you remember the previous discussion which were having if you look very carefully Q = C times VDD is the amount of charge which you seen into of you and T into fSW is basically the amount of repetition happens when this charge as to be dumped on to the ground.

With this knowledge what we get is that if you multiply therefore t into fSW multiply by charge Q I get the total current and therefore from there if you solve this equations then I get C into VDD. So this is VDD here I get VDD square into fSW the frequency operation I also get C coming into picture because effective 1/ T comes this C will be there which is available to me. So this takes care of the so this T cancel with this T and left with this expression available to us. So this exactly the same thing which we were discussing in the previous slide.

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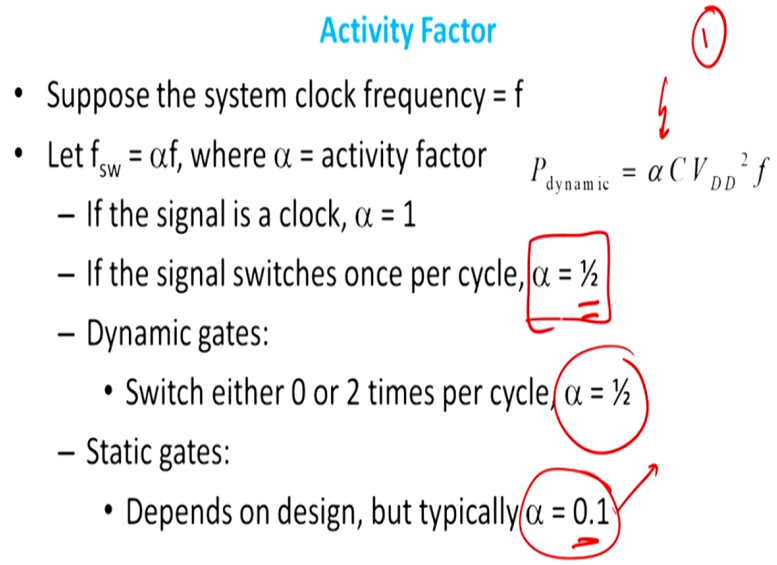

Now as I told to you dynamic will also have a factor of alpha which is basically the activity factor. Now if alpha equals to half right and if alpha = 0.1 then or alpha = 1 then respective alpha = 1 if I reduce the alpha = 0.1 I will have approximately 90% reduction in my dynamic power without even altering the frequency but what the cost I am paying for it is basically that performance actually stops to go down I will tell you the reason why when alpha is 1 alpha is 0.1 primarily means out of 10 clocks cycles when you are using the CMOS is actually giving 0 to 1 transition 10 times when alpha = 1.

So a heavy switching was there and large amount of data was pumped into the whole system but if it is 0.1 it primarily means 1 out of 10 data 1 out of 10 clock cycles was a power consuming cycle right which means that you are only allowing to do one switching per 10 cycle which basically implies that your ending up having a less amount of data available to you which results in a lower power dissipation.

But the cost to pay for it is possible in the performance right so static get typically as got a value of alpha = 0.1 we will discuss dynamic gates of half and as I discussed with you depending on the number of clock cycle alpha can be defined an activity fracture can be defined very easily in this case.

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Static Power

- Static power is consumed even when chip is quiescent.
  - Ratioed circuits burn power in fight between ON transistors
  - Leakage draws power from nominally OFF devices

$$I_{ds} = I_{ds0} e^{\frac{V_{gs} - V_t}{nV_T}} \left[1 - e^{\frac{-V_{ds}}{V_T}}\right]$$

$$V_t = V_{t0} - \eta V_{ds} + \gamma \left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$$

As I discussed with you what is static power? Static power is a power which is consumed even when the chip is in a sleep state or in the sleep mode and you do not have any direct path available to you between short circuit and ground but because of leakages there will be some amount of power being dissipated right if you have ratio of circuits what is the meaning of ratio of circuits?

Those circuits in which the W / L ratio of pull up which is PMOS and pull down which is NMOS determine the functionality of the chip in such a scenario I and the W / L is available to you more current will be flowing through to it and therefore it consume a larger power it will draw a larger power from VDD rail. For example if you make PMOS W/L larger then you will be drawing larger amount of power from the VDD rail right.

Whereas if you W/L for a NMOS is larger you will be able to dissipate the power from the capacitor on to the ground in a much faster phase fine. So this things should be cleared to you all of you now leakage power is given by the standard formula which you see in front of you here VT is the thermal voltage N is the factor which goes from 1 the ideal value of N = 1 VGS is the applied gate voltage Vt is the threshold voltage of the device and this is by virtue of the body effect in consideration.

But static power can be reduce drastically by doing body effect that is what I wanted to tell you here if you want to reduce Ids which is this one you need to make your VT larger and larger

right. If you make it VT larger and larger right if you make it VT larger VGS – VT reduces and therefore e to the power Vgs – e T by e ta VT will actually reduce drastically right. So I have a two VT's here one VT is threshold voltage and this VT is basically your thermal equivalent voltage KT / Q.

If you make it VT large therefore as you can see you can actually reduce the leakage power so this is standard technic people do that is using doing body effect then try to reduce the threshold voltage of the device which we have already studied and that will make your steady power dissipation lower right. So let me just therefore give you what important issues are there as far as reducing the dynamic power.

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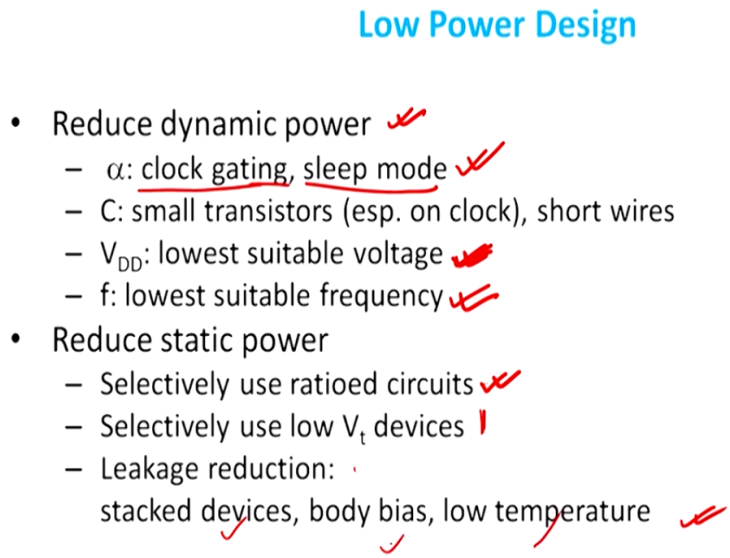

So as I discussed with you do nothing else best methodology available to is just reduce is suitable VDD right. Please keep in mind when you reduce VDD you also reduce the current right and therefore your power dissipation goes down but when you reduce your current then the amount of time taken to charge your output load capacitance also becomes larger right and therefore your delays starts to become higher which means that now I am trying to reduce my dynamic power dissipation at the cost of what at the cost of a larger delay at my output and this is the price is pay for it.

So similarly if I therefore go to the other set of story if I make it my VDD large then may be what I am trying to do is I am increasing the current and therefore I am decreasing the delay

because I am able to charge the capacitor very fast at the same instant of time ID into VDD which is the power will actually rise up so therefore power in delay just grow opposite in nature right. So reduce your VDD you can also reduce you can work with the lowest operating frequency.

So not every time you have to work with highest frequency right we can work with low for example certain affairs or certain digital logic designs not always you have to work at a very fast phase right you can actually lower down your phase slightly right when you low down your frequency power dissipation reduces. Similarly we do a clock gating a sleep mode that you do not let the alpha to go higher which means that you do not allow the CMOS to go to have larger 0 to 1 transition during the clause cycle.

So the techniques used are clock gating and sleep mode well you need to follow certain standard books to understand this out of the course at current stage but this is methodology used to have a look at many research papers many books are available where you will have clock gating properly introduce to sleep mode transistors are there right. Another methodology we will use is basically known as stacking and they use this stacking devices which you can see here for reducing the leakage current right.

So for dynamic power reduction please concentrate on VDD that is the first one the second is CL load capacitance the third is alpha which is basically the clock using clock gating sleep mode transistor and then forth is the frequency of operation which is using. If you want to reduce static power there are three options available again with us use ratio of circuits. So that you W / L ratio which we change at if you get enhance the W / L ratio you will be able to achieve a larger current right and you will be able to achieve it but static power comes by virtue of what by virtue of what sub-threshold current and your gate leakage current.

So if you have larger device sub-threshold current will reduce drastically and you can actually have a load reduced power static power. Use low Vt devices if you use it the your static power will automatically reduce if the leakage current reduces and you can use leakage reduction technique stag devices body bias and low temperature. Body bias will make the threshold voltage high or low and therefore it reduce power drastically.

So these are the few techniques by which you can actually reduce your the reduce your power let us look at dynamic power right. First as I told to you reduce VDD it has got a quadratic phenomena so there will be reduction of VDD square there will be proportional to VDD square so they will be reducing that but that is the big but here see in front of you is that as VDD approaches approximately twice Vt right which is twice Vt here.

Your current becomes so low that you are not able to sustain a good performance in the limit from the chip. So while reduce VDD is good option but reducing it drastically to a very low value will be again detrimental to your performance as I discussed with your earlier. Lowering CL primarily means that you reduce your transistor load capacitances this will improve the performance for sure because it will make it higher but then you see I will give you an example.

If you reduce the CL load capacitance but if the loading if there is self-loading phenomena what is self-loading phenomena will explain to you what is self-loading that you wanted to make the PMOS let us say longer as compared to NMOS you increase the W/L of PMOS as a result overlap capacitance says Cox everything suppose increases and it starts loading the output load capacitance.

So this is known as self-loading the circuit itself you want to improve it by improving the W / L ratios but the cost to pay for it is that charge to load the capacitance outside this is known as self-loading phenomena right and you do not want that self-lading phenomena to occur and therefore keep the transistor minimum sized. So keep it W / L ratio's L should be minimum as per the technology domain and keep W / L ratio as per the this thing.

So as I discussed with you the keep your switching activities at the lowest and therefore switching activity is a function of single statistics I did also depends upon logic of every design and already discussed with you switching activity is a function of the type of gate which you are using so the type of logic gate which you are using will determine your swathing frequencies. Switching frequency is 0 to 1 right and it that is how it define the switching activity.

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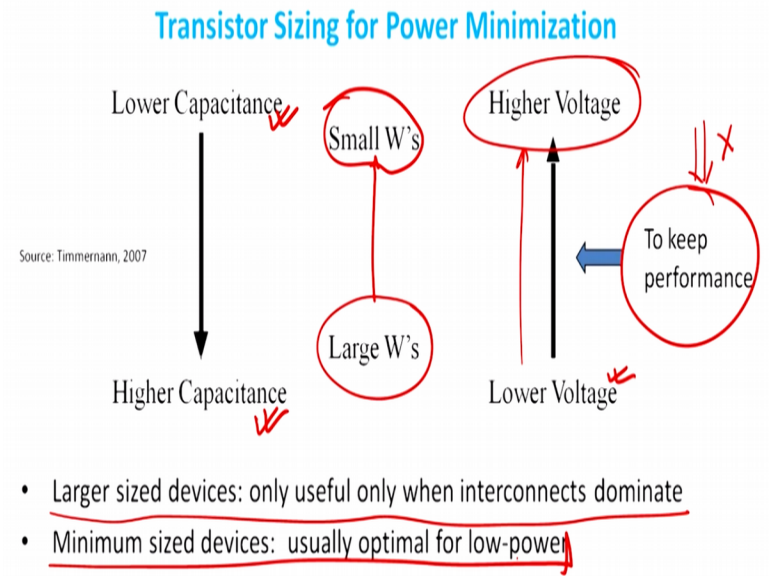

Just to give you an idea about here I will give you a brief idea about trying to say here that if you want to have a larger W here W / L width is larger your width's are larger you will automatically have a higher capacitance right because width's are larger W will be larger W into L which is basically the area under the gate will be larger you automatically have a higher capacitance.

But if your W is larger I can afford to keep my low voltage low because if W is larger you got a better current carrying capability I can afford to keep the voltage low but the problem is that in order to keep the performance of the chip in the proper state I cannot afford to go for lower voltage. So what I do? I increase the voltage to higher voltage now so when I go for large W to small W because i want for certain reason I want the area of the silicon to be low.

I lower my capacitance the less but then I have to ensure that I also have to raise the value of voltage slight voltage. So that I do not keep this performance degraded to larger extent right so this is very important once should be very careful about it that though your raising the value W all or lower in the value of W please ensure that your applied gate voltages or applied drain voltages is in this case VDD do not go below a particular device.

The larger size devices are only useful when integrate dominates which means that the interconnects to CMOS inverter if that capacitance is higher which means that there is no self-loading phenomena then only if I increase W / L of PMOS it does not influence your CL because no self-loading and you are happy with it right. But if you wiring capacitance is interconnect

capacitance is much smallest compared to the CL then there will be a loading phenomena and therefore if you change a W / L ratio of the of the PMOS or NMOS your CL will start to change as I discussed with you in the previous term.

And that makes my life difficult right is what we generally do is that we try to a minimum size device and this usually meant for achieving the lowest power of available to you right. So this is what we have discussed till now.

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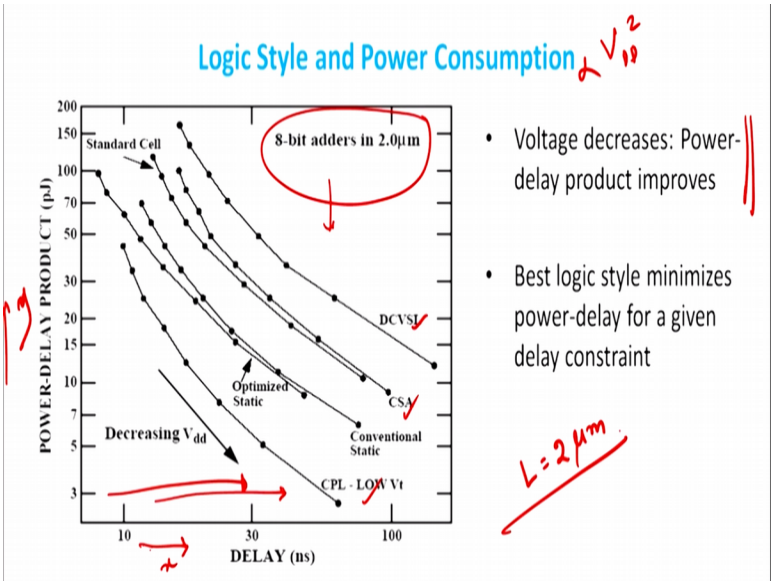

The other part I will not go into detail of this one here but I will just give you a brief idea about what this logics are you might be knowing what is DCVSL or CSA or may be CPL but what I primarily tell you from this graph is which is basically it is graph is basically a b bit adders. Adders are nothing but simple combinational clocks will study later on which add two bits 1 or 0 or 0 or 1 we will just add two bits and these two bits when they get added up they give your output right.

So what is graph I will tell you is how the delay between the primary input and primary out is platted on the X axis right and the PDP which is the power delay product is plotted on the Y axis as you can see as the delay goes on higher and higher that means you move one the X axis from left to right your PDP actually drops down I could expect to see the PDP to raise because power into delay but as you make your delay larger and larger why your delay is increasing larger and larger because you are reducing your VDD.

As you reduce your VDD please understand power is quadratic function of VDD so the power drops down quadratically right but the delay drops down linearly or increases linearly. So the overall what happens is that the PDP starts to improve right and that is very interesting phenomena which we see. That though we increase the delay and we move from low values of delay to high values of delay here my PDP reduces the reason is that I can go for higher delay because i will be I can afford to have to lower VDD.

Higher VDD primarily we will have a lower current high delay but when your current are lower you end up having lower power therefore PDP actually lowers down because reduction in power is higher as compared to increase in delay am I clear and as a result there will be almost linear or may be a quadratic flow drop in the value of the PDP in this case. This results in this drop of current value of voltages which you see.

This is an example is for an 8 bit adders which is being fabricated to my current technology 2 micron technology basically means the channel name is basically 2 microns 2 micro meter right and this give you an idea about a what the logic style is which tis words I will finish off today's lecture and next turn I will start with may be combination of logic of block and show you how it works out.

So let me recapitulate what we did today or this turn we looked into the power what are the various contribution of power in the circuit specially a CMOS in invertor circuit how does it influence the functionality of a chip. What will be also looking later on in this can I how can I reduce the power and optimize the delay and we have seen on what parameter this is the power depend and where as a designer should you plug your power plug your parameters so that the power reduces with these word I thank you and for listening to this lecture and we will meet next time thank you very much.