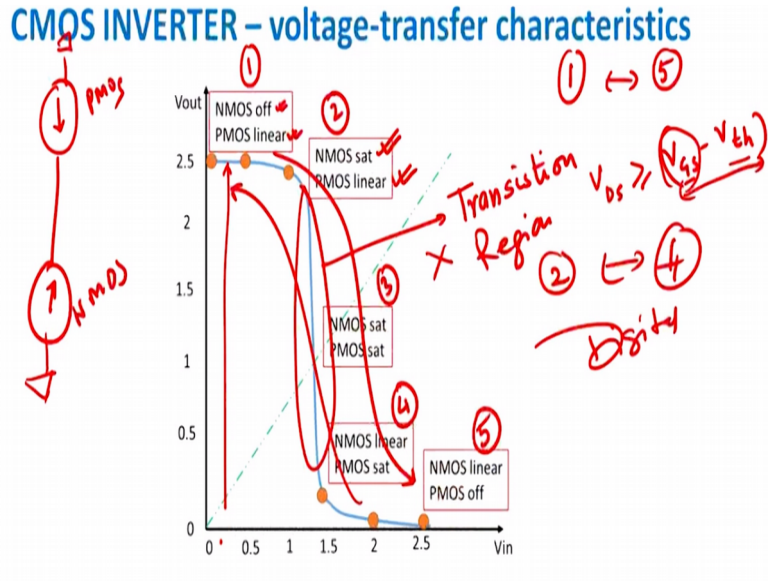
CMOS Digital VLSI Design
Prof. Sudeb Dasgupta
Department of Electronics and Communication Engineering
Indian Institute of Technology – Roorkee

Module No # 02
Lecture No # 06
CMOS INVERTER BASICS – II

Welcome back to this section or of COS invertor we have discussed how in our previous lecture in previous slide how you are able to plot the VTC. So this is known as the voltage transfer characteristics of the device now if you look here and this slide if you look at the slide here we have distinctly 5 regions of operations right.

(Refer Slide Time: 00:49)



So let me name it 1, 2, 3, 4 and 5 so there are 5 distinct region of operation if you remember when my input was low which is somewhere here which is region 1 right in region 1 which is this one since my input was low which means my gate voltage was low NMOS was obviously switched off. So that is the reason NMOS is off but my PMOS was working in the linear region it was behaving like a resistance right.

So I have got a linear region in P here right 1 and 5 are divertically opposite because in 5 input voltages are high which means that the gate to source voltages are high which primarily means that NMOS was in the linear region behaving like a resistor and PMOS was cutoff. So therefore

1 and 5 are just antiparallel to each other sort of, if you look at region 2. Region 2 is the place where your NMOS, V in has become a slightly higher which has resulted in NMOS entering into saturation.

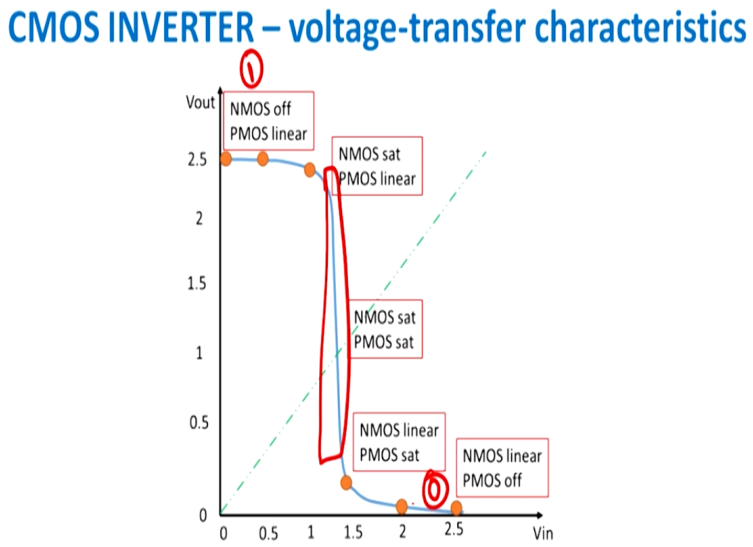
Because please remember for saturation VDS will be greater than equals to VGS – Vt where VG is gate to source voltage Vth is threshold voltage. Now if you gate because V in was the gate to source voltage since we increase this V in this quantity has become larger and therefore drain to source what is drain to source for NMOS? When your input was low where your input was low it was cut off and therefore drain to source voltage was effectively very low.

But now I am getting an increased value of VDS the reason being my V in actually increasing I am trying to make my NMOS ON and therefore my voltage at the output is now getting latch to the ground. So this allows that to be in NMOS in the saturation region and PMOS to be in linear region right. Just the opposite will happen in 3 in 4 in 4 the NMOS will be in linear region and PMOS will be in saturation region and therefore just there opposite to each other as we just now discussed with you right.

Because NMOS and PMOS are at the symmetrical device in nature what happens in region 3 that is quiet interesting. In this case both NMOS and PMOS starts to behave as a saturated device right so which means that I will have a PMOS in saturated I told you in the previous term it starts to behave like a current source I will have another here NMOS and this will be PMOS and this will be NMOS here right and this will be VDD and this will be ground.

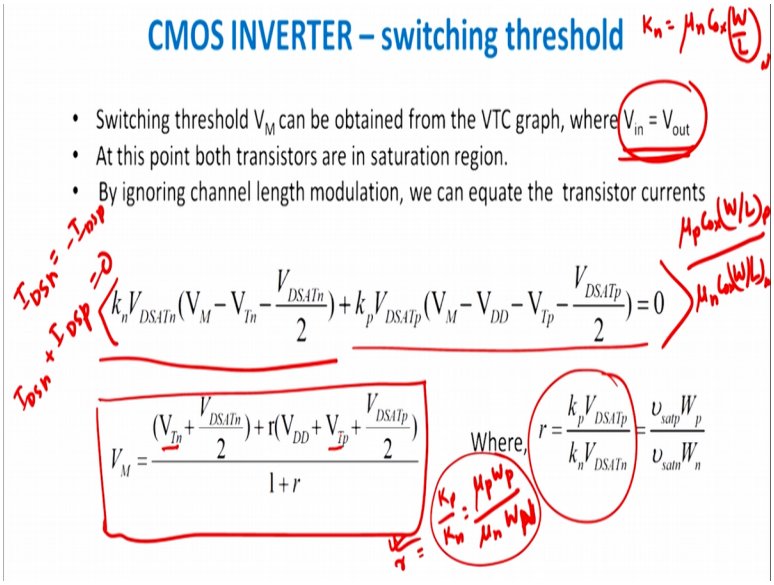
And now you very well know that two current sources in series is totally an unstable condition and therefore this region which you seen in front of you is basically what is known as the transition region right and you do not want this transition region to occur in any digital design. For digital design this is the strict no where you can operate so what you need to do. You need to very fast go from this point to this point or from this point to this point so it is basically 0 to 1 transition or 1 to 0 in the output 1 to 0 and input 0 to 1 transition right. So you have to be very cautious about what you are trying to do as far this circuit is concerned.

(Refer Slide Time: 04:02)



But two important points before you move forward is that this region is unstable this region is fully unstable because two transistors are in series to each other behaving as a current source this will behave as a output 1 and this will behave as a output 0 fine. So this is the voltage transfer characteristics of invertor. Let it be therefore defined to you what is switching threshold?

(Refer Slide Time: 04:25)



Switching threshold is defined as that point where V in = V out if you go back to the previous slide and if you plot a line which is at 45 degrees angle right and if you plot a line then where it cuts the point is the point where you will actually get V = V out right. So this will be the point where V in = V out provided this is basically a symmetric profile which means that this is perfectly symmetric as respect to this.

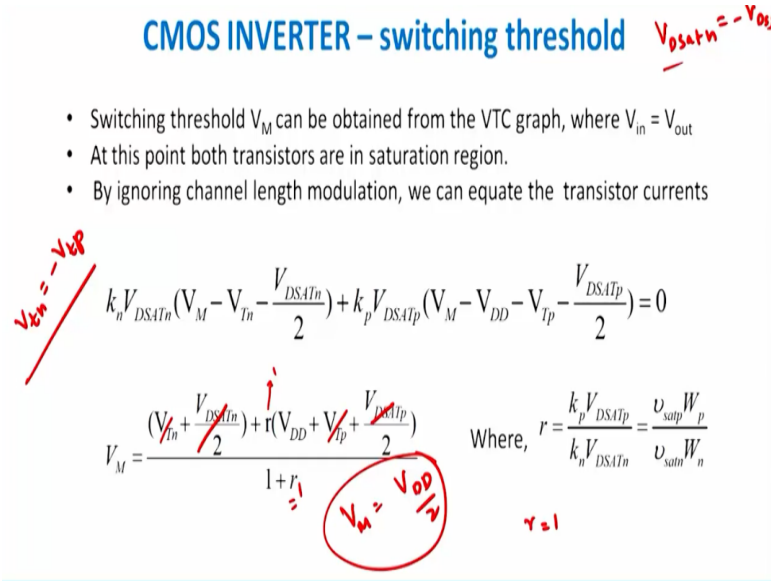
Assuming they are same then a straight line and angle of 45 degree gives you an idea about where V goes to V out. So that is differential switching voltage as I discussed with you at that switching voltage bot the transistors NMOS and PMOS and already in saturation which means that both are behaving as the current source and therefore I can safely say that IDSn will be equals to the – of IDSp and therefore IDSn + IDSp will be always equals to 0 and this is what the equations is all about.

So this is your IDSn assuming there is a velocity saturation and this is your IDSp which is basically a velocity saturated and therefore Kn and Kp are known as process trans-conductance parameters KN is defined as Mu N Coxide W/L of N. So if you equate this do also the manipulation and make V in = V out I end up having my expression for VM to be equals to this one this is the expression for VM right.

Where R is what? R is defined by this formula Kp / Kn means basically Mu p Cox W / L of p divided by Mu n Cox W / L of n right. So if you look very carefully if you assume that oxide thickness for both NMOS and PMOS are equal lens are also equal because lens do not change it is width which we play with I will actually see that Kp / Kn will actually boiled down to Mu p Wp / Mu n WN this equals to R multiplied by of course VDSAT N and VD SAT p.

So if I assume that VDSATP and VDSAT N are equal I will have just this ratio to control in order the value of Vn fine and let us see how it works out. We very well know therefore that the mobility so if you want R to be equals to 1 and if I assume that **you're** your VTn = VTp right. If I assume R to be = 1 so just to give you an idea about what I am talking about here.

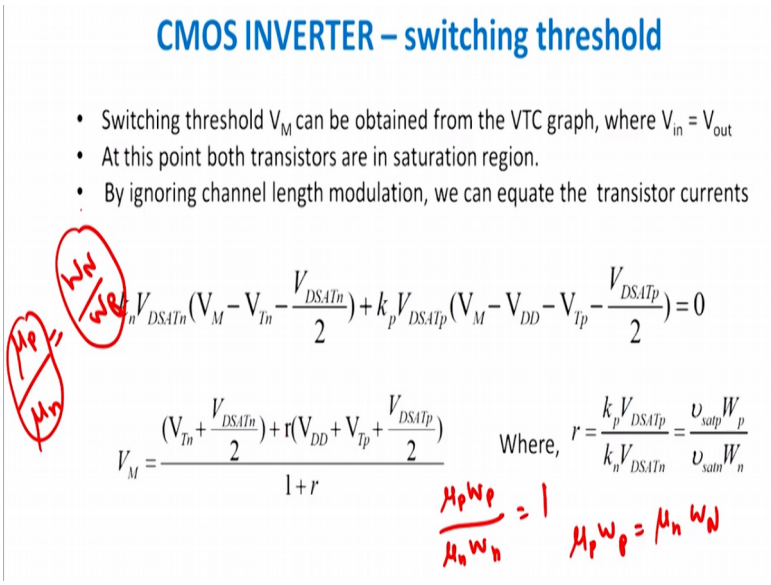
(Refer Slide Time: 07:07)



If I assume that R = 1 right so this becomes equal to 1 assuming VTn = VTp so they are opposite inside as I discussed with you threshold voltage will cancel out because VTn = - of VTp assuming this to be true that they are symmetric bodies we will have and also assuming that VD satn = - VD sat p again because there are NMOS and PMOS.

So this will get cancelled out I will left with VM = VDD 2 because R =1 so 1 + 1 = 2 I get V = 2 VDD / 2 which means that if I assume R to be = 1 my switching threshold is just half of the VDD it quiet interesting observation that if you want the switching to be symmetric that means both 1 to 0 and 0 to 1 transition to be symmetric try to keep your the switching threshold at half the VDD value right. And you will automatically get a faster switching rates available to your but when it is R = 1 you have to be very cautious.

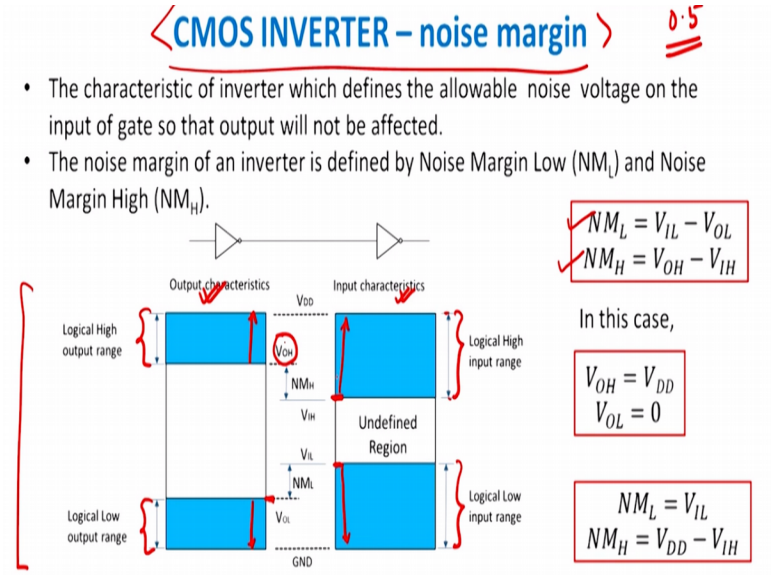
(Refer Slide Time: 08:13)



When it is R = 1 as I told you I get Mu p Wp /Mu n Wn to be equals to if you want to assume to be equals to 1 then I get Mu p Wp must be equals to Mu n W n right now but they which automatically means that Mu p / Mu n = W n / W p. Now the mobility of the electrons approximately 3 times that of the holes. So if this **3** 1 / 3 times here this will also 1 / 3 times which primarily means that my PMOS widths should be made at least 2 to 3 times larger than NMOS widths.

In order to have a symmetric transition from 1 to 0 and 0 to 1 fine so we recapitulate one small point switching threshold is where V in = V in = V out. First symmetric switching is VDD / 2 I require that my PMOS width should be approximately 2 to 3 times or the other NMOSFET's. With this we come to the third part of our talk here third part of our design here and what is known as the noise margin right.

(Refer Slide Time: 09:21)



What is the meaning of noise margin is? This is the amount of voltage noise voltage which the inverter can reject so that the output is not affected which means that the amount of noise which the inverter can reject without effecting the output right is define as my noise budget. So if I say my noise margin is 0.5 volts it effectively means that 0.5 volts of input noise it will easily reject.

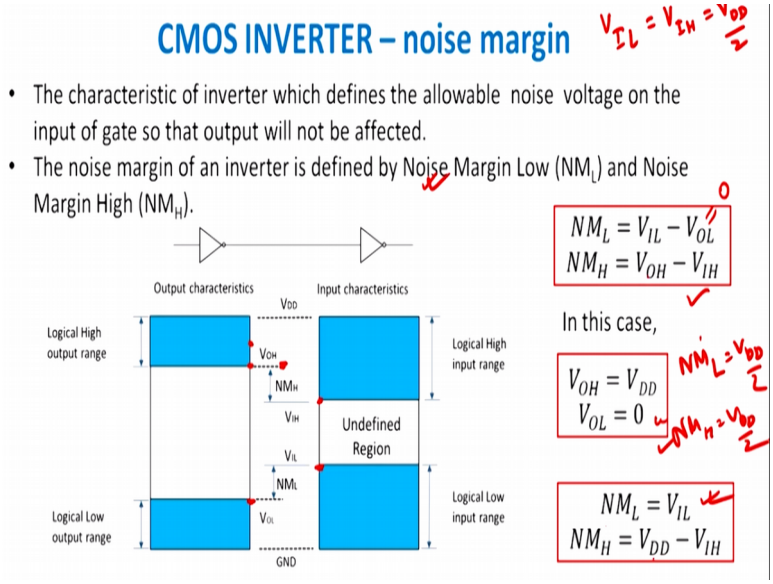
Anything larger than 0.5 volt will actually make my input go to a higher value and therefore there will be a switch in output side right. So your so higher the value of your noise margin better is the capability inverter to actually reject it or remove the noise and make the signal noise ratio's higher. Now take two types of noise levels available one is known as NML low noise level and we have NMH which is high noise level.

We defined two quantities here and these are two important quantities here so if you look at this graph here which you see in front of you this graph here right if you look at this graph here this is the input characteristics this one and this is my output characteristics right. So if a input is high VIH is input high VIH I stands for input H is for high VIH is input is high VIL is input is low then I have VIH input is high I get VOL out low.

So for when input is high VIL I get output low and if I go on increasing the voltage in this direction the voltage will go in this direction right. Similarly when my input is low VIL right then my output is high VOH out is high and if I go in this direction low I go in this direction high right. So I have band of voltages which explained to me that I have logic low level input range I

have a logic high level input range and this is your logic high level output range and this is logic low level input range fine. But then the problem comes that so we define high noise margin NMH as the difference between VOH and VIH.

(Refer Slide Time: 11:46)



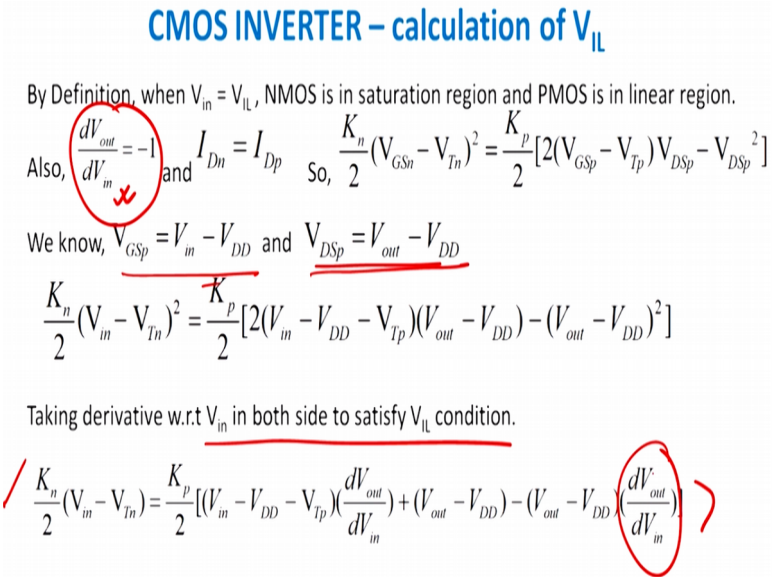
Which means basically the difference between this point and this point in voltage domain right this difference between the two and we define NML as the difference between VIL and VOL between these two levels right if this level NMH is very high it effectively means so I will give you an example if this is very high say VOH was basically here and VIH it was where it was so differences become higher.

Which means that for input low VIL I will get a swing of output voltage much closer to VDD and I can therefore reject the noise which is there inbuilt in the input side. This is a very a important discussion or a domination of a noise margins that whenever my input is low my output is very high input is high output becomes low and difference between them is basically this one.

Now ideally if you look at this case for this case we have discussing here I know that VOH output I will be ideally VDD and input output low will be = 0. So if I feed this values here I get NML = VIL – VOL since VOL = 0 I get NML = VIL and if NMH = VDD because VOH = VDD I get VDD – VIH right. So the low noise margin = VIL input low what is the value of input low it is 0 again the minimum I can go is basically input low is a I can go to 0.

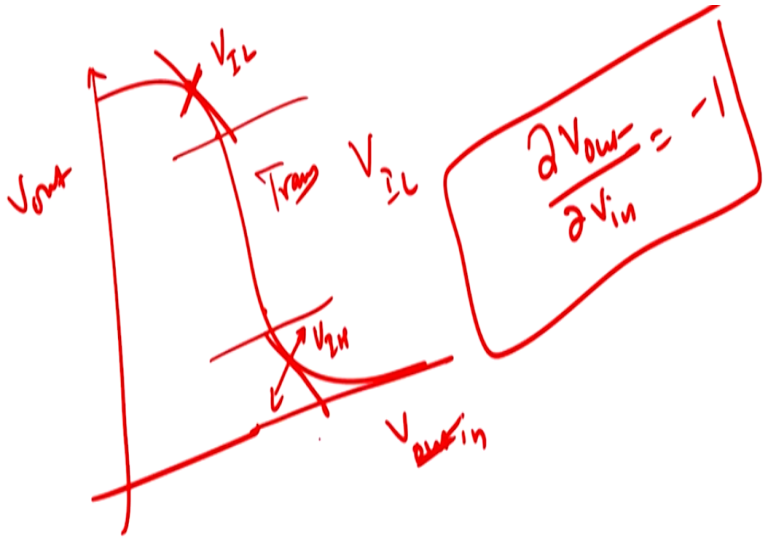
So ideally I can NML is also = 0 so we will not discuss that point at this stage but I forget VIH here now quiet interestingly if I am able to make VIL = VIH = VDD / 2 then you see NML also becomes now equals to VDD / 2 and NMH also becomes equals to VDD / 2 the noise margins are exactly equals and this is the most ideal state of affairs where the high and low margins are equal which means the noise related to one will be also rejected in the equal probability as noise related to 0 that can only occur when I assume that VIL = VIH right and we can have that equals to VDD/2.

(Refer Slide Time: 13:59)



Now how do I calculate VIL by definition VIL there is a reason why we can do it.

(Refer Slide Time: 14:13)

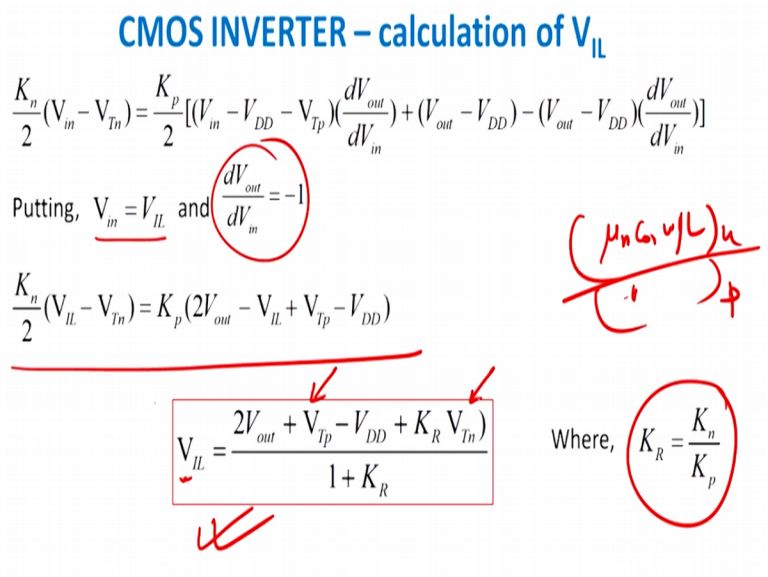


But the definition states to me that VIL can be found out or can be understood VIL can be understood where if you have plot the voltage transfer characteristics right this is V out say versus say this is V in V out and this is V in let us suppose this is V in then we find out two points right where DV out DV in = -1 right. Where you have DV out DV in = -1 that is the point where you will see a transition of input low and input low VIL right.

So just to show you so therefore this is what we have studied DV out = DV in anything larger than that you will have problem and the problem is what? The problem is that if you have anything larger than that you shift to this region or to this region in this region you see first small change in input you will get a large change in output not a stable condition and therefore there is a reason not a transition region as I discussed with you.

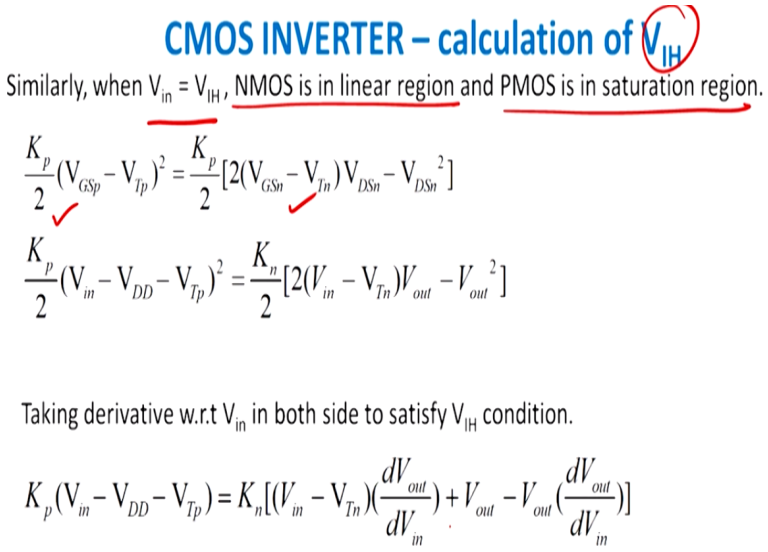
Therefore this is a boundary sort of at edge where we define VIL and VIH input low and this is VIH high right this is V in versus V out. So I define VIL and VIH at DV out = DV out DV in = -1 and that makes my life easier. If you solve it and we do and therefore we get VGS = V in – VDD and VDS = V out – VDD. If you satisfy both of them and if you write a if you take a derivative with respect to Vin from both the side and satisfy this condition as well as satisfy this conditions. I finally get this expression here now assuming DV out DV in = -1 I fit the value directly in this case.

(Refer Slide Time: 15:59)



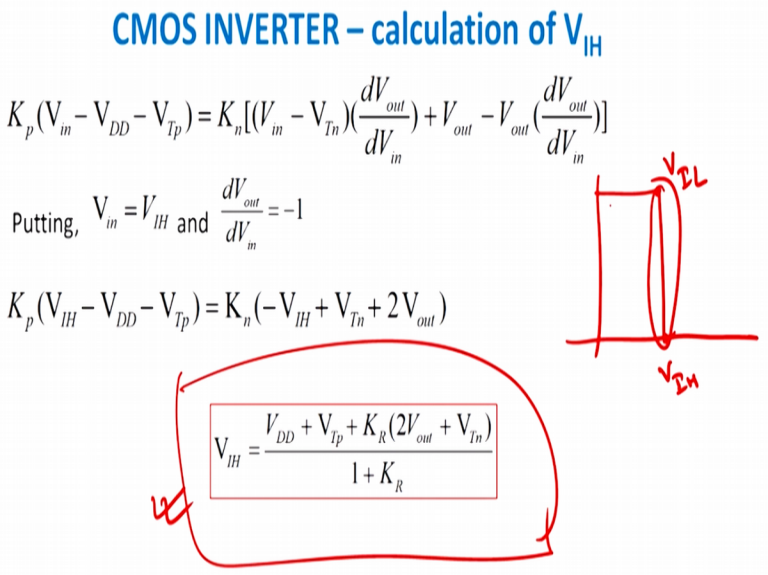
And what you finally get is putting V in = VIL and DV out = DV in = - 1 I get this expression from there I get the VIL = this expression and therefore VIL = 2 V out + TP threshold voltage of the MOSFET – VDD – KR into VTL right KR into VTL will be available here. Where KR is Kn / Kp where Kn / Kp is basically Mu n cox oxide W/L of W /L of N divided by same thing of our P. So this is by this is my VIL which I have (()) (16:38) say for VIL is depending on threshold voltage of PMOS it depends on the threshold voltage of NMMOS and the relative values of W/L ratios of NMOS and PMOS which is quiet interesting we will see later on as we move ahead. Now how to calculate VIH? Since we know VIL was the same concept DV out DV in = -1.

(Refer Slide Time: 17:00)



Here Vin will be equals to VIH right and we also assume that please remember where I was calculating VIL at that time NMOS was in saturation region and PMOS was in linear region but where I am calculating VIH which is this one my NMOS is in linear region and PMOS is in saturation region fine. So now i have to put this two equations in after equated derived del V out del V in I have to derive assuming del V out del V in = 1 – 1 and V in = VH.

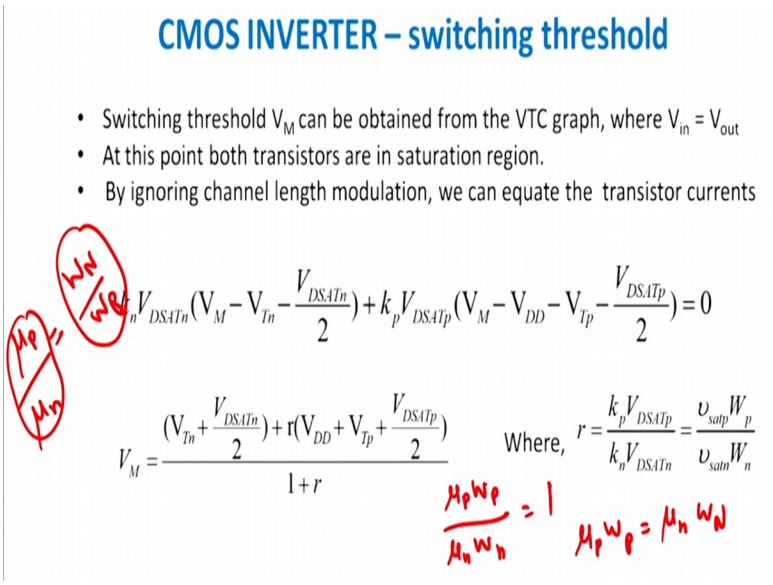
(Refer Slide Time: 17:33)



We get this expression finally as this one which we get for VIH right we get for VIH again it is depending on value of VTN, VTP and KR and KP. Now in you want to just have a look into all these issues here you will see that VIH is depending on the value of VTP so what I will tell you is that if you make your VTP large that means the threshold voltage of PMOS large right you automatically get a VIH is very large which means that VIH starts to shift in the X axis towards to right it moves towards the right.

And therefore the transition region becomes larger and larger ideally please understand you want the transition region to be something like this so ideally VIL or VIL will be exactly equals to VIH they have to exactly one on top of each other I do not want this transition as far as digital logic is concerned.

(Refer Slide Time: 18:28)



So let us look what we are happening or what is there in this case as far as this design is concerned as I discussed with you just now therefore. For KR = 1 right I get this so if I plot a graph here of super impose on this I make it like this super impose of that at this is 45 degree line going parallel to it then I can safely say that this where some nominal case this is 1.5 or on 1.5 we will get this value.

So this is the point though I have not drawn it correctly but around 1.5 for nominal case we will get KR = 1 and in that case VM will be equals to VDD / 2 provided VTN and VTP are exactly equals and everything else has been taken care of. Please understand VM / 2 can only come to you if you assume that VTN = mode of VTP which means the threshold voltage are equal and the R value = 1 which means that the width of PMOS is made three times larger as compared to NMOS.

Then only you get a symmetric design otherwise you would not have symmetric design now with this knowledge or with this idea what we can do is if we say I have good PMOS primarily means that my PMOS aspect ratio W / L is made larger if it is made larger my KR reduces as the KR reduces my VN starts to become higher and higher and therefore the whole graph shifts to the right? And therefore the VM shifting is there similarly when I say good NMOS I mean to say by aspect ratio of the pull down device is higher and therefore VM reduces and therefore the VM reduces and therefore this becomes a.

So KR in this case the KR becomes less than 1 in this case KR becomes greater than 1 fine so you see very clearly that depending on the process parameter variation primarily W/ L ratio I can slightly shift the value of VM but I cannot shift it drastically high or low right. So please understand VM is the quantity which depends upon the process to a larger extent I will on the structure of the device sorry not on the process but the structure. I will just show you the concept of VM is using till now.

(Refer Slide Time: 20:54)

CMOS INVERTER – switching threshold

- Switching threshold V_M can be obtained from the VTC graph, where $V_{in} = V_{out}$
- At this point both transistors are in saturation region.
- By ignoring channel length modulation, we can equate the transistor currents

$$k_n V_{DSATn}\left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right) + k_p V_{DSATp}\left(V_M - V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right) = 0$$

$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1 + r}$$

Where, $r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{\upsilon_{satp} W_p}{\upsilon_{satn} W_n}$

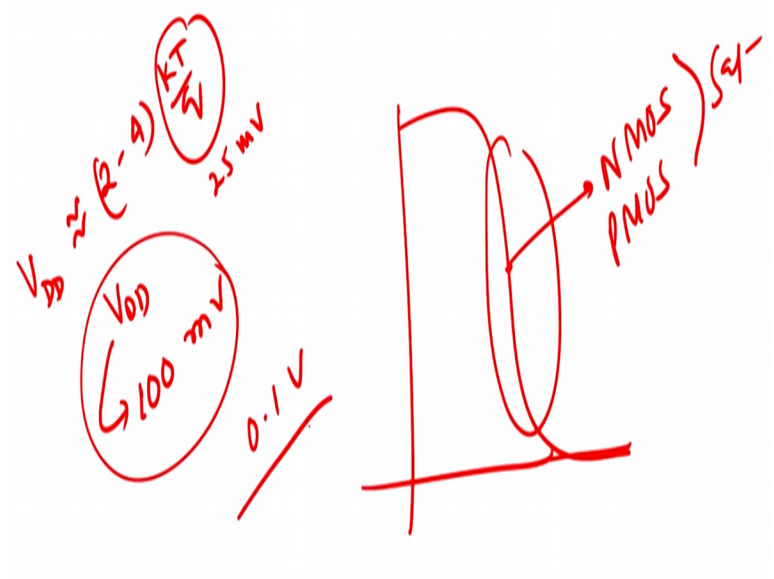
If you see this graph here for this expression which I was discussion with you earlier this expression see VTN and VTP are fixed by the device VT SATn and VDSATp was fixed by the device. So once the device have been fabricated you cannot do a change in that you are left with R. R is depending upon this quantity in this case your W / L are fixed R is also fixed VM is fixed.

Which means that once the device has been fabricated on chip you have no way at this stage to make your switching threshold change drastically right and that is the important point I wanted to raise a this stage of time right. We come to the last part of the section and that part is that we want to find out the channel gain. Channel gain is primarily what do you mean by channel gain it is basically del V out del V in is basically defined as my channel gain right.

As I discussed with you the channel gain should be as high as possible so that you are able to move out of the transition region at the fastest possible which in the shortest possible time where

should we move on either to 1 or to 0 fine. So either you should move to 1 or to 0 and you will be able to therefore move this further and further away okay with this knowledge what we try to do is that so what where you are actually finding at the voltage gain at the middle of the VTC middle of the VTC means what?

(Refer Slide Time: 22:16)



Where very middle of the VTC something like this that you do like this and this is middle of the VTC so if I assume it to the VTC here please remember NMOS and both PMOS where actually in saturation right. If there is in saturation I will just equate that current and VDD = 0. Assuming that channel and modulation is always there so this lambda V out which you get from here and lambda in V out is this is for NMOS and this is for PMOS this is for PMOS right.

So you see lambda P into V out – VDD is what you get fine so lambda into will be actually we getting here 1 + Lambda remember it is 1 + lambda VDS. So drain to source of PMOS is nothing but V out – VDD so this lambda P V out –lambda P VD is what you are getting here. If you differentiate it and if you solve it del V out del V in I get this big expression.

(Refer Slide Time: 23:17)

CMOS INVERTER – voltage gain

Ignoring second order term and setting $V_{in}=V_M$

$$g = -\frac{1}{I_D(V_M)}\frac{K_n V_{DSATn} + K_p V_{DSATp}}{\lambda_n - \lambda_p}$$

$$g \approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

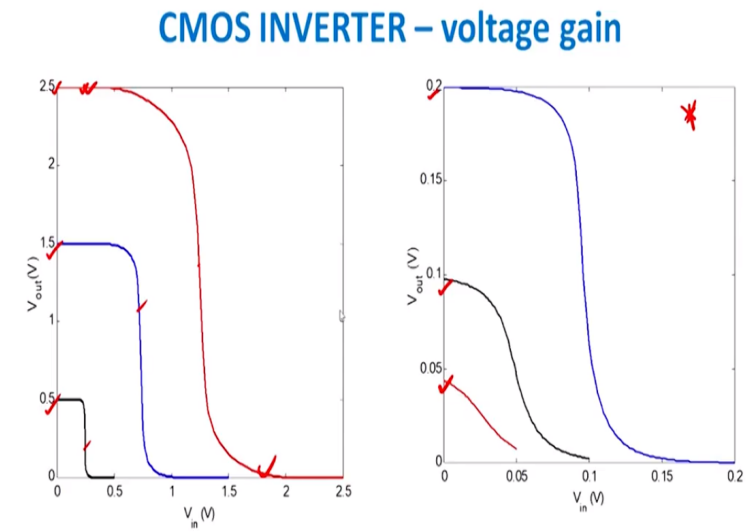
- Gain is almost purely determined by the technology parameter
- It is slightly depends on the transistor sizing ratio.

And from this expression finally assuming that V in = VM because that is where we are actually planting the design we see that G which is the gain is written as quantity right where everything is known to you lambda and lambda P are known to you R is origin but the previous slide discussion already know to you VM is known to you also know VTn you also know VDSATn available to you from there you can calculate the gain.

Quiet interesting gain, gain again is again governed by transistor parameter so process technology parameters. So lambda, lambda p again process system this is process dependent this is again process dependent so gain is process dependent which means that once there been fabricated electrically you do not have a any ways of changing the gain drastically but I will release an exercise to you can you do that by the knowledge you have gained till now you can have a methodology by which you can change the gain even after there have been fabricated.

Just think about it it was discussed in the previous lecture on this issue I give already done this issue. This is the last slide before we conclude this this part of the topic is that assume therefore make your so if you go back in the previous slide it also this G gain dependents upon the value of VM it depends upon the value of VTn and it depends upon the value of VDSATn.

(Refer Slide Time: 24:45)



Adapted from Digital Integrated Circuits (2nd Edition)- Jan M. Rabaey

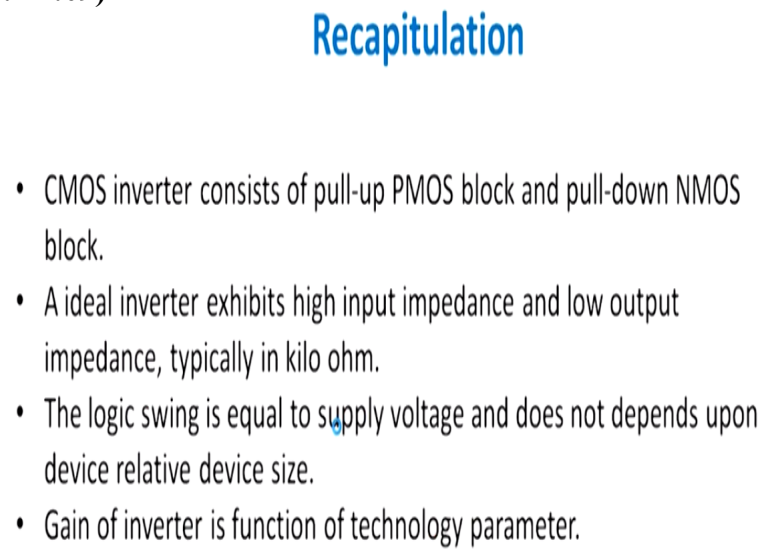
Now let me plot for you V out versus Vin right for various values of VDD so what I do I plot for 2.5 then I got for 1.5 then I go for 0.5 right and I go for 0 .2 this is 0.1 and 0.5 so they are in all continuation this to have increased the scale so the visibility of this graph is better. If you look very closely here as the VDD is dropping down right as the VDD is dropping down **so is** so is this this transition right so the transition between high to low is also faster in case of 1.5 at this much faster steeper in case of 0.5.

So lower the VDD right higher is the gain because the steepness of the curve actually becomes larger and larger in this case right and you are able to do steep thing. The price you pay for it is that your noise margin are reduced noise because noise margin is directly depend on the value of VDD since you are reducing on the VDD your switching speed will increase possibly but your noise margin are reduced drastically but if you increase if you reduce the VDD beyond the particular point please understand if you reduce your VDD we are also reducing the current charge discharge the capacitor.

If you reducing VDD you are also reducing the current to charge the capacitor therefore it is take the more charge the capacitor. So at the cost of noise margins you will actually have a reduced value higher value of your delay will be there because of because of lower current to flow right. Typically what people have shown is that typically value the which you have shown is that typically you can go up to VDD which is approximately equals to 2 to 4 times KT / q right.

KT / q is approximately 25 milli volts right so 2 to 4 means 100 mili volts so typically so if you can go up to VDD = 100 milli volts. Anything lower than this you have a problem that the problem is that the threshold voltage is very small very close to VDD and therefore there will be no even switching between high to low and low to high. So the typical standard is you maintain minimum up to 100 milli volts which is basically 0.1 volts is the minimum which you can go higher than this better it is in terms of noise margin in this case right.

(Refer Slide Time: 27:09)



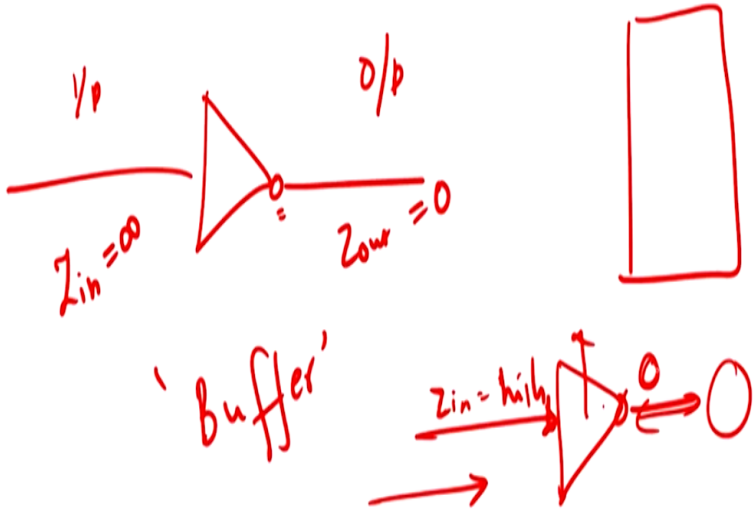
Let me recapitulate what we have done till now we explained to you what do you mean by CMOS invertor how it works out. We will also understand what is the pull up network pull down device pull down device pull is PMOS pull down is NMOS we have understood an ideal inverter we will have an high input impedance infuriately high and a low output impedance and therefore there also used as buffer we will just discuss that point.

Logic swing as I discussed with you will go from VDD to 0 so when my PMOS gets ON my output load goes to VDD NMOS which is also goes to 0 so the swings are very high and therefore the logic levels are also fully satisfied then it go to high logic levels. Very important when you do very large fan out circuits and a does not depend upon the relative size of the devices. So whatever sizing you do the functionality of the CMOS inverter does not get affected.

Yes, what gets affected is of course the delay all those things noise margins slightly but not the functionality of the inverter. The last point is that the gain voltage gain of the inverter is always the technology dependent quantity right it is always depending on the type of technology you are

using or all practical purposes. One point which you should be careful about or you should know about is that and which I have left is that.

(Refer Slide Time: 28:31)



Invertor can also act this is the size of the inverter which we were discussing so this is my input right and this is my output and you put a small circle in front of it this is got therefore Z in in infinitely high and Z out is infinitely is approximately goes to 0 and therefore they can be used very well as buffers right (()) (28:50) buffers. Buffer is what? Is basically for matching impedances at the output source.

So typically the chip input chip is very high impedance if you have therefore it goes into inverter then this I will Z in will be equal to I which will basically mean that the signal coming here will be very easily transfer to inverter and since output of a chip is very low input impedance output impedance so this is also low they will easily match. So load matching will be very well at the IO of a design and that is the reason we generally refer to the fact that inverters are also very good buffers and most of the inverter chains are used in buffer designs also. So with this we come to an end of this lecture and we will start the next lecture subsequently out of this thank you very much.