CMOS Digital VLSI Design
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Module No # 01
Lecture No # 05
CMOS INVERTER BASICS – I

Hello everybody and welcome to the next session of NPTEL online certification course on CMOS digital VLSI design. This module is primarily named as CMOS inverter basics and this will be part 1 and we will be also dealing with the other features of that in the second module for this course. What we will be doing in the subsequent slides I will just give you the outline of the whole module which is approximately 45 minutes to half an hour.

Primarily we will be looking at the CMOS inverter now CMOS inverter is the main workhorse of all digital VLSI circuit design which primarily means this is one structure or a circuit which helps you to do a 1 to 0 and 0 to 1 transition at a very fast pace. What we will be also looking is into is basically two things so we will have a basic look at the basic idea of inverter CMOS.

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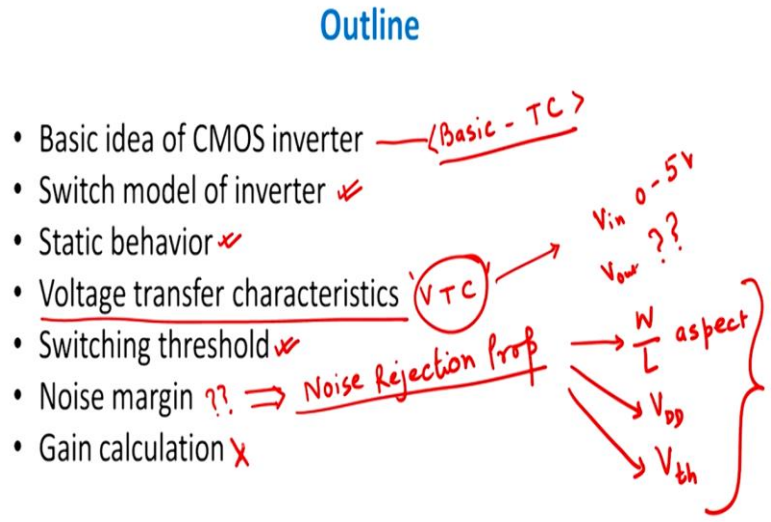

So this is basic idea means it is functionality and it is what is known as the transfer characteristics. So we look at it basic characteristics and transfer characteristics after you understood this part we will have a look at the switch model of an inverter which means that

given an inverter right can I do some approximations in the inverter so that the understanding of the transfer characteristics is relatively easy for all of us.

Without compromising on the output characteristics of the device after having done the switch model of the inverter we will actually go for the static behavior analysis. Static behavior primarily means that if you give a DC bias how will the output voltage change with respect to the DC bias for an inverter. We will also look into the fact that how therefore we will be able to design a draw a voltage transfer characteristics which means that if the input various from 1 to VDD or 0 to high voltage how does output vary?

So this VTC is primarily means that if I am varying input from say 0 to 5 volts then how my output is varying in what fashion. So this is what we are supposed to do as far as voltage transfer characteristics of the device is concerned. Once you understood the VTC or the voltage transfer characteristics of the device we should be in the position to explain what is the meaning of switching threshold what is switching threshold is very important characteristic just like the threshold voltage in the device which we have understood in the previous lectures.

Switching threshold is defined as that voltage at which the transition between 0 to 1 and 1 to 0 takes place right. So we will define what is switching threshold and we will see how can we calculate the switching threshold from the VTC of the device. So if I know the voltage transfer characteristics how do I know the switching threshold of the device. Then we be actually looking at what is known as the noise margin right.

Very very important property of the inverter which primarily means that if you have if you input a signal on to your inverter any signal will obviously have a noise right electrical noise are inbuilt inherent in all the signals whose origins are varied so it is variety of noise which will be there for example Gaussian,1/f noise will be, there will be shot noise will be there and something will be because of the wiring which carries the signal because of that they will be some noise there will be junction noise and so and so forth.

And our job will be the very stage will remove the noise as much as possible right because if we put it into the amplifier and try to amplify the signal the noise also get amplified at the same amount. So I need to reject noise at a very early stage of my processing right so that signal to

noise ratio are higher at later stages which therefore comes to an important issue of a CMOS invertor that is inverter intrinsically is a very good noise rejecter.

So what you will be understanding in noise margin is basically what is the meaning of noise rejection property right. So this is the noise rejection property of an inverter and this noise rejection property means that how I can able to reduce the noise or remove the noise at a very easily. We will also see how this noise margin or the noise rejection property is related to the applied voltages related to the aspect ratio but what is mean by aspect ratio as discussed in the previous term this is aspect ratio right.

We will be repeat this how it is related to VDD which is the applied voltage how it is related to the threshold voltage of the device and so on and so forth. So once why we are doing this then we can actually manipulate these things these properties and achieve a very good noise margin for us right. So that we are able to achieve a very good noise rejection. The last part of the outline of the whole talk will be we will be looking at the gain calculation right.

And this is quite important because CMOS structure or the CMOS inverter has been the main state not only for digital design but for analog design as well and we will I will discuss with you why gain calculation is important? What do you mean by gain?

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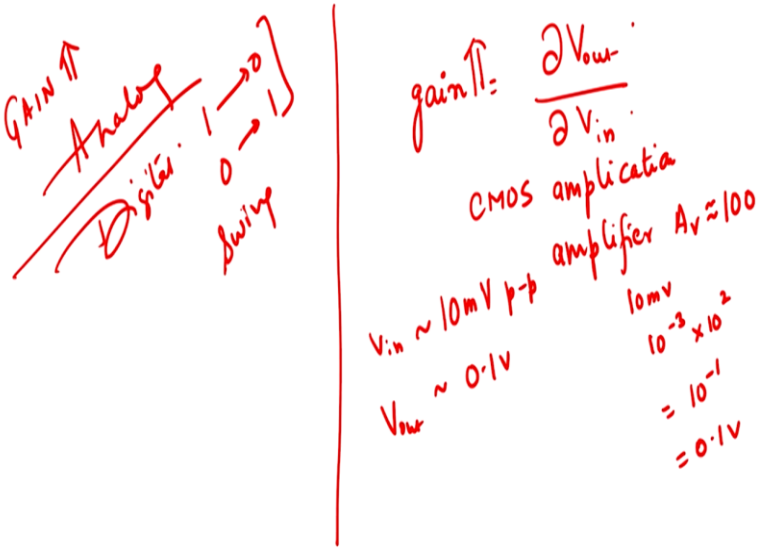

Gain as the word suggest gain basically means rate of change so it is basically del Vout del Vin right. So how much change in the output is there because of the change in input. Now if your gain is high I can use the CMOS for my amplification purposes also right CMOS I can use as an amplification or as an amplifier right I can use it as an amplifier for all practical purposes which means that it is voltage gain AV which is voltage gain maybe if it is 100 let us suppose that if I give a input peak to peak stream of say 10 milli volt which is 10 to the power -3 volts then the output will be 10 to power +2 which is basically = 10 to the power -1 which is just equals to 0.1 volts.

So basically meaning that at 10 milli volt milli volt peak to peak input will result in a Vout of approximately 0.1 volt for this CMOS which means that I can use the CMOS both for analog design as well as digital design why for analog design? Because there I can use it as a amplifier for amplification of analog signals and we will see how it will be used for digital signals right. This is one thing which we should be careful about the second thing is having a better gain or a large gain also allows for the inverter to swing from 1 to 0 and 0 to 1 and a much faster pace. So your switching speeds are much higher between 1 and 0.

So having a gain which is high not only helps you for analog designs but it also helps you for digital design why because in digital design your 1 to 0 and 0 to 1 swings these are very good swings because it will move very fast because the gain is very high. We will see in the subsequent slides how it works out right so I hope I able to explain why gain calculations is very important. With this basic outline of the whole talk or the basic idea let me go to the next slide I will explain to you the basic inverter it is a very important and it will remain with that for the whole module till will finish of this course in CMOS digital VLSI design.

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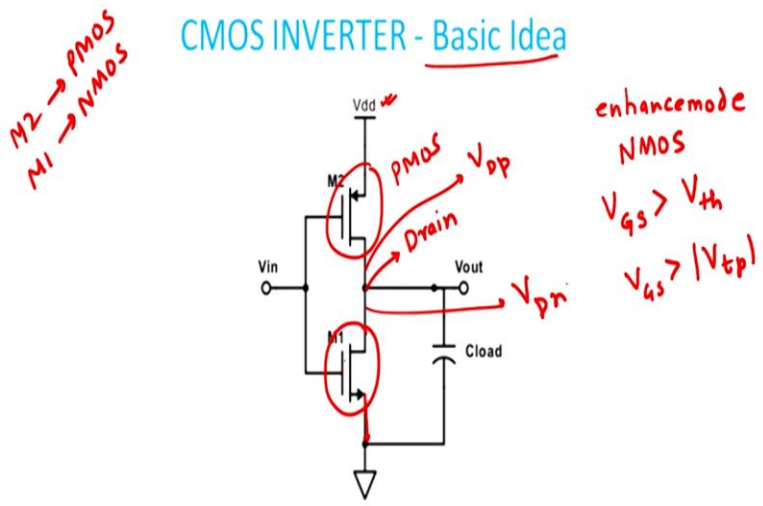

Figure : A static inverter with capacitive load

If you look here closely this is the basics idea so this is the basic idea and I will I will explain to your how this works out. See if you look very carefully we have discussed in our previous term in a previous lecture that if I am using an enhancement mode MOSFET and if it is an N channel enhancement mode MOSFET and if it is at N channel which is an NMOS I require a gate voltage right remember should be larger than the threshold voltage of the device for to make it all for an NMOS.

For a PMOS i require it to be less than or equal to should VGS should be greater than mode of Vtp which is basically mean that threshold voltage of the P type device right. And if it is so I will be able to achieve it is switching ON and OFF condition. So let us see how does it work as a inverter so what is that this is basically a PMOS so this is a PMOS here right it connected it is source is connected to VDD right as where discussed earlier we have an NMOS here whose source is connected to be ground and we have whose gates of M1 and M2.

So M2 is basically your PMOS right is PMOS and M1 is your NMOS right and I am giving input to the gates of M1 and M2 right. So please understand for all practical purposes in the input signal in most of the cases in digital VLSI design will be given to the gate side of the device. So the gate will be primarily responsible for taking the input signal right and you will in most of the cases where example in this case in front of you.

You will have a output at the drain of the two so this is basically the drain of PMOS and the drain of NMOS are together they are shorted with each other. So the drain of this is basically your drain of PMOS and this is your drain of NMOS and they are shorted together and we will get an output. Let me show to you therefore with the idea how does it work as a device which is at a inverter what is the inverter basically mean?

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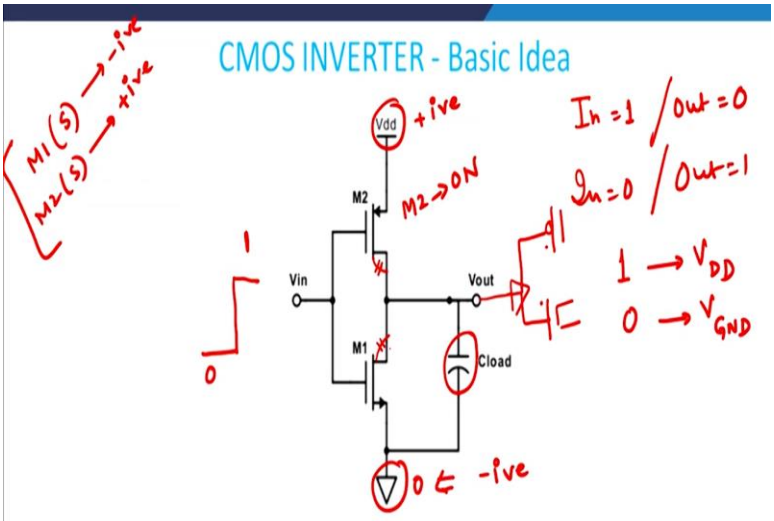

Figure : A static inverter with capacitive load

Inverter means that if you give an input 1 if I give an input = 1, I will get output = 0, if I give an input = 0 I get an output = 1. So this basically means it inverts the signal right please understand when we say 1 it corresponds to VDD which is the applied voltage here right and 0 corresponds to VGND right so ground which you see here is just happens in a ground is 0 and this is a positive voltage.

Please keep in mind you can also encounter inverters where this ground can be actually a negative voltage but you have to always make sure that the source of M1 right. The source of M1 source should always be to the most negative terminal please understand and M2 source should be at the most positive terminal of the whole system if you want to do work it properly. With this knowledge let me there for explain to you how it works out. As I just now told to you if I give an input of 1 I get of output 0 if input of 0 I get an output of 1 so let us see how it works out.

So let us give you an input transition from 0 to 1 right 0 to 1 fine so initially I had an input way from which is basically 0 and then I do a transition and go from 0 to 1 let us see how it works

out. When it is 0 please understand M2 will be switched on right let us suppose do the capacitance here now this capacitance we will discuss later on but primarily this capacitance is defined as the load capacitance and it effectively takes care of any capacitance occurring between gate and drain here CGD of PMOS.

It also takes care of CG this here NMOS gate to drain it also takes care of the next stage inverter design which means if you if you drive a next stage inverter then it looks something like this right it looks something like this. So input capacitance is here and the output capacitance is here if you add all those together we get C load available here with this what we therefore we come to the point therefore.

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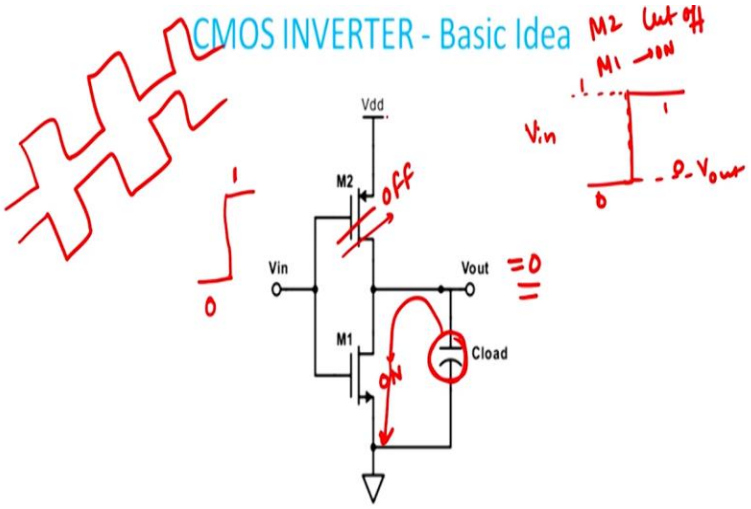

Figure : A static inverter with capacitive load

Therefore if I give 0 to 1 transition here I get if I get 0 here M2 is switched on from my basic discussion which we have discussed earlier and since it is 0 my M1 is basically off when we have 0 input because for enhancement mode N channel MOSFET you require a gate voltage larger than the threshold voltage for this M1 to be on. But since the gate voltage applied is less than the threshold voltage which is 0 almost cut off.

So M1 will go to cut off so M1 will be going into cutoff and M2 will be actually switched on and therefore it will be saturation. So this will start to behave like a current source M2 will therefore behave like a current source and M1 will be cutoff and therefore it will basically a 0 nothing will happen. When it is there then this C load will get charged by which dimension by this path right.

So you will have VDD through M2 because M2 is ON charges to C load right so what i can do therefore is that I can replace this M2 by a simple resistance and I can therefore make this as a open switch we will discuss this the next slide only but this is what we can do. So this is the RP and this goes to VDD which means that capacitance is getting charged to a high value when my input is 0 which means that this voltage here will actually go to high value why?

Because capacitance getting charged so as long as your input is 0 my output will always be equal to 1. Am I clear? This is the charging process right let us look at the other side of the story. Now let us suppose it goes from 0 to 1 right as it goes to 1 just the reverse happens in this case what reverse happens? Reverse happens is that suppose I am going from 0 to 1 and i can go to 1 here from 0 then M2 goes in the ON state because threshold voltage is large than the gate voltage is larger than threshold voltage M1 goes to the ON state at M2 goes to an OFF state right.

So M2 is now in cutoff and M1 is in ON state saturation state and therefore what will happen this will be cutoff right and therefore there will be no direct connection between VDD and V out but quite interestingly my the accumulated voltage across this charge accumulated at C load will find a low resistance part will actually go to the ground from this place am I clear? So what will happen to Vout? Vout will go to 0 because initially it is fully charged to 1 now it is finding at low resistance path through which can drop down and therefore V out goes to 0 right.

And therefore Vout goes to 0 which means that if my input goes from 0 to 1 this is my Vin right Vin actually my out goes from 1 to 0. So this is my Vout and this is my Vin so I get 1 to 0 and this is 0 to 1 right so this is the basic understanding of a inverter therefore given as a signal and therefore if I give a signal something like this let us suppose the clock I give right the I will start getting a signal which is just negation of that means when this is high say this is become slow and so on and so forth it will go like this.

So right and will something like this a anyway so whenever input goes high output goes low and vice versa we can have a look which means that an interesting part therefore comes to the mind that CMOS therefore can be useful for switching from 1 to 0 and 0 to 1 that is very important and important design consideration. As I discussed with you in the previous slide now let me give to you switch model of a inverter.

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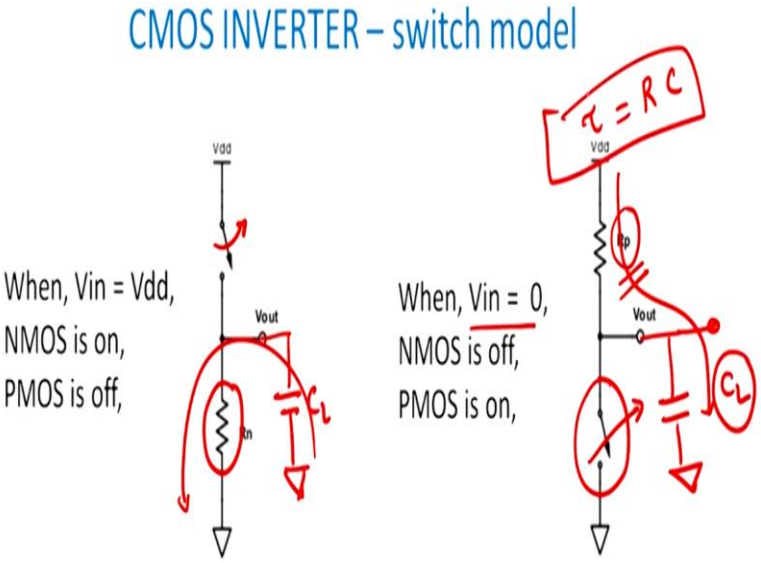

As I discussed with you in the previous state that whenever with Vin = VDD let us suppose when Vin what was Vin?

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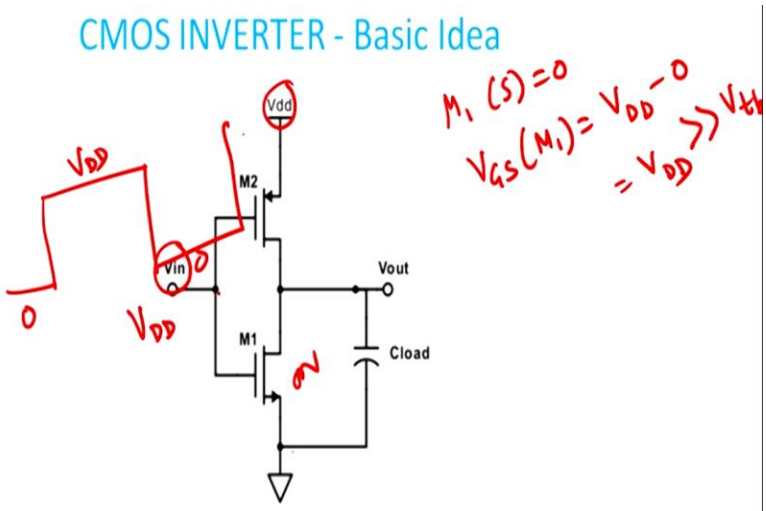

Figure : A static inverter with capacitive load

Please understand Vin what nothing but this Vin right if i give it equals to VDD right and this also equals to VDD right then gate to source because source is grounded for M1 so for M1 source is grounded. So VGS for M1 will be nothing but VDD – 0 and therefore equals to VDD which is much larger than the threshold voltage of the device therefore switch ON the device M1 right. So what I can giving here is I am giving 0 and then I am giving VDD here and I get I am going to 0 and again VDD so this is 0 and VDD right.

So if I look at this slide now by previous discussion when Vin = VDD as I discussed with you NMOS goes to the ON state and therefore it is therefore this is a direct part source and drain of the NMOS and therefore it is represented by a resistance here RN and the PMOS is in the cutoff state and therefore it is represented by a switch which is open switch in such a case. This is switch model now the reverse will happen what when Vin = 0 PMOS which is ON and NMOS which is OFF.

So I will replace PMOS by a switch or by a resistance whose value = RP and we will replace the NMOS by a switch which is basically open right this is switch model available to you. So when the switch closes down it is represented by a resistance switch opens it is a open circuit right. Please understand here you will have always a capacitance here CL right you will always have a capacitance here CL this capacitance comes by virtual of many factors which is discussed to you in the previous term.

Which means that this capacitor is initially charged through this resistance right CL and then next phase it is getting discharged to its resistance right. So it is basically a first order differential equation solution right you have 1 passive element here available with you 1 passive element which is basically CL. So you will have first order differential equation these first order differential equation you know very well to solve it you must have studied in your network theory courses and solutions will give you what is known as the delay.

Basically RC time constant RC delays right and therefore you see the importance of the switch model that first time it gives the working principles and without compromising on the output characteristics of the device gives me the value of the delay available to us for all practical purposes right. We now come to the therefore the static behavior will discuss one by one let me give you the first easy one then and we go for the difficult one.

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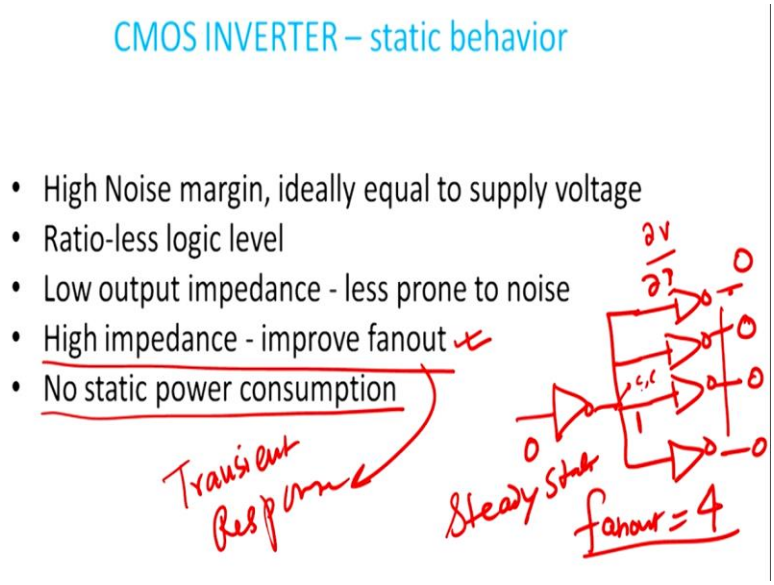

What happens is let we start with the last part but there is no static power consumption as I will explain to you what do I mean by that? Static power basically means that when the device is not operating or not switching between 0 and 1, 1 to 0 then we define that to be static operation which means that you give 1 you get output 0 or you 0 you will get output 1 and you are staying there for infinitely long duration of time then we define that to be as the static condition what is dynamic condition?

Dynamic condition is when you have repeated switching's available to you right and therefore dynamic whenever you talk of static power consumptions there is no power consumption and the reason being very simple the reason being why it is very simple because in static case you do not have any direct path between VDD and ground if you look very carefully in static case whenever you give 1 or 0 there is no direct path between the VDD and ground.

So you will never have short circuit current available between VDD and ground this is very important observation which I want to focus here that means the power dissipation levels static power dissipation levels are typically very small. Let us look at high input impedance the impedance is what? Basically Del V Del I basically input impedance now if we go back to the previous slide here and or even here if you want to go and if you look at the structure.

You see I am giving the input to the gate side of my M1 and M2 you remember your go back to basic physics of MOS device.

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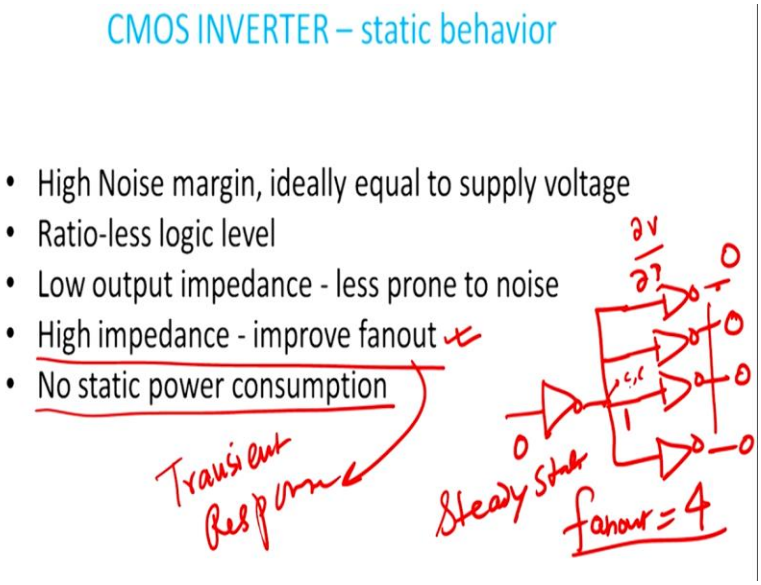

Then the gate side will have what will have oxide layer right with a very large dielectric constant. And therefore any signal which you give on to M2 there will be no current flowing in this direction or even in this direction why because your oxide thickness is so small is basically a dielectric and insulator so there will no current flowing through the device as a result Del V Del I will be infinitly high.

Which means that the input impedance of the any device especially the inverter is very very high right I will just leave a statement at this stage this will help you improve a fan out. What is fan out? Fan out is defined as the capability of a single device driving N number of large such devices is defined as fan out i will give you an example. Let us suppose I have an inverter and it drives 1, 2, 3, 4 such devices such means with same characteristics the devices are being drawn then we defined the fan out to be equals to 4 in this case right.

So high input impedance means that you can have large amount of fan out or you can have large I can tell you the reason why? See since they are all connected like this which you see in front of you and since there is not current path available between this point and this point ideally you can drive infinite number of such devices very easily in static mode not in dynamic mode please. In static mode means what I give a 0 here I get a 1 here I get a 0, 0, 0, 0, 0 here everywhere that is all I just stand there and I wait for infinite long duration of time this is the static case.

Under such a criteria, I can actually drive infinite number of devices under ideal condition in static mode. However in dynamic design whenever you are doing a transient response whenever you are using a transient. So this is the this also known as the steady state response steady state but the transient response actually is degraded I will explain to you why because of this. See the reason why is transient means what you are giving a rising or falling pulse which means that at any point of time you are now either charge or discharge a capacitor.

If your fan out is high then at this node you actually see large number of capacitance and therefore to charge or discharge a larger capacitance you require a large amount of time and therefore the speed slows down or the degradation of frequency takes place. Second this is an important point which we will be encountering as we move along and discuss in the other parts.

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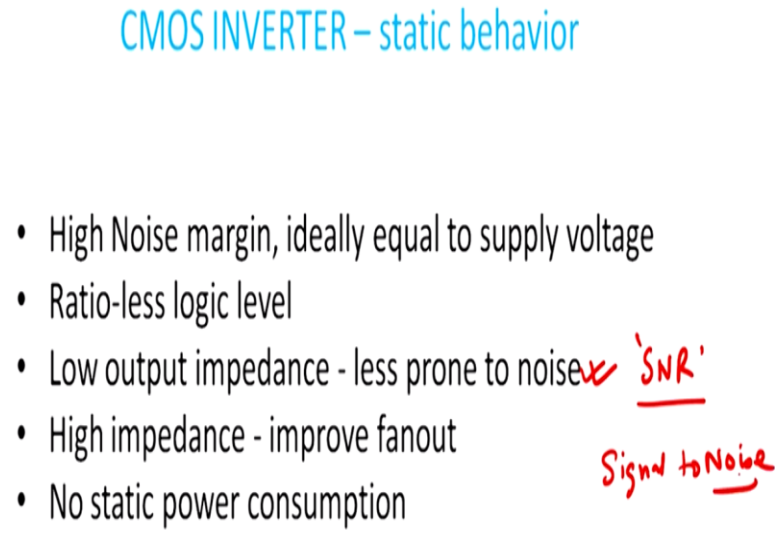

The third part is basically your this part that means output impedance is typically very low right and low output impedance is primarily means that it is less prone to noise which means that there are any noise sources inserted at the output of my NMOS it could easily rejected and have a noise free environment and therefore signal to noise ratio and at the output are typically very high right.

So this is SNR is basically signal to noise ratio right the third thing is ratio less logic level which I will put it here a very important one it tells me that it is respective of the aspect ratio of PMOS or NMOS irrespective of the aspect ratio W / L of PMOS or NMOS the static behavior is

independent of that of W/L ratio. Which means that you go on changing any W/L ratio you will still get a 0 to 1 and 1 to 0 transitions.

Which means that for any value by W/L aspect ratio NMOS and PMOS I get easily get the logic levels available to me up till VDD. So where I am going? While charging I am going to VDD while discharging I am going to 0 so please understand very very important property therefore is the first one which is this one that while charging I am going to VDD and while discharging I am actually going to 0.

So I am able to get the full swing of my signal out swing available to me and I am not wasting any of the signals in CMOS inverter so this is quite interesting and important property of this static behavior of the device just to give an idea this device there is also name for this device which is used.

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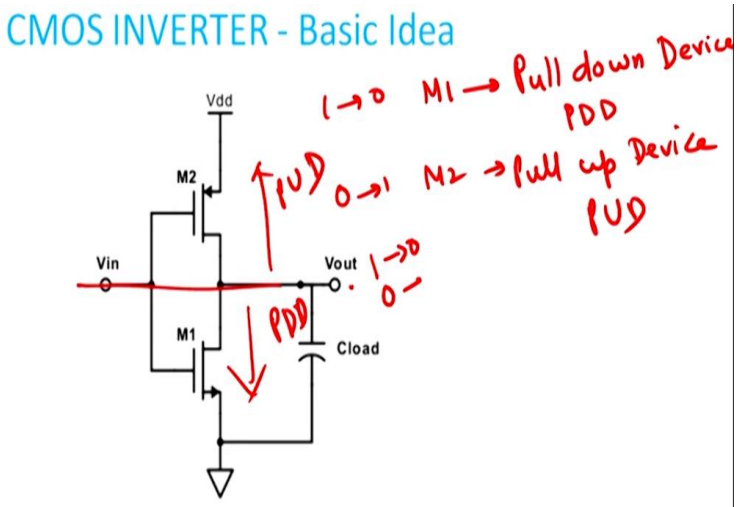

Figure : A static inverter with capacitive load

Since M1 is responsible for pulling down the voltage at V out from 1 to 0 we defined M1 to be also known as pull down device right or also refers to PDD and M2 since it is responsible for 0 so this is 1 to 0 and this is responsible for 0 to 1 so we define this as a pull up device so it is pull up device. So I have got a pull down device and pull up device everything below so the best way to notify is and we will be doing it when combination logic comes into picture.

And everything below V out is pulled down every above V out is pull up so this is your pull up network this is a pull up device and this is your pull down device or your pull down device right PMOS is the pull down device we have understood how to therefore we have understood the static behavior. Please understand I am not still not doing any dynamic behavior which means that I am not giving 0 to 1, 1 to 0 transitions I have only giving 0 or 1 and checking out what is giving in the output right.

I am satisfy with the fact that I get the full swing and I also get very important fact that the output node please understand the output node here right output node which is this is the output node right.

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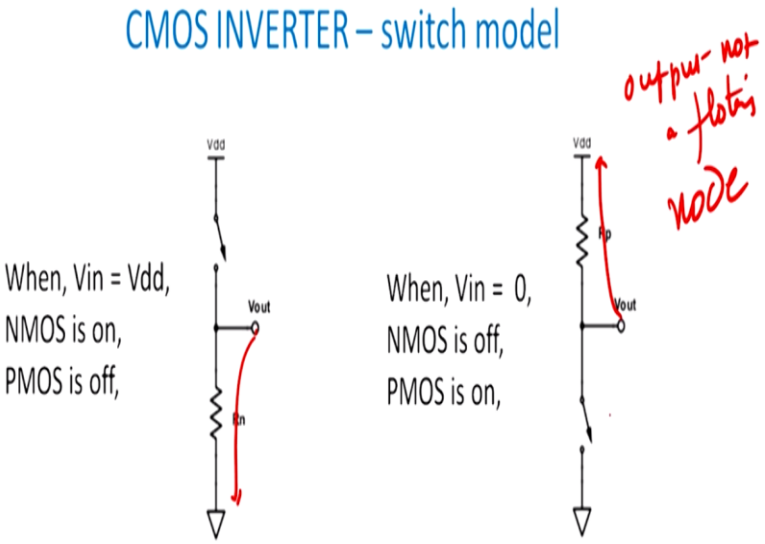

It is either connected to a ground or connected to VDD it is never floating node please understand so output node is not a floating node it is not a floating node right it is either connected to low impedance ground or to VDD both are low impedance in fact voltage source ideally output impedance of a voltage source infinitely is infinitely small approximately equals to 0 and this already ground.

So every time it swings to VDD or to 0 the output node is connected to a very low impedance node right and that also makes it very less prone to noise right. We now come to the important idea that if we have understood how a CMOS works can we try to find out the IV characteristics

of voltage transfer characteristics of a CMOS? Which means that if I vary input from 0 to VDD how does my output vary in the output phase right?

So what we will be doing is we will be varying from 0 to VDD let us suppose VDD is 2.5 then we vary input from o to 2.5 and we see how output is varying in a relative same manner right. So this is my job for next 2 to 3 slides let us see how it works out right. So what we need to do? Again coming back to your previous diagram or previous explanation you see very clearly here right.

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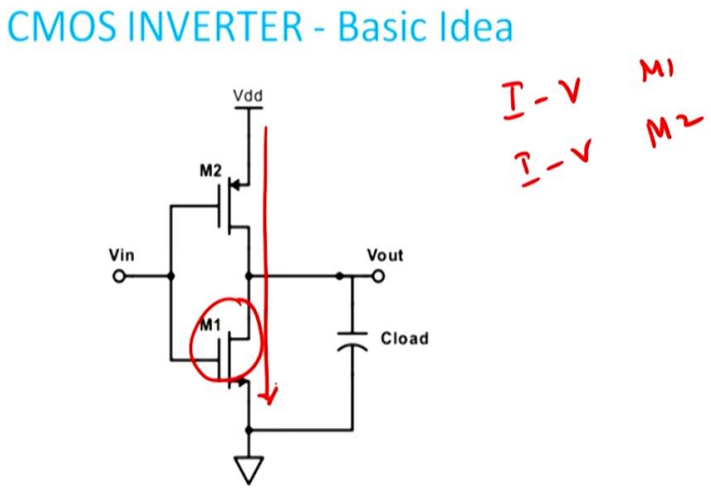

Figure : A static inverter with capacitive load

The idea is that if I able to plot the IV characteristics of NMOS right I plot the IV characteristics of NMOS. I also plot the IV characteristics of PMOS both can be easily done right then we try to bring it on the same coordinate system because please understand the VDS for NMOS will be positive but VDS for PMOS will be negative. So we have to do some manipulation to bring it on to the same scale same VDS scale right.

Once you have done that a quiet and important and interesting property is that since the current flowing through them will always equal to each other we try to find out those points in the characteristics where the current for equals for both NMOS and PMOS. Once we get those points we simply add those points and we get the voltage transfer characteristics so let me see let me explain to you how does it work out as such.

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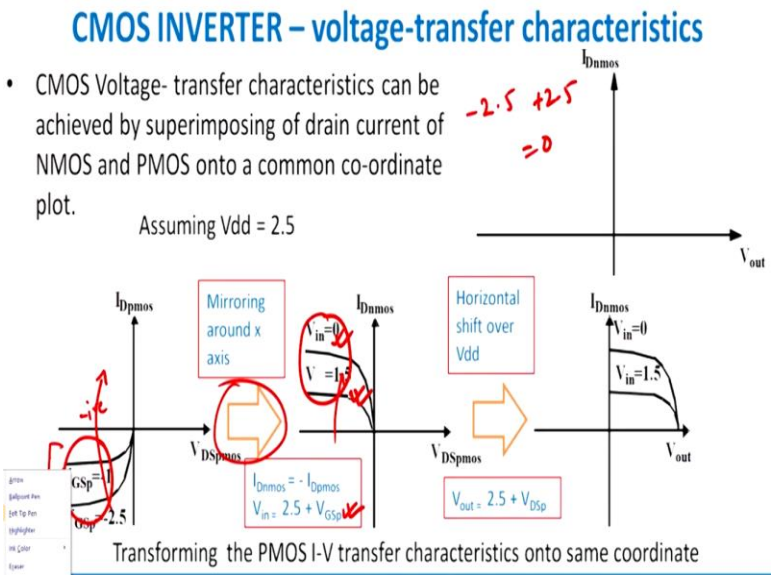

First step is we plot the graph for PMOS please understand in PMOS your VDS will be negative so this is negative side this is negative and your IDVD characteristics is also negative therefore the current is also negative this side is negative and VGSp and VGSp is – 1.5, - 2.5 which means for -1 you have smaller current and – 2.5 we have a larger current as expected from my previous discussion we will not go further then we have already explained into you in this manner.

But it is exactly almost symmetrical to NMOS apart from the fact that the access VDS is been shifted that is all looks exactly the same right what we do next step is? Look we try to find out this we do a mirroring so we do a mirroring across X axis so this is my X axis I mirror it across the X axis. So what I do? I just blank it over the X axis so what I did I blank it over the X axis. As I did the there is some governing equations which should be very careful about understanding right the governing equations are this.

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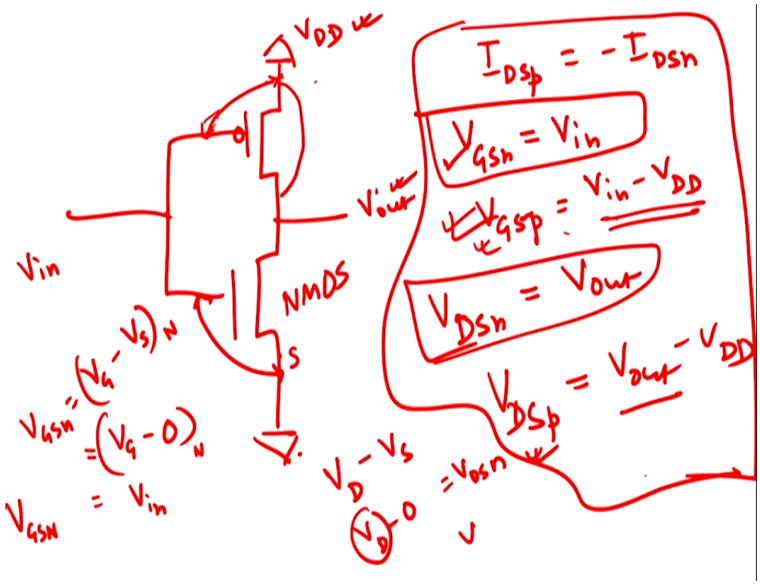

So let me say I have got NMOS here and PMOS here this is my PMOS right and this is NMOS here and this V in and this is V out right then certain governing equations should be very clear to you this is VDD the first governing equations is IDSp will be equals to – IDSn right and very true also the current continuity will always be maintained negative side because it is basically a electron and another is whole.

VGSn – Vin I will explain to you VGSp = Vin – VDD we have VDSn = Vout and we have VDSp = Vout – VDD. I will explain to you how we are getting all these terms see what is the meaning of VGSn? VGSn is gate to source of NMOSFET so I have got NMOS here so gate to source this voltage is this is grounded VGSn will be VGSn will be VG – VS of NMOS agreed if this is true then what I get from here is VG – 0 of N.

What is VG is nothing but Vin so Vin will be for the NMOS will be there so VGSn is always = V in right? So this is clear to you this is clear what we come to VDSn again very simple drain to source of NMOS drain to source of NMOS which is this one again drain to source is VD right VD – VS right so what is VS? VS is as I told you is always grounded for a NMOS because this is source of NMOS is grounded.

So VD – 0 will be equals to your VDSn but please understand VD is nothing but V out so it is basically VDSN = V out clear? So these two are very simple and basic clear let us come to this point VGSp and VDSp so if we look at VGSp this is gate to source of P type MOSFET. So I

have given Vin here so the voltage between these two points will be noting but Vin – VDD it is straight forward.

So Vin – VDD is VGSp fine this is also done let me come to VDSp is what? Drain to source for type so this gate to source and drain to source for P type is drain to source of P type right it is nothing but Vout will be there right and therefore there will be this is this will be Vout – VDD. So so finally we end up having these four equations which are the governing equations for inverter this are four governing equations for inverter fine this is first comes from current continuity and other four comes from direct idea of substitution of voltages.

If you have understood this then let us see what happens here I just now told to you that IDn = IDSp. So when you transfer from along X axis you get the same positive current as you are getting in the negative directions so whatever negative current you are getting in here you get the almost same current on this part but then please understand as per my discussion just now which I have shown to you Vin.

So if you look at V in is nothing but VGSp + VDD V in if you look very closely here so VGSp = Vin – VDD so what is your Vin? Vin is nothing but VGSp + VDD assuming that VDD is 2.5 then I get 2.5 + VGSp this equations I get this. So whatever value VGSP was once case – 2.5 so -2.5 + 2.5 if you add I get 0 and this is this one and I get -1 + 2.5 I will get – 1.5 + 1.5 I get this.

So I am able to do what I am able to convert on the X axis and change the value of gate to V in from 2.5 and 1.5 to 0 and 1.5. If you have understood these two points which are quiet simple and explainable we now do a horizontal shift along the Y axis. So we first of all did what we first of all shifted along the X axis and now we are horizontally shifting it along the Y axis right so we are doing what?

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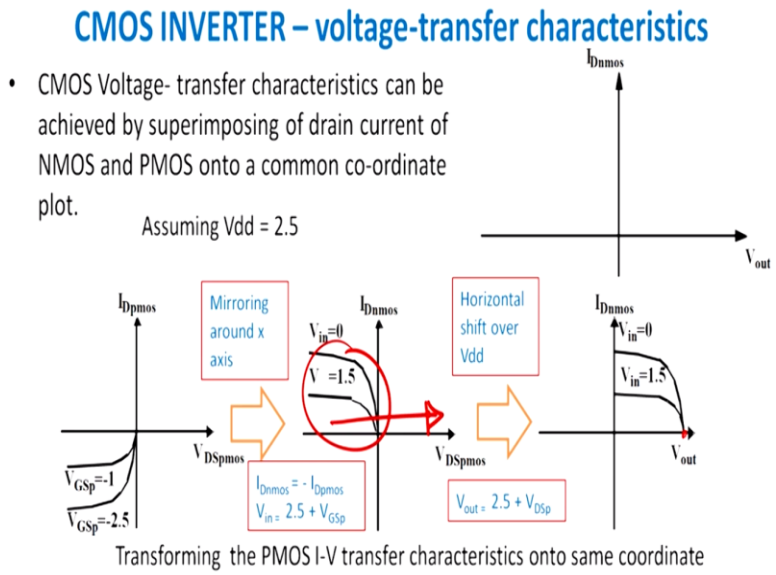

We are shifting the whole thing from here and putting it this side and we have got somewhere where right you will ask me where should I till where should I shift well look at the governing equation. If you look at this point governing equation this one you can see that Vout will be therefore equals to what VDSp + VDD fine. So if **if** this is true I get 2.5 + VDSp so what we do we just shifted to this side and you got Vout here I got shifted to this point right what does happened is have been able to shift my PMOS transfer characteristics and made it almost in the first quadrant.

Please understand my NMOS IV characteristics is always in the first quadrant and my PMOS is always in the third quadrant. So I have to move from third to second, second to first right and that is what we have got here so let me see finally what happens therefore.

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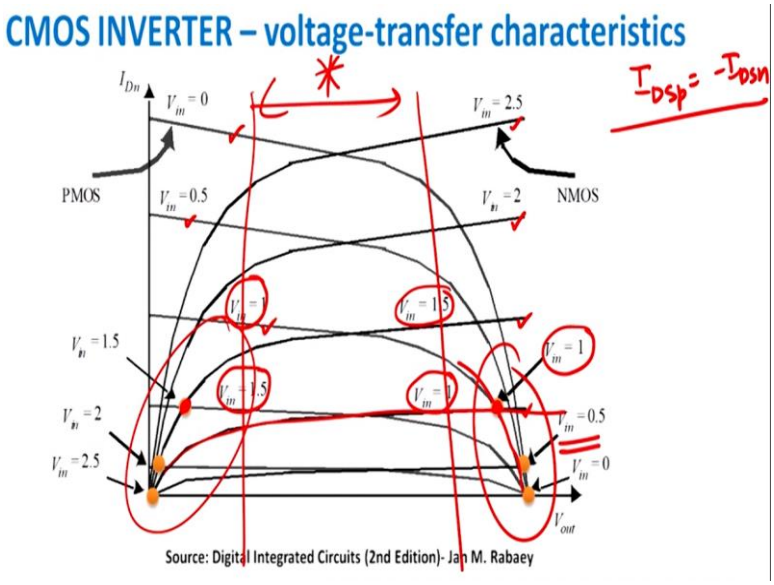

So this was an NMOS this dark line which you see in front of you are all NMOS right and we have been starting this V in = 2.5 so V in is in gate to source voltage V2, V3, V4 and super impose on that what these light lines and these light lines are what PMOS. So starting from here they are going like this now what do you do you see which point is say for example I will give an example let us say you take Vin = 1 right and you take Vin = 1 somewhere on this side.

So Vin = 1 is this one right so this is equals to Vin = 1 this Vin = 1 so this equals to Vin = 1 for NMOS right and this equals to V in 1 for PMOS and they cut where we cut somewhere here. So this is the point where gate to source for both NMOS and PMOS will exactly the same the current flowing the device will also be same. So I will get IDSp will be equal to IDSn fine. Similarly the same applies to this point also where you cut Vin = 1.5 and Vin = 1.5.

So this is the point where it cuts have you understood this point I think it is clear to you therefore why I am taking the same voltages because I because when I apply Vin it exactly applied to PMOS and NMOS the same manner and that is the reason you get something like this with this knowledge or with this idea let me some to therefore the basic concept of the voltage transfer characteristics.

And the basic concept therefore is that we will have therefore only those voltages which are either low or either very high. There is no voltage or no current in this region please understand this region devoid of any transfer characteristics. So either it is located here or located here with

this knowledge we will just discuss this and stop here for this lecture that we will have Vout versus Vin right and you have to plot those points where you get the same amount of current.

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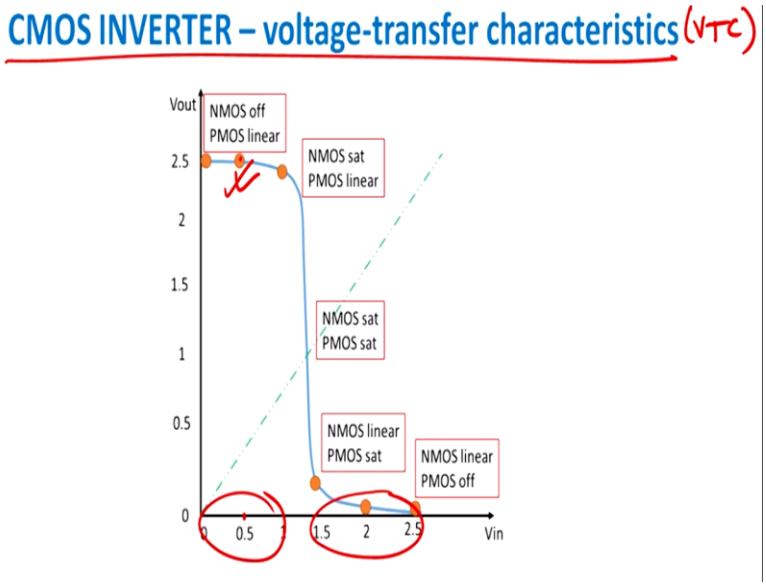

So if you see here for Vin = 0.5 I was getting a 2.5 explain also got the point why when the input is low output will be high when the output is high input will be low how I got this points i got these points from these this region so how do I get it? so related to 0.5 I just check out where I am doing it this is somewhere here is almost near to V out which is 2.5 volts when I go to higher voltage let us say Vin = say Vin = 2.5 or 1.5 let us say then say I go to 2.5.

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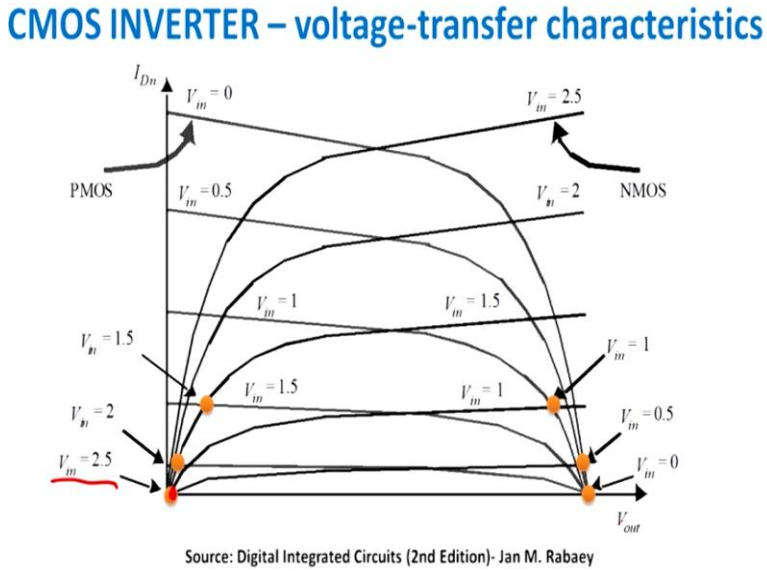

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When Vin = 2.5 the cutting takes place very near to 0 axis 0 of Vout so therefore which this knowledge I can safely assume that this curve which you see in front of you is primarily the defined as the CMOS voltage transfer characteristics VTC right which means that when the input is low output is high when the input is high output is low fine with this knowledge or with this idea let me stop here for this time we will continue after this with in this thing thank you.