CMOS Digital VLSI Design
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Module No # 01
Lecture No # 04
MOS Parasitics and SPICE Model

Hello everybody again welcome to the fourth lecture in the series of the NPTEL online certification course. The topic of this lecture heading of the lecture basically MOS Parasitics and SPICE models.

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Outline

- MOS Structure Capacitance
  - MOS Overlap Capacitance
  - Channel Capacitance
  - Junction Capacitance
- Source-Drain Resistance
- SPICE Model for MOS
- Equivalent Structure of SPICE Models
- Model Equations of LEVEL-1, LEVEL-2 and LEVEL-3
- Recapitulation

What will be covering in the next half hour or so is basically the various capacitances of the MOS structure. So we will be looking in the MOS structure how it works in MOS devices we have already seen that we have also seen two important parameters that how can a MOS devices under short channel effects behaves and under long channel effects behaves we have seen how can a MOS can used as a switch.

A very important property of any digital VLSI design or chip is to find out the total delay of the signal moving from primary input to primary output of the logic which means that one of the important properties of parameter or properties of digital VLSI chip or for digital chip is to find

out delay. Why delay is the important? Because ultimately you should know that what maximum frequency the chip can perform. So one upon delay of that will give the maximum frequency.

Therefore to understand the delay two very important properties of the devices are resistances and capacitances as you are very well aware of this fact possibly. Why capacitances because see if there are larger capacitances you require larger amount of time to charge and discharge the capacitances. And similarly if the resistances is high your on current will be low and therefore you require a larger amount of time to charge and discharge the capacitor.

In both the cases your delay will be large and therefore it is quite essential and very important that we study, what is the capacitance model of a MOS structure therefore given a MOS structure. I will be designing its capacitances how it capacitances looks like. Out to which what are the important properties? The first property is MOS over there are parts of capacitor and one of them basically the overlap capacitances we will look at the channel capacitances we will look at junction capacitances.

We will be also looking at so this will take care of capacitance modeling of a devices similarly we also need to know the source to drain resistances that means the resistances offered by the devices between source to drain. But, the very important property or characteristics is all this two things R and C are all biased dependent which means that its value will go on changing as you apply various biases across the network right.

Unlike other properties structural properties for example that do not change with bias but resistances and capacitances will change with respect to bias because of simple reason that the amount of voltage which you give will determine that how much amount of current will be flowing through the. We look into the source to drain resistance then we go to SPICE model why spice model?

Because we will be giving you assignments during the assignment phase we will giving you assignment on spice. So I would recommend that this stage please download the open source available or spice package from the net you can actually download may be P spice which is personal spice if you have T spice it all the all the more better which is tanner SPICE you can also have any other EDA tool which manipulates or which replicates or mimic spice. So you

should have this module available one of the standard tools for circuit simulation for this will all are for circuit simulation and very important tool and very widely used to across industry as well as in the academia.

And then we will look into what are the spice models available to us there are various models equations for level-1, level-2 and level-3 of spice. What are these levels? And what are the governing equations available with that and we will recapitulating our whole lecture plan.

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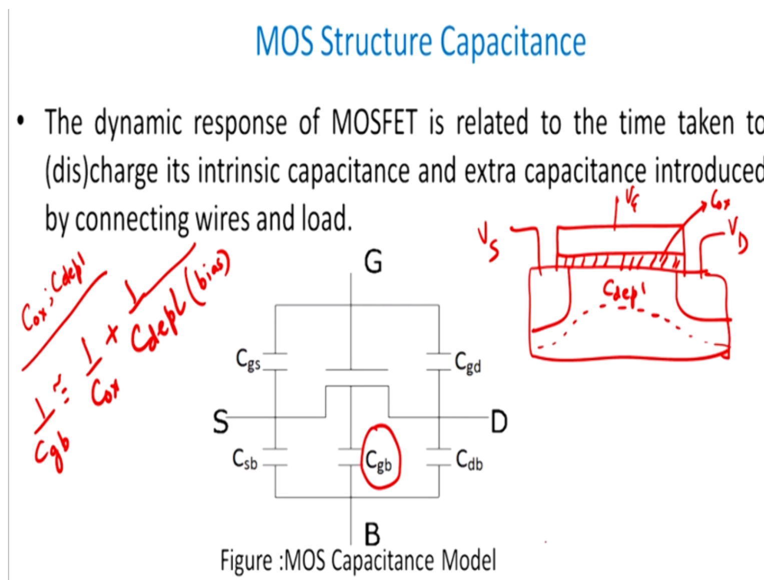

Let us look at the MOSFET again I will like you to maybe I can here draw here itself the same figure I have been drawing it for the last few lectures and something like this right this is what the structure which is seen in front you and we have been learning it for quite a long time but this time it must be you must be aware of all this structure available here so adding source drain and gate right.

Now you see therefore this gate is actually having an oxide layer here right and as I discuss with you the previous term that this oxide will be given by oxide capacitances Cox they will be also a C depletion which will be available and this Cox and C depletion will be in series to each other this we have also discussed. So that together is basically my Cgb, Cgb primarily means gate to bulk so I get 1 upon Cgb is almost equal to 1 / Cox + 1 / C depletion right.

$$\frac{1}{Cgb} = \frac{1}{Cox} + \frac{1}{Cdep}$$

As I discuss with you earlier therefore those Cox is fixed constant depending upon the value of Tox and the value of a permittivity of the material which you have to taken as dielectric. This C depletion is basically bias dependent quantity and therefore this will go on varying as you change the bias and therefore Cgb is obviously the strong function of the bias. This is Cgb right now let me come to other items here.

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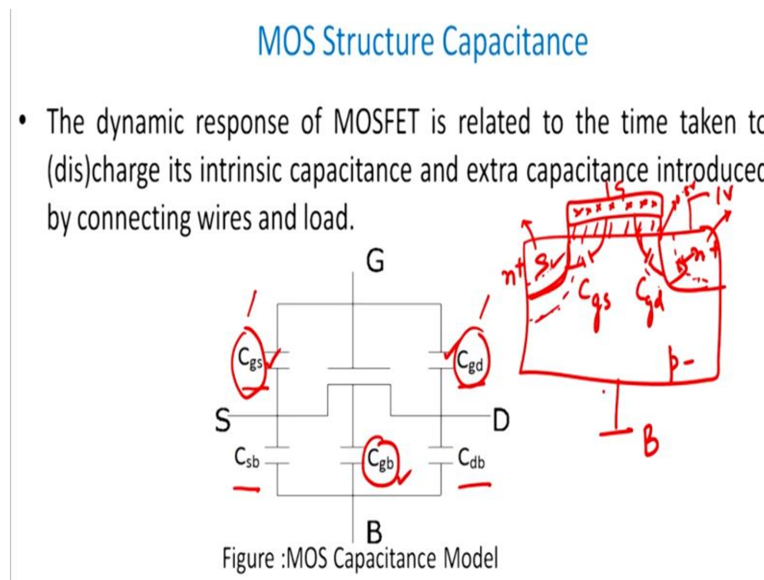

This is done we have to done with this one right we now come to Cgd and Cgs again if we look at the figure here Cgd and Cgs. Even if you draw here like this source and drain and you have gate here see this is highly this is basically a metal so you will have large electrons here you will also have large electrons here by virtue of doping because you have done a doping which is of very high concentration at this side and this side once you have done that and it is separated by dielectric here

Therefore this Cgs gate to source is basically the capacitance form by virtue of large amount of charge carrier at the source end and at the gate end and this is basically your Cgs same thing same logic can be applied to Cgd so this is Cgd write so I got Cgs I have got Cgd. So these are two capacitances which are there why because they are primarily they are because you have a

large consideration gradient between the two or there is a large concentration of charge carrier separated by dielectric in between the two right.

Now if you reduce the doping concentration of this region or this region you actually lower the charge and therefore lower the capacitances right. But the cost to pay for it is that now since your n+ will have a lower charge. You will have lower current not only that the depletion thickness will depletion thickness which was available earlier more on this side will now extend more towards source side as well.

So there will be large drop in the depletion region the voltage which you apply on the drain side there will be a large drop across the depletion region. So if you apply so let us say you apply 1 volt here actual voltage visible here will be may be just 0.8 volts may be I hope I am able to explain to you what I am trying to say by changing now the doping concentrations I can actually change the value of Cgs and Cgd right and that is quite important.

So with this we have finished with this and this let us come to the last two which is Csb and Cdb. Csb is source to bulk and Cdb is drain to bulk as you can as i discussed with you this bulk which you see in front of you. This is a p type substrate and therefore there will be always a depletion region here as well as here.

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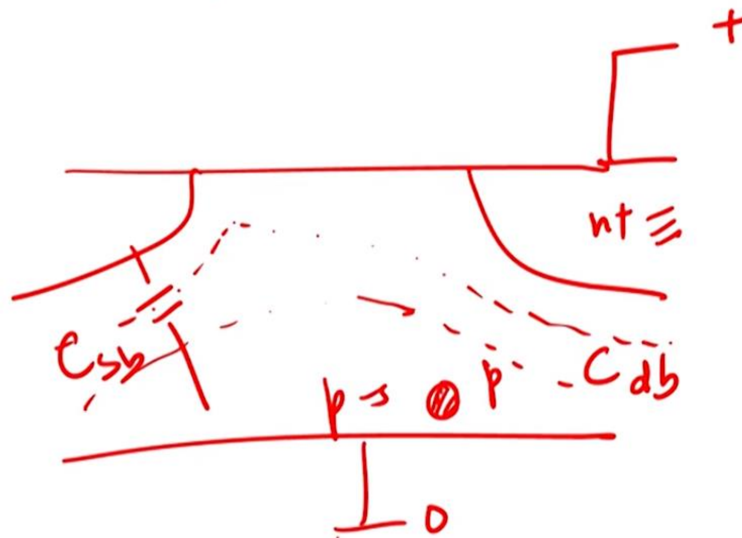

So if we can see here if i have a substrate here and if I apply bias here then there will be a depletion region here there will be a depletion region here. This depletion region is what this is

pn+ right. So there will be depletion region here this is positively bias suppose this n type MOSFET. I make it 0 let us suppose no effect. But still there will be depletion region here.

Make it more negative this depletion region become larger and larger this side and this side right so you get the point therefore I will be able to do large amount of variation. Therefore, this so this is basically a large amount of there will be a large amount holes available here. There will be a large amount of electrons available here separated by dielectric here depletion region not conventionally dielectric devoid of any free charge carriers therefore, this will act as Cdb similarly this will act as Csb.

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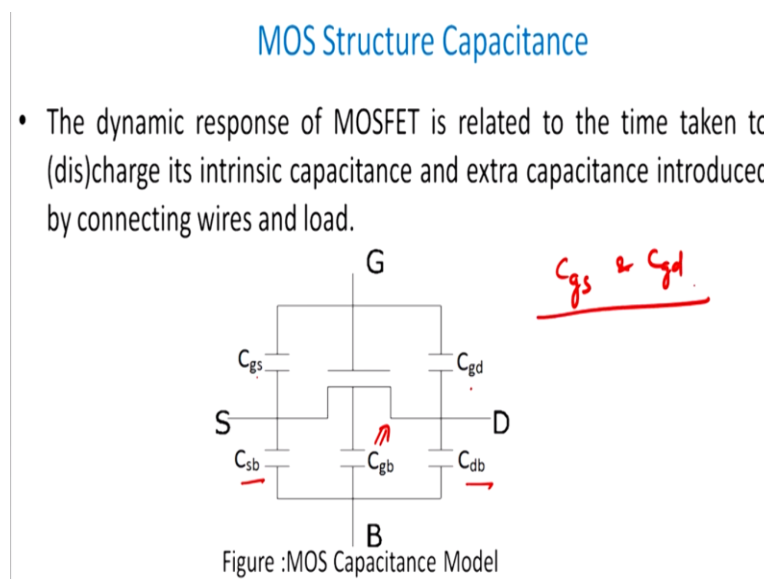

So what I get from here is therefore, that finally you will have what? you will have Csb and Cdb. And this therefore Cgb is composed of Cox and C depletion Cgs and Cgd are by virtue of charge carrier and the capacitance between area is gate and drain, and gate and source and Csb and Cdb are between source and bulk and drain and bulk. With this knowledge let us discuss each one of them individually now. This Cgs and Cgd can be again broken down into two major components.

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MOS Overlap Capacitance

- Ideally, the source and drain diffusion takes place right at the edge of gate oxide, but practically it diffuses below the gate oxide with lateral diffusion of x_d.

$$C_{gs0} = C_{gd0} = C_{ox} x_d W$$

where $C_{ox} = \varepsilon_{ox}/t_{ox}$ is a capacitance formed due to gate oxide.

Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

The first one is basically CMOS overlap capacitance please remember in my first slide where I was discussing MOSFET. I discuss with you there will be a lateral diffusion of a charge carrier from source and drain. So, this is a lateral diffusion taking place in this direction fine is the lateral diffusion happening along this direction. When there is a lateral diffusion taking place here the effective L actually reduces again discuss with you but not only that you see very important part that now you have some part of the gate which tends to overlap with the drain and the source which is which part this part and this part right.

Now what is happening unlike in the previous case now you have direct overlap between the two charges separated by dielectric? This is defined as my overlap capacitances right so, what I am trying to say is if this is poly silicon gate which you see. This is my source and drain and this is the overlap which is happened right this overlap. So this picture is nothing but the cut picture along Y direction so this is the cut here I am taking photograph from the top. This suppose this is Xd which is the Xd is basically my overlap distances right and Xd.

And Ld is the effective length which you in front of you right then we define Cgso and Cdo; O basically means overlap here. So Cgso assuming that this Xd same on both direction how? Because this doping and this doping is again same source doping and drain doping is exactly the same then we assume that this Xd on the source side say Xds is exactly equals to Xdd which is the Xds is the source doping on the source side is exactly equals to the source doping on the source side. Assuming what?

Assuming that the doping concentrations is same and the source and the drain side is same. If you assume is true there i get Cgso = Cdo = Cox oxide layer per capacitance into Xd into W. W is the width, width is in which direction? This is the width right and Xd is this dimension so basically this is the area right and this was oxide capacitance per unit area. So you get what you get from here is basically the total cap.

So Cgso and Co is basically my oxide capacitance sorry overlap capacitance total overlap capacitances. Cox is the oxide capacitance per unit area Xd into W is nothing but area so area gets cancelled out and I get the total capacitance available to me by virtue of the depletion capacitances or overlap capacitances. Now after we have understood what are the various criteria of a overlap so in most technologies today you do have overlap.

So C overlap is one of the primary reason you do have Cgs and Cgd right the second is which is the channel capacitance this is what was discussing with you this Cg channel capacitance with Cgb gate to bulk across the channel.

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Channel Capacitance

- The most significant parasitic MOS components are channel capacitance, which consists of C_{gcs} (gate-source), C_{gcd} (gate-drain) and C_{gcb} (gate-body).
- These capacitances are dependent on region of operation and applied terminal voltages.

G G G
C_{GC} C_{GC} C_{GC}
S D S D S D
Cut-off region Resistive region Saturation region

Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

Let me come to that and explain to you till now we were looking into the most significant part of the MOS component are channel capacitance which consist of channel capacitance of source side so you will have between gate and you will have between source right as I discuss with you between gate and drain and between gate and the bulk to the body.

So there will be three components here gate source, gate drain gate and the bulk and gate in the body. So I define Cgs as the gate to source capacitance Cgcd is gate to drain and you get Cgb gate to bulk right. Now let us see how it is works out let us suppose I have a devices which is something like this. So now I am now understand I am using MOS as two terminal devices alright.

What are the two terminals? Sources grounded gate I am giving one potential and drain I am giving another potential. So it is just two terminal one is gate and drain is also let us suppose grounded does not matter at this stage. Now what will happen is when you have cut off mode.

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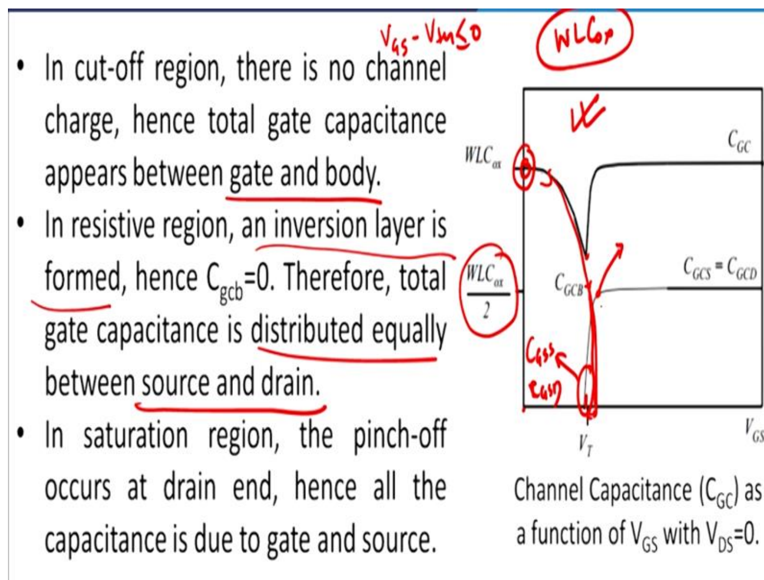

So let me come to next case in the cut off mode when Vg is less than Vth right is less than 0 there will be no channel fromed as I will discuss with you. Hence the total gate capacitance appears between gate and body so it will be fully between gate and body so out of the three here gate source, gate drain and gate body all the capacitor will be govern by gate and body.

There will be no contribution of gate and source and gate and drain why because there is no charge which will be contribute. So because it is all fully depleted there is no free charge carrier available here. So everything is pushed back to the depletion layer here there is no contribution for source and drain side further the drain and source side have been actually made to ground state.

Now in the resistive region when your gate voltage is above the threshold at that point of time an inversion layer is formed as in inversion layer is formed. There will always a there will so in inversion layer form is form and therefore your block contribution goes to zero why? Because know you have layer of electron which screens the potential or which screens the charge and therefore the bulk will not be able to add to the over all potential and therefore you see Cgcb which is basically your bulk potential goes to 0.

Which means that if you look this graph here this was initialize when your gate voltage is 0 cut off when it was cut off the whole potential as discussed with you appears between gate and body therefore the total gate potential was how much WLCox. So why it was basically like this because C depletion was infinitely basically infinitely large as a result you will have only WL Cox 0 there will be no depletion capacitance and therefore the overall charge will be 0.

As you reach to a threshold voltage somewhere here since it is screening phenomena. The gate component will go to 0 so is this what is happening its goes to 0 just at the threshold marking this suddenly falls to 0. Now what happen as it is falls to 0 the capacitances is taken carry by the source and drain right and therefore the total gate capacitance is assuming that there is no potential applied is equally distributed between source and drain right.

And therefore they become equal so what can I do WL Cox by 2 so I initially WL ox and now I get WL ox by 2 at what time at Vt just less than Vt I get WLCox / 2. So it is initially 0 there was no contribution of Cg there was no contribution there is no contribution of Cgcs or Cgcd here but exactly at this point there is a contribution exactly at the threshold voltage there is a point there is a contribution.

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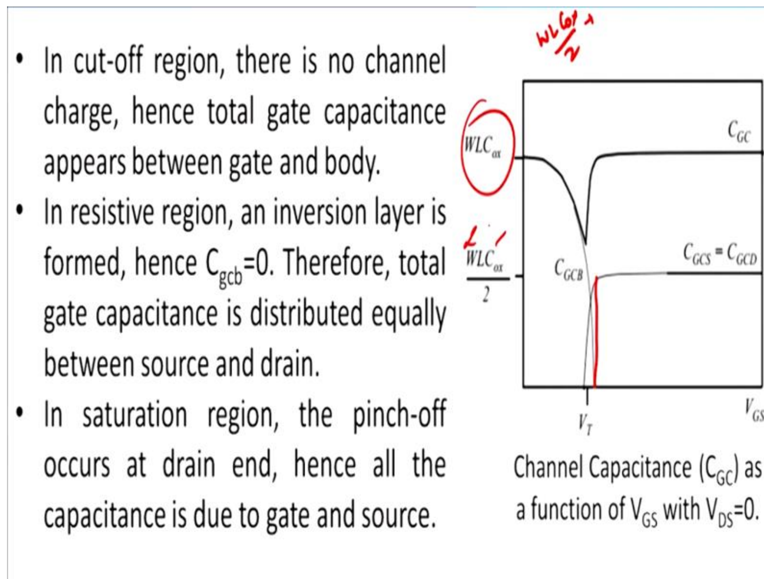

So what you see is exactly at this stage right where this goes to 0 everything is taking care of by at least half of the gate to source gate to channel sorry source and gate to channel by drain side. Since individual of them is WL Cox / 2 if you simply add to them together I can get total WL Cox because there they are in parallel actually. So if there are parallel C1 + C2 I get total WL Cox and assume of therefore increase Vg the total capacitor still remains the same which is WL Cox. But how it get distributed in channel between the source and drain is a big question and it is still being watch into.

But at this stage at least for the VLSI design course which we will be doing it we will assume that there will be no contribution from the body once the gate voltage crosses threshold voltage and is only contribution is through source and drain and we will also assume for the time being that there equally taken care of by source and drain which is WL Cox / 2. WL is the area Cox is the oxide capacitance of per unit area and by 2 right. So this is what we will be discussing or we will be assuming in to be true.

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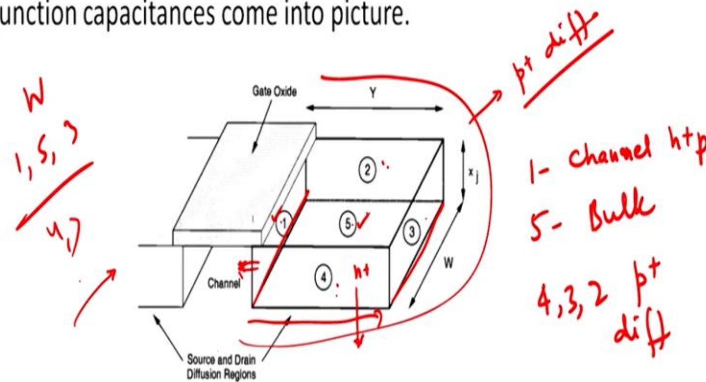

Now we come to the third part of the capacitance model and that is known as the junction capacitance. Junction capacitance if you look at the again channel here this is basically my line diagram of the figure then this is the channel. This is basically your n+ region right so there are five surfaces available here 1, 2, 3, 4 and 5. 1 is basically towards the channel so this is toward the channel. If we look very closely 5 is actually towards the bulk right 4 is across the layer so generally what happen is that to make two devices isolated from each other. We give the diffusion well around the devices so what we do is this is n type we give a P well around the devices.

So there will be a P well sort of p+ diffusion layer or a diffusion layer available here. So I will have surrounded P type here so that the two devices do not get shorted with respect each other. So what you will see is you will have 1 junction 1 to channel so 1 to channel they will be with 1 junction which is basically n+p channel which is n+p. We will also that 5 with bulk why 5 because 5 is attached to bulk 4, 3 and 2 are attached to this p+ diffusion layer.

So there are 5 junction capacitances available to you at this stage and they are all area dependent so for example if you make a W large who will get affected 5 will get affected right because W into L W into this distance is basically 5. If you increase W is also influence 1 so 1 will get affected 5 will get affected right but prima facie it looks like 4 and 2 will not get affected 3 will affected. So if you change W 1, 5 and 3 will get affected.

If you change L as the name suggest I will get 4 and 3 get affected. So if you change the W/ L ratio aspect ratio. This junction capacitance becomes the sensitive function of these values or voltages right and this becomes bit complicated as far as this deriving this capacitances is concerned. Why we are doing it? At the end of the day I want the total capacitance available in a device for finding out the delay and therefore the maximum frequency of operation.

That is what I was asking that there will be therefore a large number of PN junctions which will contribute into the total junction capacitance available to us. So there will be a how many PN junction and there will be actually if you look very carefully there will be a 5 PN junction available right and the 5 PN junction will be all in parallel and therefore we need to add them up to get the total capacitances available to us. However there are strong function of applied voltages and parameters right if you look here further get the picture correct.

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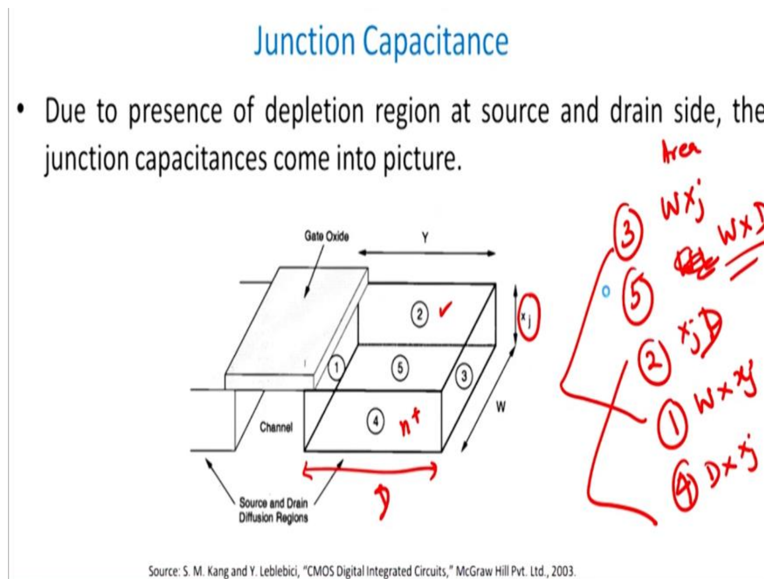

Yes if you look here this is defined as the Xj. Xj is the diffusion length or basically the thickness of the n+ drain layer right and W is the width of the area so the number 3 as got an area W into Xj whereas number 5 as an area this is an area which is W into L similarly 2 as an area Xj into L right or Xj sorry is not L. W into L but it is basically W into this dimension. Let us suppose we call it as whatever we call as say may be drain D let me call it D W into D right we will have number 2 which is this one will have Xj into what into D so what will be 1?

1 will be basically W into Xj right and number 4 will be what? Number 4 will be D to Xj so these two will be behaving in the same manner and this two will be behaving in the same manner and this will be behaving in the opposite manner. So these thing will be clear to as far as notational symbols are concerned right and we will be able to formulate the policy. Now what happen is PN junction diode theory is well known to you from a basic days what we do is just convert this into ordinary reversed bias or forward bias or PN junction diodes. And the capacitance derive thereof can be directly fed into the junction capacitance of this one.

And if you look therefore it is given by this formula which you see in front of you this is generalized formula sorry this is the exact formula which were using it were phi 0 is basically built in potential and V is the applied bias. What is built in potential? See built in potential primarily means that if you look back in this slide and if you look clearly at this point.

$$Cj(v) = A\sqrt{\frac{\varepsilon q}{2}\left(\frac{NaNd}{Na+Nd}\right)}\frac{1}{\sqrt{\phi_0 - V}}$$

This is basically n+ and p right even if we do not apply any bias there will be a small depletion region which will be available here right. The built in potential is defined as the amount of potential required to cross this depletion barrier fine. So the amount of voltage required so phi built in is basically the built in is basically the amount of voltage amount of applied voltage to cross the depletion region right.

So this is known as phi built in or phi built in is basically the amount of voltage is required to do that which means the amount of voltage to cross the barrier. Why is it like that so that will explain in this slide see when you applied a bias. The built in voltage in the applied voltage will be in the opposite side and therefore the negative sign available here. If you look very closely to this equation this negative sign is primarily because of the fact that when you have built in voltage and when if you apply a voltage which is reverse the built in voltage there will be a negative sign available to you.

So when you do reverse bias sort of mechanisms this voltage goes on increasing in the negative sense, as a result the subtraction of this minus this goes on decreasing and therefore Cj increases and there is true also in this depletion becomes larger and larger the junction capacitance starts to rise up.

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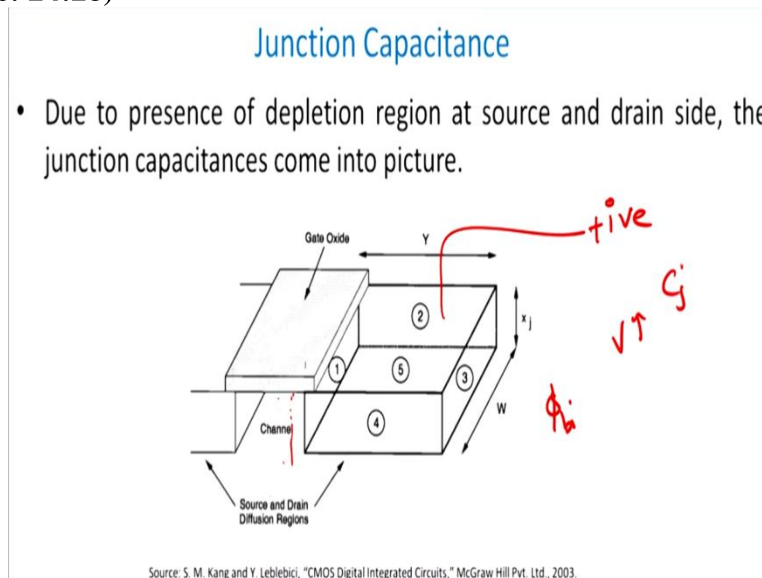

Which means that therefore coming back to the previous slide if you therefore have positive voltage applied here as the drain voltage and it go on increasing the drain bias more and more this depletion thickness become more and more and therefore phi built in becomes more and more right and not only the phi built in we are also increases become more and more and therefore the capacitors actually becomes larger because you are actually increasing the area.

We also this is generalized formula this is the Cj0 is the junction capacitances.

$$Cj(v) = \frac{AC_{j0}}{\left(1 - \frac{V}{\phi_0}\right)^m}$$

When you do not have any applied bias when you applied bias is 0 and is given by the formula. So as you can see here as this bias is increases here this quantity become larger and larger 1 - this quantity goes to the smaller and smaller and therefore Cj goes to the increasing. So when V increase right when V increase the denominator term that is the denominator term will go on actually decreasing and therefore Cj will go on increasing right and A is the area of the cross section between the two right.

This is quite interesting phenomena which occurs here once you have understood the capacitance part and we have been able to find out what the capacitance is looks like all our capacitance which works out. We so end of the day all the most capacitances made up of 5 capacitance gate

to bulk, gate to source, gate to drain, source to bulk and drain to bulk right and there will remains almost bias dependent and also structural dependent.

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Source-Drain Resistance

- Another parasitic component which affects the performance is the resistance in series with source and drain.
- This effect is more pronounced in smaller feature size.

$$R_{S,D} = \frac{L_{S,D}}{W} R_{sheet} + R_C$$

G

R_S R_D

S D

where R_{sheet} and R_C is the sheet and contact resistance respectively.

We also look into source to drain resistance, what we say is that the source to drain resistance will be depending upon the contact between resistance Rc is the contact resistance here and it will depend upon the resistance offered by the device itself. So you please see a MOSFET if you look very carefully as I discussed with you if you look at a MOSFET structure and understanding it properly.

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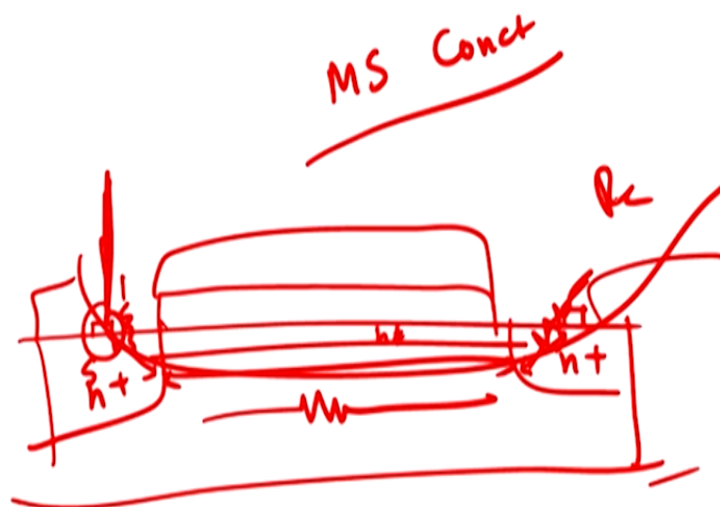

We will see that when the devices is ON state this n+ you have thin region here which is n+ and we will have n here may be n here not n + and we will have source drain and so on and so forth and this is with you right. If you look here the resistance offered by this channel is one part the resistance offered by this region and this region is another because the current will be flowing in this manner.

So conversion of current will be flowing in the opposite direction and there will be also a resistance offered by the contact between the metal and the semiconductor this is the metal layer which takes the current from the MOSFET and this is the semi-conductor. So this will be a metal semi-conductor contact right and therefore there will be a potential drop here and therefore the resistive element here.

So there will be a one resistive element corresponding to this and there will be a another element corresponding to this so this will be the channel resistances and this will be the contact resistance this will be Rc right. So this was what I meant to Rc is the contact resistance Lsd is the source drain region divided by L into R sheet happens to be value and this is how you calculate the value of Rsd source drain resistance right.

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SPICE Model for MOS

- SPICE is a general purpose circuit simulator.
- SPICE has three built-in MOSFET models-

1. Level-1 (MOS1)-described by square law of I-V characteristics.
2. Level-2 (MOS2)-detailed analytical MOSEFT model
3. Level-3 (MOS3)-a semi-empirical model.

- Second order effects such as SCEs are included in MOS2 and MOS3 models.
- MOS models can be included by .MODEL statement in a particular simulation.

So this is the typical value which you calculate for all practical purposes resistances. Now, when you understood R and C individually without going into details because at least for digital VLSI design at this stage you do not required too much knowledge about all the resistance all the capacitors from many detail point of you whatever is been told to be is enough to calculate the

values of resistance and capacitors for typically circuits which you will be handling in this course right.

Now an important an idea or important discussion is primarily on spice right a spice is a basically a model a spice is a model which is basically used by large number of circuit. So spice is basically circuit simulator so this spice is basically a circuit simulator I will recommend that you please download this from the website it is open source available to us and you can actually simulate small circuits in that is almost like a ORCAD tool for circuit simulator and you can use this for MOS devices in the MOSFETs only there large number of model facts available and they are pretty accurate and easily done for at least 15 to 20 number of active devices per schematic.

And it is a very general propose circuit simulator so you do have it is more of plug and play so you have resistors you have MOSFETs you have capacitors you have large number of battery source types of profile and everything you do it. Spice allows you to do three types of simulation one is known as DC right and AC and third is basically a transient. So all these three they allow to do DC means you apply a fixed bias right you apply a fixed DC source and you try to find out the current and voltage at any appropriate node in the circuit.

What is AC exactly what to find the current and voltage at any appropriate node in the circuit but then the current source and the voltage source is basically AC in nature so I will have A sign omega T sort of available of omega T or whatever maybe AC wave in general. What is transient? Transient is again you are not giving a DC or AC but you are giving a pulse that so let us say you give a small pulse here or you give a small pulse here then with this pulse how does the circuit behave that is known as transient analysis.

So this is very small time to analysis domain analysis this is a large time domain analysis and this almost equal to 0 DC as you can understand is basically a non-time zero analysis.

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MOS device spice model as we know of it is as got level three models but the level 1, level 2 and level-3 right. Level 3 is a semi-empirical models. Semi-empirical primarily means that out of large amount of experimentation using fitting parameter concepts I have been able to have the IV characteristics of the MOS device in level 3.

Level 2 is a detailed analytical MOSFET model so detailed analytical MOSFET model which is available to us by taking second order affects also into consideration. Level 1 primarily refers to square law so whatever we have been teaching till know whatever I have been delivering to you across this lecture all are all basically square law models of IV characteristics and level 1 uses that model for all practical purposes.

All second order effects are including in MOS 2 and MOS 3 which means all second order affects are included here. SCE and SCE but there is no and this is no SCE level 1 is does not any a model here. How you do it you insert dot model statement you insert when you do a simulation. So when we give you to assignment I will tell you how to do it but you do a dot model statement in order to do a particular simulation right. What is the let us the equivalent structure which SPICE uses its pretty interesting and since now you understood the various capacitors and resistive model It will be becoming very easier for you to understand.

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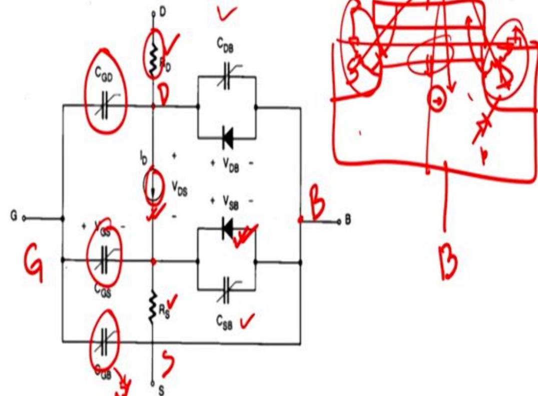

Lets looks at the structure here and let us suppose source drain as I discussing with you right i have a bulk here right i have a bulk here. Now lets us look at RD. RD is what? The resistance offered by the drain end this RD will consist of contract resistances here plus the resistance offered at this point right you will have a RS which is basically resistances between these two points as well as contact resistance this is S this is D agreed.

Now when the device is operating as a current source you will have this being replicated as a current source. So this the that current source which you see so I have RS, RD, RD i have a ID. Which is basically have a MOSFET of current source let looks us look at CGD this is gate to drain this is gate, gate to drain remember we just now discussed with the overlap capacitance junction capacitance and this is variable why? Because is a biased dependent you have CGS. CGS which is this one gate to source.

So gate given positive this is my source end this is my source and this is my drain end right. I also have fourth terminal which is basically my bulk right so this is my bulk which you see in in front of you this is drain, this is gate and this is bulk and this is source. So gate to bulk is basically my this gate to bulk this one so I will have to gate to bulk why? because directly body so this is basically my body capacitance right.

So I have three capacitors CGD, CGD, CGS and CGB right I have got two resistances RS, RD I have a current source here. Let us look at this and this if you look as i discussed with you this is

basically a P you will have a diode which is something like this right this is VSB right and this is the source so you will have two diode one will be towards drain end.

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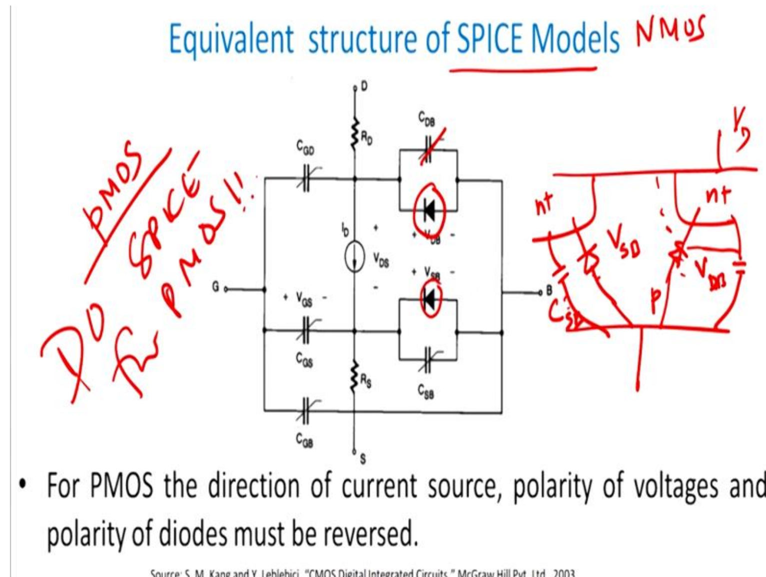

So just to remind you just to remind just to concentrate on lower side I will have P type semi-conductor n+ right I will apply a drain voltage VD. So if I have a P type here and N type I will have something like this which is nothing but VSB on source to bulk so this basically your CDB this is VDB this is DB drain to bulk right drain to bulk as a diode why? because this is a reverse bias junction diode there will be also capacitance which is CDB. CDB is what? Between drain to bulk so there will be a capacitance also between this is again the voltage variable capacitor which you see already discussed in the previous slide.

This will be again therefore this is n+p so you will have a something like this right this will be value be C as this will be V source to bulk right and there will be capacitance which will be C source to bulk right again a variable capacitance. So this is the overall and there will be parallel to each other so you see these two are in parallel to each other is to parallel to each other and therefore this is the equivalent structure of the spice model. For PMOS all the polarities and current source direction to be reversed I leave as an exercise to you to please do the spice model for NMOS please do spice model for do spice model for PMOS as well so please do it for PMOS.

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LEVEL-1 SPICE Model Equations

- In linear region- $I_D = \frac{k'}{2}\frac{W}{L_{eff}}[2(V_{GS}-V_T)V_{DS}-V_{DS}^2](1+\lambda V_{DS})$
- In Saturation region- $I_D = \frac{k'}{2}\frac{W}{L_{eff}}(V_{GS}-V_T)^2(1+\lambda V_{DS})$

  To maintain the continuity at the linear-saturation region boundary, $(1+\lambda V_{DS})$ term is included in both the equation.
- Five electrical parameters i.e. k', V_T, λ, V_{TH} and Φ completely characterizes this model.

So we will be we are almost concluding the lecture now and giving you the various progress of spice model equation which we use. As I discussed with you for level 1 we have already taken into consideration Id is will be given by K prime by K prime is nothing Miu L K prime is nothing but Miu L C oxide / 2 into W / L effect into 2 into VGS-VT into VDS – VDS square 1+ Lambda VDS this is again in CLM.

$$I_D = \frac{k'}{2}\frac{W}{L_{eff}}\left[2(V_{GS}-V_T)V_{DS}-V_{DS}^2\right](1+\lambda V_{DS})$$

$$I_D = \frac{k'}{2}\frac{W}{L_{eff}}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

In saturation region as I discussed with you it will not be strong function of VGS but if you VDS but if you CLM into consideration it will be function of VDS its take this into consideration of all practical purposes again I take (1+ Lambda VDS) as continuity equation continuity term between these two points when VDS = VGS-VTH at a starting of the on set. As I discussed with you the five electrical parameters which you see in front of you are all basically process dependent parameter and they can be easily found out by the you understand the doping and the structural parameter of the device .

We can do spice level 2 model equations and this spice level 2 model equation are more accurate as compared to level 1 and I will not go into detail of how they are form.

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LEVEL-2 SPICE Model Equations

- To obtain more accurate current equation the voltage dependent bulk charge must be taken into account.

$$I_D = \frac{k'}{(1-\lambda V_{DS})}\frac{W}{L_{eff}}\left\{\left(V_{GS}-V_{FB}-|2\Phi_F|-\frac{V_{DS}}{2}\right)V_{DS}-\frac{2}{3}\gamma\left[\left(V_{DS}-V_{BS}+|2\Phi_F|\right)^{3/2}-\left(-V_{BS}+|2\Phi_F|\right)^{3/2}\right]\right\}$$

- The saturation voltage is given by-

$$V_{DSAT}=V_{GS}-V_{FB}-|2\Phi_F|+\gamma^2\left[1-\sqrt{1+\frac{2}{\gamma^2}(V_{GS}-V_{FB})}\right]$$

- The saturation current is given by- $I_D = I_{DSAT}\left(1/(1-\lambda V_{DS})\right)$

But this is the equation which you see in front of you for the drain current in the linear region and this is my saturation region right and this saturation region which you get this is the VDsat for saturation region. So please understand here rather than speaking as this is basically your velocity saturated drain to source voltage.

So that that the reason I have written to be as Vdsat right and it depends upon the value of VGS - VFB. VFB define as the flat band voltage difference between the metal and semi-conductor as you can see from all this discussion as you increase the values of VGS prima facie you VDsat also start to increase which we already seen in our previous discussion even level 1 MOS devices if you increase the VGS make over drive larger you end up having a threshold larger so this thing threshold available to you larger pinch of point voltage available to you.

We come to the last spice model which will be discuss there are actually large number of levels but I will be concentrating only on till level 3 it is bit complicated because it is more of semi empirical what we do is you do a large amount of data analysis and do the large amount of experimentation then do the curve fitting and then you take the coefficient of the line of best fit and that will be your MOSFET level 3 model.

So we do the large amount of manipulation here in order achieve the best results. The idea is to achieve or to get a the value of IDVD at a much faster phase. So if we have to do the backup the

envelope calculation without going to details of it level 1 to level 3 is sufficient to take care of all your requirements. But If you what to be more accurate taking other effects in the consideration you need to go at higher level. The price is pay for it off course computational complexity at the time taken for the algorithm to converge.

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LEVEL-3 SPICE Model Equations

- This level precisely includes the short channel effects. The majority of the equation of Level-3 are empirical.
- The current equation in linear region is expanded using Taylor series-

$$I_D = \mu_s C_{ox} \frac{W}{L_{eff}} \left(V_{GS} - V_T - \frac{1+F_B}{2} V_{DS} \right) V_{DS}$$

where $\left[F_B = \frac{\gamma F_S}{4\sqrt{|2\Phi_F| + V_{SB}}} + F_n \right]$ shows the dependence of bulk charge on the geometry and F_n includes the narrow channel effects.

Bulk - V_{th}

So what you see from here is that in this case specially in level 3 you also take the bulk charge which you means that the how does your bulk influence your the threshold voltage. So which is not available in the level 1 and 2 are the larger extent in level 2 is available in level 3 and therefore if you change VSB drastically you actually see a change threshold voltage in level 3.So if you want to use bulk substrate effects which is body effects try to go for level 3 spice model.

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Recapitulation

- The dynamic behaviour of MOSFET can be analyzed by the knowledge of its capacitance.
- SPICE is a general purpose circuit simulator.
- Three levels of MOS models are basically used in SPICE for simulating the MOSFET structure.
- LEVEL-2 and Level-3 models have includes the second order effect in it.

So let me recapitulate what we did today what we did in lecture for this lecture. What we did was we try to analyze the dynamic behavior of MOSFET not the behavior at least but the parameters required to understand the dynamic behavior. Dynamic behavior means that you have applied voltage and then it is varying and I am trying to read how the capacitance is varying with respect to applied voltage so and hence so forth.

And therefore trying to predict resistances and capacitances based on that and therefore the total overall delay on the system. And therefore we have understood the various capacitances available there have the five capacitances which primarily can be broken down and each can be individually calculated and therefore the total capacitance can be found out. We also understood the resistance how resistances formed it is form by the channel resistance as well as the contact resistance source and drain.

We finally ended with spice general purpose simulator what is the spice though you require larger amount I will leave as exercise to you to please go through spice simulator it is corresponding manual and you come back to me. If you have any queries regarding that level 2 and level 3 are generally mend for second order effects and level 1 is mend for without any second order effects and they are straight forward pretty very simple early prediction of the current voltage characteristics with these words I would like to thank you for you patient hearing and we will continue with this topic in the next class thank you.