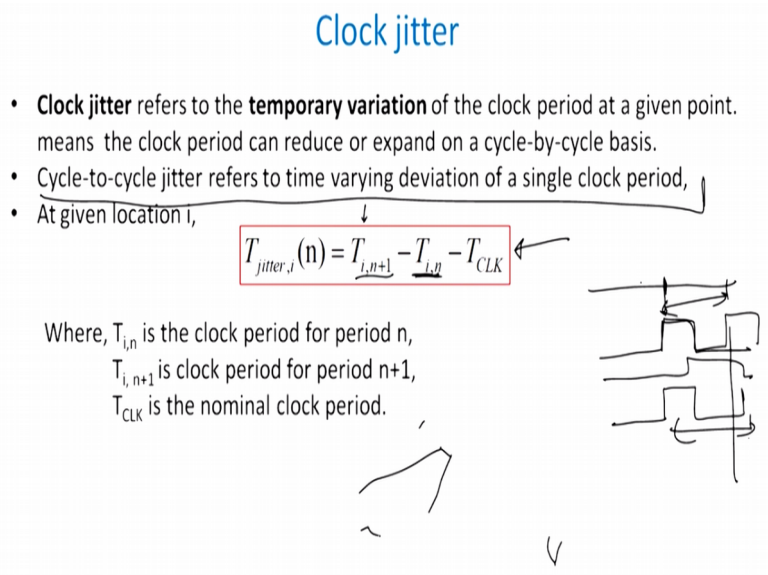
CMOS Digital VLSI Design
Prof. Sudeb Dasgupta
Department of Electronics and Communication Engineering
Indian Institute of Technology – Roorkee

Module No # 08
Lecture No # 36
Clocking Strategies For Sequential Design –IV

Hello everybody welcome to the online NPTEL certification course of CMOS digital VLSI design and we will start with the forth module of clocking strategies used for sequential logic design in the previous module we have looked into various issues related to clocks Q and what are the various issues for example what is the positive clocks skew what is the negative clocks skew and how does it adversely impact the functionality of a sequential logical block and how does it effect the set up time whole time and the frequency operation of the frequency logic.

In this module we will be concentrating on next problem area of clock and that is clock jitter so start with clock jitter let us see how it is works out. Now clock jitter is referred to the temporal variation of the clock period at given cycle of time which means that from each cycle to cycle within this same clock then time period might not remain fixed time period may vary. SO let us suppose at one point of time the time period was one in the next cycle it becomes 1.1. So there is increase in the time period it becomes 0.9 right so the temporal variation in time domain from cycle to cycle for each clock pulse is basically defined as clock jitter.

(Refer Slide Time: 01:47)

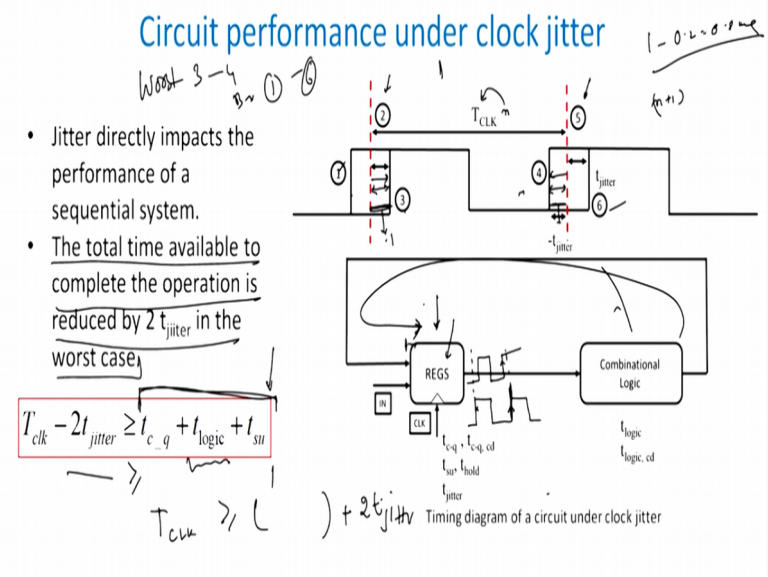


So as you can see therefore that the clock cycle to jitter refers to time varying deviation of a single clock period right. So let us suppose at a given location means let us suppose I have interconnect here at this point I am trying to measure the clock let us suppose at this point I have a clock pulse coming here right. So what I am doing is again at Ith location I am measuring it over a period of time and then what I see is the next clock pulse arrives it just shifted to the right or the to the left or what is happening is that even if it is like this right if this is like this the next clock pulse it starts here but then it ends somewhere here let us suppose the capital T which was initially this much as now becomes this much.

So this is the difference between capital T value here so that is what is basically known as jitter (()) (02:43) how do i define jitter capital T which was initially this much as now become this much so this is the difference between the capital T value here. So that is what is basically known as jitter so do I define jitter mathematically? Jitter is defined as a if you look in this red colored square clock the jitter had ith location for nth jitter for nth clock pulse I get the T I n + 1 basically means that for n+1th clock pulse.

If my variation is there because of capital T so the difference between that and the previous clock pulse which is the current clock pulse – t clock so that is basically the basic value of jitter you got the point that means it is the difference of the first so Ti n+1 is the clock period for the period n+1 at n+1th period you have a clock period of Ti n+1 at cock period n you have T1 – 1 if you subscribe these two the difference minus the T clock is basically my T Jitter which is here. So T jitter is basically the nominal T clock is basically nominal clock period right so the difference between the two is basically my clock jitter I defined to be as clock jitter.

(Refer Slide Time: 03:49)



Let us look at fact how does it vary so your nominal clock pulse if you look is basically edge 2 to edge 5 that is the nominal nominal clock pulse which you see but what has happened is that in the next clock pulse either it is shifted to 3 and to 4 or it is shifted to 1 to 6. So it was initially 2 to 5 but in the subsequent clock pulse at nth clock pulse you have but this as TCLK at n+1th clock pulse let us suppose we have 3n4 as the edges.

So what has happened in this dimension in this direction and it has shifted in this direction in this direction so this is shifted this side and it is shifted this side. So what has happened for every 1 clock pulse T my jitter is shifted to twice jitter so if this is my jitter which you see then this + this is the net difference in the value of capital T. So if a capital T was let us suppose once again and this is 0.1 milli second then 0.1 + 0.2 so 1 – 0.2 is happens to be 0.8 milli second to be the next clock pulse are known as the clock pulse available to you with jitter.

So that is what I am trying to say that therefore the total time available to complete the operation is reduced by two times jitter in worst case scenario that means worst case what? Why worst case? I am assuming that the rising age of the clock shifted to the right in temporary domain and also the second rising age is shifted to the left so both I was actually cramped down so your T is actually reduced you can have also a rising age shifted to left and the falling second rising edge shifted to the right then you will have the capital T in that you are safe because in that case the overall clock period actually increased the price we pay for it basically your lower frequency of operation.

But then functionality would not be disturbed but in this case when you have shifted the edge 3 to the right edge 4 to the left you end up having a large constraint on the functionality of sequential logic therefore you see this red color box which is in front of you this one if you look very carefully now the constraint here now therefore is T clock – two times T jitter must be greater than or equal to whole equation which we have already studied in our previous modules that you have T clock – two times T jitter should be at least greater than equals to a particular value right and that is already been fixed here by all practical purposes.

If you therefore shift T jitter on the right hand side I get this whole quantity T clock therefore should be greater than equal to whatever + 2 jitter. So unlike Q jitter is always a problem right because there is no minus sign there is always positive which means that it is adding to the time clock and therefore your overall timing will be larger in the case of a jitter as compared to SQ right.

And therefore it is always essential that jitter should be taken into account whenever you are doing a simple derivation. Now there is no if you see I have a register here you just see here and I have a H trigger clock here I have giving input here as a combinational logical block then you have a feedback path which again set back to the register. So obviously we are talking in terms of Q this will be negative Q this will be positive Q.

And therefore so if this a jitter in the clock itself then what will happen is that it will jitter in the clock then in during the first rising age of the clock it is sample the data it go through the combinational logical block with T logic as the total delay Tcq delay of the register is already available to it set up delay will be set up time violation will restrict the entry to the clock but when the next clock pulse arrives which is here your data should be ready at least one set up time before and then it will be able to sample the data.

And let us suppose let us jitter then what happened is at the same the same place at the Ith place only what has happened is this is shifted like this so what has happened is something like this let me show it to you what has happened therefore is that this which was rising edge which was suppose here and your second rising which is here let us suppose this rising edge is shifted to this

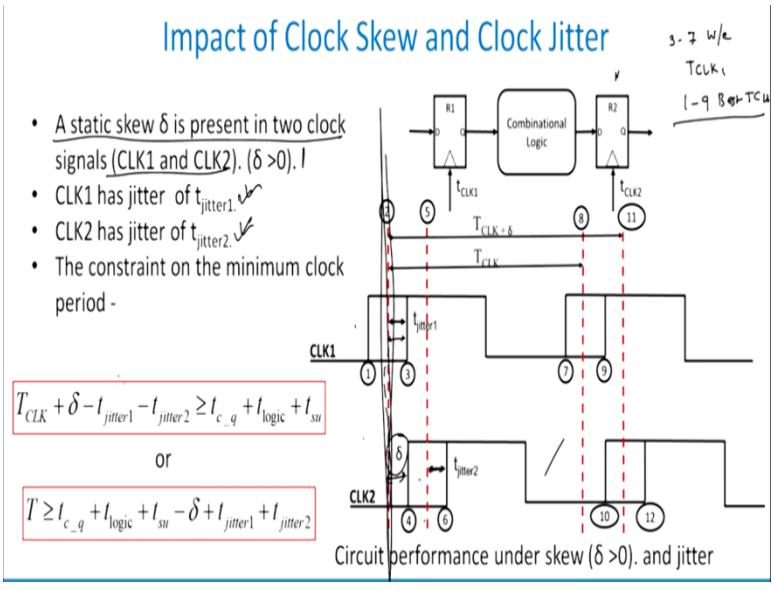
and the falling edge which is rising edge here actually shifted here right because of some problem.

As a result what has happened therefore is though you are able to sample the data in register and through the combinational logical block by the time it reaches here right it should have reached here by the time is actually is already passed off the rising age of the clock is already passed off and therefore you have to wait to the next rising edge to come into picture and therefore your functionality will be effected in such a scenario right.

And that is the problem area of a clock jitter ah clock jitter if you have even under the worst case the worst case is basically your is 3 to 4 edge and the best case is basically your 1 to 6 edge this is to (()) (09:02) right. If this is 1 to 6 edge you are actually adding to the total clock if it is 3 to 4 it is actually reducing the clock drastically low this is what is known as a clock jitter and the and therefore the constraint is given by this red color diagram which you see in front of you.

Now let us look at impact of both clock Q and clock jitter so please understand jitter in this case there is no negative this clocks Q which is negative. So let us look at the overall impact of the clocks Q and clock jitter right and that is quiet important and essential to understand.

(Refer Slide Time: 09:41)



Let us suppose that I have a I have a register R1 and I have a register R2 here and there is a combinational logical block here and between R1 an R2 you have a delta skew is there right. So

static skew delta is present in the two clocks clock 1 and clock 2 and delta is greater than 0 so I am assuming it to be positive clock positive jitter sorry positive skew right and clock 1 has a skew of T jitter 1 and clock has a t jitter 2.

So this is what t jitter 1 this is got t jitter 2 right so if you look at the diagram here and if you look at this is the nominal clock which you see is red colored is basically the nominal clock which you see. Then if you look at clock 1 since clock has got a 2 jitter 1 this has shifted to the right t jitter 1 approximately. So you actually wanted to evaluate at 1 at 2 you ended up evaluating at 3 right therefore if you go to the next rising edge you can add at 7.

So 3, 7 3 to 7 is the worst case sort of a t clock 1 and 1 to 9 is the best case t clock for t clock 1 best case jitter t capital T. Similarly if you look at clock if you look at clock 2 clock 2 if you look the you will see that clock 2 is to only this not only jitter had 3 jitter 2 but you also have a shifting of delta from nominal value. So initially this was the clock available to you this is the rising edge of the clock I would expect to see both the clock 1 and clock 2 are rising from same instant not happening.

So therefore there is skew which is positive in nature which helps me to shift this in this direction on the right hand side why and therefore if you understood all these basic concepts here and look at the timing diagram therefore and I get therefore this is t clock from here if you measure t clock to t delta. So this is your nominal value and therefore since it is already delta you add delta 2 T clock I get t clock at delta here this is a nominal t clock this is your jitter which you see for the first clock this is jitter which you see for the second clock.

Now if you understood this the right hand side of the inequality does not change because that is basically the requirement irrespective what is happening there. So this right hand side is exactly the same of the let us look at the left hand side and let us see what happens. So therefore t clock since it is a positive H trigger positive skew i get t clock + delta – t jitter 1 – t jitter 2 why minus because your actually compressing the clock right.

So therefore when therefore it is putting higher constraint on the clock therefore you have a – t jitter available to you whereas this is the positive skew it is relaxing a timing constraints. So positive skew relaxer timing constraints whereas a negative jitter will always give you to a not a

negative jitter but positive jitter will always give you a problem constraints in terms of overall issues.

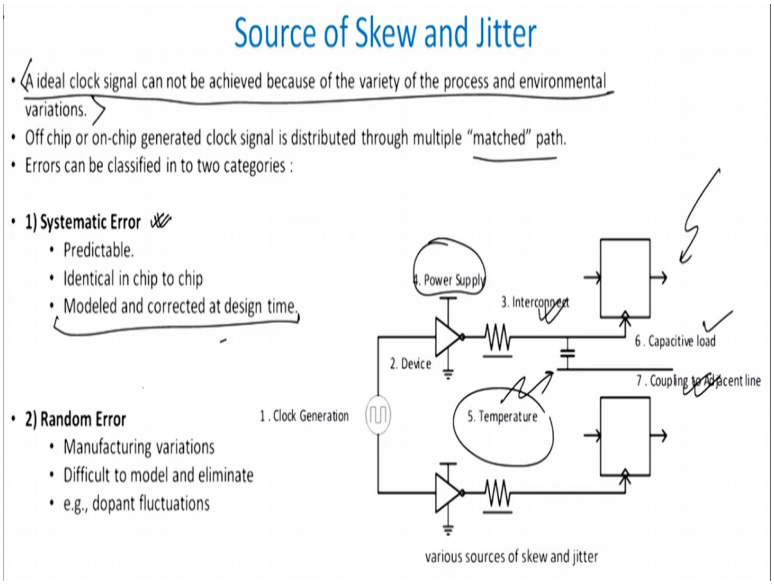
So you see therefore if you shift therefore this side everything I get a new values to be like this so T should be greater than all these things. So if a jitter increase right if a jitter increases as you can see delta increase you are in a best position because it is (()) (13:06) decreasing therefore this overall will decrease and therefore timing constraints will be not too much but if your t jitter 1 and t jitter 2 increases then you end up having larger capital t in order to sustain this whole issue.

So if you are multiple clocks and each of the clock is having individual jitter available to it then the overall clock can be typically clock the overall frequency of the reference clock will be very low in order to sustain this inequality into consideration. So you see therefore or you appreciate now that the problem which is there in a in a clock skew and clock jitter taken in together right taken in together.

If you understood what is basically clock skew and clock jitter and we also understood why clock skew and clock jitter come let us see what is source of skew and jitter right and let us see why it is coming into picture what is the ideal clock? And ideal clock is the one which basically moves from point A to point B in time domain without showing a skew which means that there is no shifting in terms of its raising and fallings edges and it should also not show jitter.

But in reality since you always have long interconnects path you have typical interconnect RLC available you will always have a delay associated with the raising age of the clock or for that matter of whole clock.

(Refer Slide Time: 14:32)



So that is the reason that is what is written here is that the ideal clock an ideal clock cannot be achieved because of variety of process and environmental variations right. So it is very difficult to achieve an ideal clock because of large number of process for example I will give you an brief example also. Let us suppose you have a clock you are driving three sequential blocks in bulk case and five sequential block in other case.

Then the cap loading of the clock itself will change right and therefore the clock will see different loading for different cases so even if the interconnect lens as same if the loading is different then you will also have this problems available to me. So they depend upon the process as well as environment. Environment when I say I mean to say the environment of IC which in which you are placing the whole chip okay.

Now what we try to do is that even if it typically clocks are always generated off chip for most of the cases not all the cases but most of the cases you generate clocks if chip even if you generate off chip or on chip you try to on the signal to the driver where you are driving the sequential logic for that matter any logic through matched path when I say matched multiple match paths. I mean to say that those paths whose RLC elements are exactly the same.

So that even if they are having a skew right individually of them so if individual path is skew but if the skew is exactly the same between the two or the jitter is same between the two they cancel out each other and we will actually able to be see the difference between the two that is the

reason you will have even if you do the off chip or in on chip generation of the clock that does not matter and you will have a matched as long as a matched path you can have a 0 skew and 0 jitter available to you.

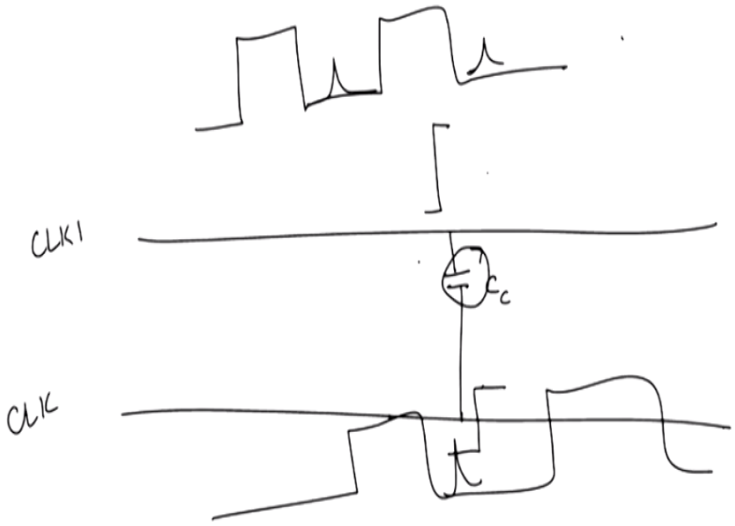
Now the two types of error which occur in a system or in a design let us what are the issues are will come each one of them. So the first issue is basically systematic error right. Systematic error is basically error which is very much identifiable and it does not from chip to chip so if I do the fabricated chip I fabricate the chip in the second lot then with in this two chips they will be known variation they will remain almost the same it is highly predictable in nature systematics errors are and they are generally modeled and can be corrected during the design cycle.

So this are the nothing related to the pure fabrication part but as to do more of a similar logic part so if you can sustain and create your own logic blocks and able to correct it during the design type cycle you will be able to have a reduced systematic errors and they will have a much smaller what are random errors?

Random errors are primarily errors because of manufacturing variation so for example you design a design the say for example simple reason the width of the interconnect actually changes as you move around then the resistive offers changes and therefore you will have a skew that is what is known as a random variation or a manufacturing variations. Now it is rather very difficult to model and eliminate all the issues and therefore some will be there which will give random variations right.

One of them being at the you can have a doppen fluctuation, random doppen fluctuation so and hence so forth that will results in a large amount of change the various jitter of skews and jitter are shown in this diagram which you see in front of you various diagrams I will give you an example.

(Refer Slide Time: 18:17)



Let us suppose you have a you have a clock here and the clock is being routed through this path your this is the clock one and I have a clock two path vertical routed through this path now let us suppose I have a coupling capacitance here because of some problem then a rising edge of the clock here or here will influence. So let us suppose the clock was something like this right and this clock was something like this right.

So what will happen this will influence this and you might get a small over drives here and you might actually get small bumps here small bumps this is be because there will be interconnect coupling through this coupling capacitance here and that will result in a spurious values of output signals and therefore your power dissipations levels can go up right? So this is one which gives you an area that you can have a capacitive coupling available.

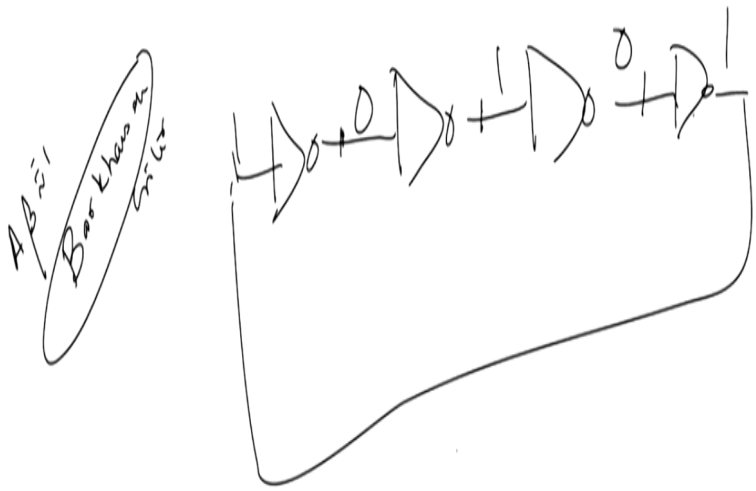
Of course the second one is the temperature now whenever you do a analog design specially at 180 nano meter and above your power dissipation are relatively large right because it is in analog as a name suggest you will have automatically larger power dissipation. So if you doing a on chip design and you power dissipation goes beyond the particular level the clock generating though it is off chip you might a local variations because of temperature.

For example threshold voltage change or even you can have a larger (()) (19:41) effect available to you so on and hence so forth which might result in a change in the value of skew and jitter and that should be taken in consideration as far as is concerned. So we have understood what is the

capacitive load we have also understood a coupling through adjacent line under interconnect with already doing it for a quite clock time and a temperature we just now explained to you.

Similarly the power supply is not stable small variation in power supply also results in large variations in the output right. So these are the we sources skew and jitter in typical circuit sequential circuit which you see in front of you as I discussed with you let us look at therefore sources of skew and jitter once again ahh first look at the clock generation the source of clock generation itself course jitter and the reasons is. Say for example we are taking a VCO right voltage control oscillator right so even oscillator, oscillator is what?

(Refer Slide Time: 20:38)

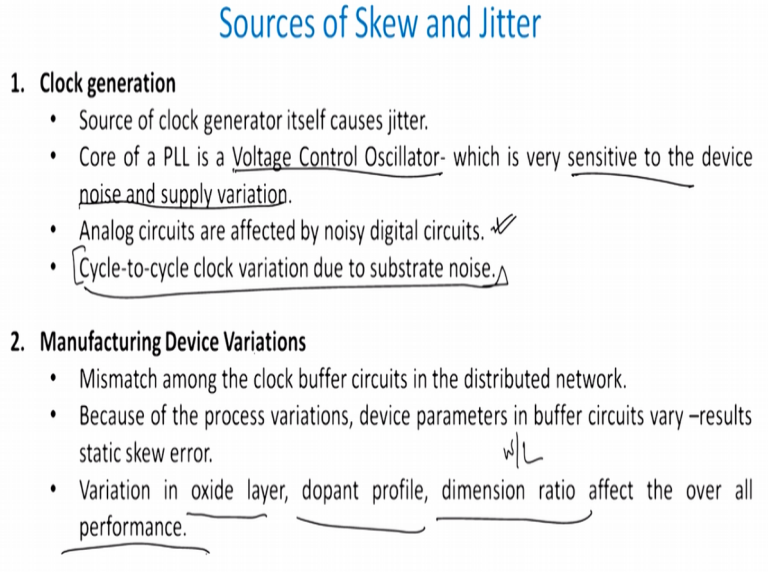


Is basically followed the (()) (20:35) criteria you will have a let us say inverters (refer time: 20:38) which are connected like this and then so this is 1, 0 and then this and this is 1 and it do a feedback path here and here basically a oscillator right very straight and simple we have looking at it that you will provided you are able to how so if you are able to sustain A beta = 1 approximately = 1 and phase difference = 180 degree then you have Barkhausen's criteria and you will have positive feedback available to you barkhausen's criteria will be there a positive feedback will be there (()) (21:11) oscillation right.

But then as you have starting having sustained oscillations you do not care for the fact that there is issue that with right oscillation becomes larger frequency or high or frequency you will have higher power dissipation and therefore one chip power will increase or on chip temperature will

increase which might result in the shifting of the each of the switching threshold of these transistors and as a result you might have a change in the value of clocks skew.

(Refer Slide Time: 21:40)



So this thing you should be taking into consideration as various issues similarly the VCO the core is basically very sensitive to device noise and supply variations so this is supply variation means that your VDD is not very much properly regulated and it is varying slightly your peak to peak variation will also be there in a VCO as well as if the device noise is not removed properly or removed properly you will have those noise coming into picture and if the noise floor is very close to the amplification then you might also have you can also see an amplification of noise itself.

So that is the problem and therefore the third topic was that if the noise is circuits analog circuits are effected by noisy digital circuits right. So digital circuits are typically noise if they are noisy yon can easily remove at digital signal because as long as it is less than switching threshold you can easily remove it but in analog the case is not like that right and therefore cycle to cycle clock variation due to sub state noise you will not be in detail of this one right the last one but the first three one should be very careful about that you should can have your VCO which is primarily the clock of cycle is very sensitive device variation and device noises as well as supply variation.

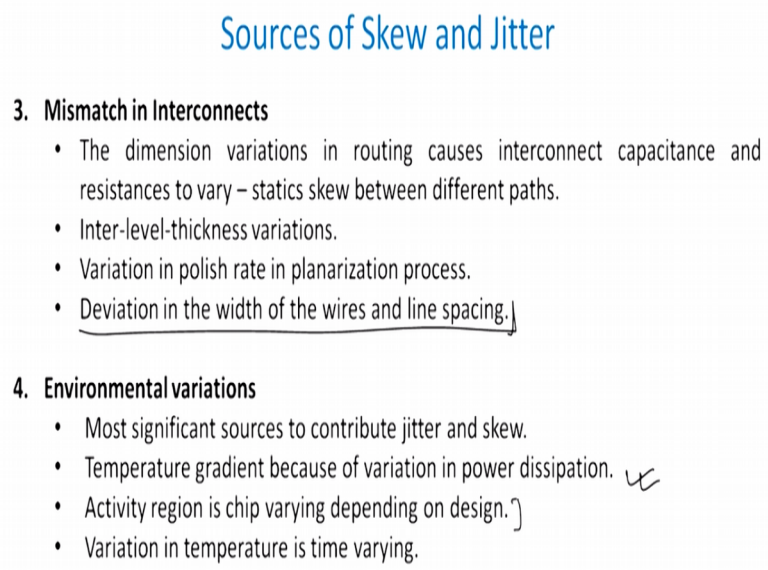
The source itself which is the clock generated itself is very prove to all the variation manufacturing defect variations we have already discussed in the previous slide but primarily say

for example variation lock side thickness and dimensional ratio means W by L ratio if you change then it effect overall performance in the systems. Similarly because of process variation or device parameter variations you might have a problem with the statics skew error also.

So there will be a static skew error will remain with you for long period of time and this as available in the buffer circuit right. So what are the sources of skew and jitter one is basically the clock and the second is basically the manufacturing effect so these are the two major implications right. The third one is basically mismatch integrate which have already dealt with you that if the routing interconnect is not equal lens then you will have a mismatch in terms of capacitances and resistances and therefore they will be static skew between the different parts clock.

Then let us suppose as I discussed with the W so interconnect with have thickness either thickness is not properly maintained across the whole region you will have local variation or thickness variation as a result you will have resistive variation taking place here.

(Refer Slide Time: 24:18)



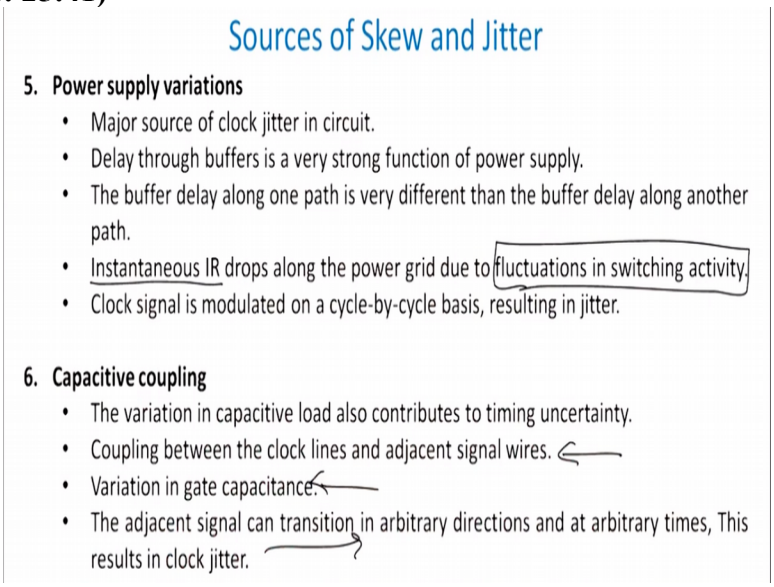
Then similarly that that is the fourth point that you will have deviation in the width of wires and line spacing and that will make it very difficult for it to do. Let us look at the final environmental variation variations and power supply variation can capacitive each one of them. We look at environmental variation this is the in fact environmental variation is the most significant

variations which effects your jitter and skew right and that is the most influential sort of mechanism which it does.

If you have a temperature gradient which is written here because of power dissipation level if the temperature gradient that adds to the skew drastically and then if the activity so for example so you are using a high facility power of the chip right whether data is moving very fast and it is activity factor is very high then the temperature there will be very high as compared to a part where activity fact is low then there will be temperature gradient between those two regions which we result in a distribution of the clock getting disturbed you will have clock available at that particular point skew available at the particular point.

Let us look at the power supply variation as I told you this is one of the major reasons for clock jitter not for skew but for jitter power supply variation and the buffer**.**

(Refer Slide Time: 25:41)



So if I have a two buffers so I have a clock I have a buffer now if the buffer power supply for the power changes the buffer output impedance the buffer impedance level will change right and therefore the two identical buffer which was earlier identical will not be same under the different power supply which will change your variations rare.

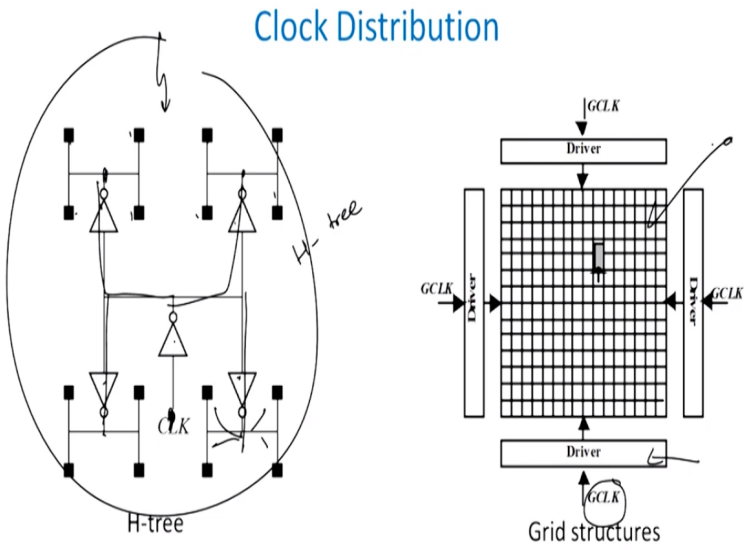
Then another one is that instantaneous IR drop is basically means power drops so if your current flowing is resistance did your fluctuations in switching activity. So a particular so let us suppose you have at a particular point switching activities 0.5 and suddenly the switching activity raises

to 0.9 or 0.85 then you have a larger activity there and because of which they will be heavy large IR drops here right because current versus resistance drops will be larger in that case.

And clock sequence therefore modulated from cycle to cycle basis basically result in a jitter what we got is for capacitor coupling as I discussed with you will have coupling between clock line is an adjustment signal wires and therefore variations gate capacitance is this will be there and as a result you were result in a jitter because the adjustment signals can transition at arbitrary directions and arbitrary times.

So if two signals are very close to each other you will have each talking to each other through capacitive coupling and there will be change in jitter as far as this is concerned. How to reduce therefore skew and jitter right that is quite interesting a best example is to balance your clock and I will just show you one of the technique which people use.

(Refer Slide Time: 27:11)



For example if you look here is basically this is H tree which you see in front of you H tree is if I have a clock here and clock is routed through exactly the same interconnect lens in the four regions for example then we define this to be as H tree. Then you have a you have a clock here right this is the clock this is the driver clock and it drives therefore it drives therefore this invertor which drives this this and this and therefore you have a clock here.

If you are driving with equal interconnects in all the directions these clocks will be identical in nature because the interconnect length from this clock is each one of them is exactly equals in dimensions this is known as in H tree clock distribution n path H-tree clock distribution path right. So that is how we discuss so a balance clock from central distribution source using H-tree or routed tree structures is a best technique for reducing skew jitter what we do is that rather than having a single clock and routing it through large distances if you can have small clocks in routing distances are minimized your jitter will be minimized to a minimum.

If as I discussed with you if I do an if I do negative delta it will be quite good so data and the clock if they move in opposite direction then we can remove the skew in that case avoid data dependency noise but shielding clock wires from adjacent signal bias which is well taken Dummy fills are generally done when you do a lay out and when you send a chip for this thing using a skew.

And also high frequency power supply variations should be restricted on chip right and therefore that is what we are trying to say so I have this has H tree which you see in front of you. I also grid structure where I so I have a global clock which drives the driver and the driver drives it across the chip and you have a grid this is basically a grid which I am talking about and across the grid you will have all the active devices available to you right.

So this is the typical clock generation which is here so what are the advantages of synchronize design advantage is that that when the system also steady state and after the clock starts only you are able to sustain a proper functionality of the chip and therefore the next step clock pulse comes you are able to sustain the computation in the proper manner.

We have also taken the worst case physical timing constraints with in the synchronize design and you the second part is that you can actually embedding a logic within the sequential structure and that is quite interesting people I have seen it for quite a long time and therefore since they are acquisitive by clock you will always have fixed delay available to you. So with this we are ending the module on clocking strategies and I will recapitulate to you what we have learnt till now.

(Refer Slide Time: 30:00)

Recapitulation

- As a result of process and environmental variations, the clock signal can have spatial and temporal variations.
- Clock skew and jitter has a major impact on the functionality and performance of a system.
- Clock skew is caused by static path-length mismatches in the clock load and by definition skew is constant from cycle to cycle.
- Realize in clock distribution is that the absolute delay through a clock distribution path is not important; what matters is the relative arrival time between the output of each path at the register points.

That you will always have a clock Q and clock jitter but you can reduce it by reducing the environmental and process variation clocks skew and jitter as got a major impact and functionality clocks skew can be reduced by doing large number of techniques we have already discussed but the primary technique available to us is that if you route the clock across equal paths matched path you will have that thing.

Environmental variation and power supply variation results in large amount of changes skew and jitter you have minimize this thing reduce it to the larger value and then similarly reduce the coupling capacitive coupling between the signal line, signal line and clock line otherwise if you letting it go there any change in the signal line will change a clock line and so on and hence so forth so with these words we have understood what is basically a clock how a clock works in a synchronic design what is skew and jitter?

What is set up timing able time evaluation constraints how we can improve it and how we can remove clock skew and jitter for practical problems such as how sequential logic design is available to you right with these I will stop at this stage thank you for your kind listening thank you.