CMOS Digital VLSI Design
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Module No #07
Lecture No #34
Clocking Strategies For Sequential Design – II

Hello everybody and welcome to the NPTEL online certification course on CMOS digital VLSI design and we will start with the second module of clocking strategies for sequential design this is the topic were we are actually looking into the various clocking mechanisms available to us for the synchronize design in a sequential circuit. We have seen in the previous module about the various issues related to clocking we have understood what is asynchornize design and synchronize design.

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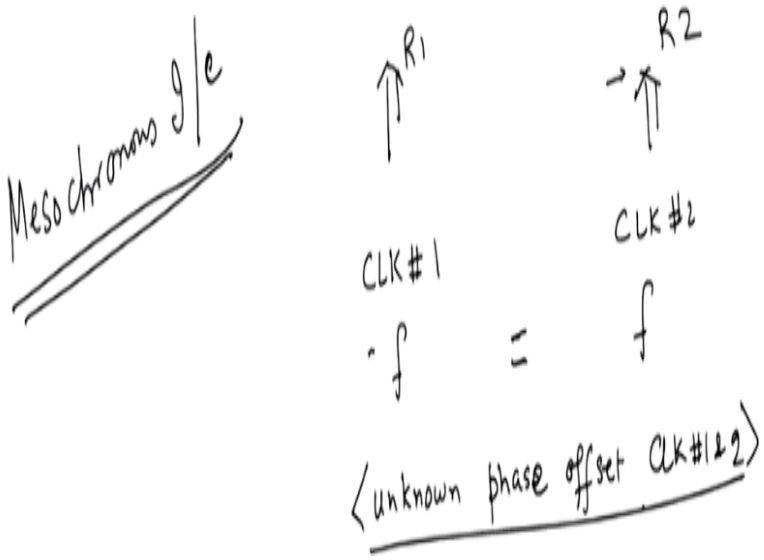

One thing which we have left in the previous turn is basically look into what is known as mesochronoms right we are not done in that mesochronoms interconnect based on this we can also have this what is mesochronoms interconnect do is that if you got two clocks right clock 1 and we have clock number 2 right then if both are having the same frequency right the frequency is are exactly same for both the cases.

But there is unknown what is known as a phase offset between clock 1 and 2. So this is unknown phase offset between 1 and 2 then there is a problem thought they are having a same frequency

but the phase difference between them in real time. Which is there mesochronoms interconnect then the problem is that you do have problem of mismatch of data and as a result the data which were sending through mesochronoms interconnect will obviously have a constant phase difference between clock 1 and clock 2.

Now if clock 1 is say driving register 1 and clock 2 is driving register 2 then you have not very sure that whether your sampling is done properly at register 2 because of this constant offset between clock number 1 and clock number 2 right. So as a result is always a problem of wrong data been sampled or even some noise may be also inserted into the system for mesochronoms interconnect based design. Now this unlike the pure synchronize design here since there is unknown offset available to us we required to do some what is known as delay monitoring or delay affirmation techniques. I just give you brief design of the delay of a affirmation techniques and from these we can see how do work with them?

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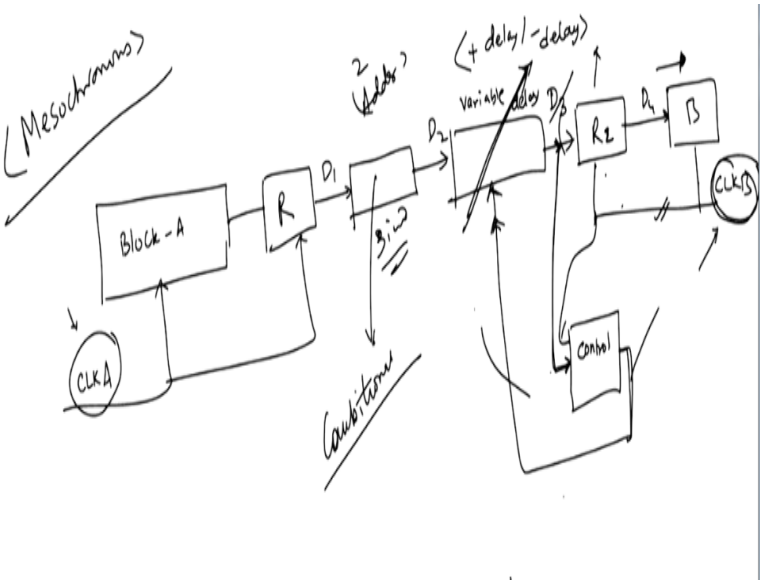

Let us suppose i have a block a this is block A so this is basically a block which is basically logic and then register here R right. And both are driven by let us suppose clocks so I have clock this is given by clock A let us suppose and data is fet from here D1 and onto the your interconnector and then this goes to D2 right. And as a result let me say you have a variable delay this is variable delay and I will explain these things just now this is a variable delay elements this goes to shift register R2 and from R2 is goes to the block B.

It is again a combinational logical block and this register and delay are driven by clock B this is clock B right and this is register I also have control unit right this is a control unit let us see how its workout? That this input will from here to this point will be the input and output will be basically like this and this control will also been controlling the clock here this is general diagram of mesochronoms design right so let us suppose clock A and clock B they are not mesochronoms.

Which means that they have the same frequency but there constant offset between two which is offset between clock A and clock B right there are only two clocks in the system there are offset. As a result what will happen is by the time a data goes via D1, D2 and then reaches R2 you automatically have some delay available to you but if you are able to make the delay equals to the difference between the setup and old violation times your there will no problem at R2 but very fact that clock B phase is unknown.

And we are not able to figure out the difference between clock A and clock B phase. It becomes very difficult, so what people do or what things have been done is from the variable delay line output you drawn line in a output control bit. So this control bit times to control both your clock as well as data feeding capability of variable delay line so let us suppose this phase of clock B was delay which means that I have to add extract delay into my data path.

So that it just false into the versing edge of the clock B so what are do this control unit seen the bit here the variable delay unit we need not understood and getting it but primarily I can add delay here so delay can be added or delay can be subtracted right can be sustained either two can be done and once you have added sustained the delay right you then end up having then the absorbs issues.

When you do have search a system then the delay coming out the data coming out at this point which is let us suppose D3 will are either be delayed are slightly less delayed as compared to previous case and it will come rising edge of the clock B. right and therefore there will be a proper register now this once you have done that assuming the clock A and B are perfectly synchronous which respect to each other.

And this constant phase difference you do not have do it large controlling beyond this point here already showed that the data available at R2 which is D3 is primarily synchronize with the rising edge of the clock B and therefore you are happy with the statement you can have therefore the actual value coming out D4 on the block B which is basically combinational block let us suppose so this is the an interesting design for mesochronoms circuit and it works fine for mesochronoms circuit which you encounter it right.

These are all where they are useful in those area were your combinational logical blocks migh not have fixed delay right but I will discussing right after the slide maybe later on they might be many false part with in the combinational logical block and these false paths needs to be removed and you only should have the true path or critical path available between the primary input and primary output of the combinational logic.

So if this is the combinational logic I am taking about right and this combinational logic is basically changing with respective overall system. For example let us suppose this have adder and then suddenly I required that rather than two input or it want to be a three input let us suppose adder then the delay will change across this path and then what are I do that will be closed control therefore this delay as to change so that it is come to the rising edge.

The cost i pay for it increase complexity and second part is that reduced the timing constraints because the whole timing constraints will be taking care of this slide and this R2 and therefore this timing constraint is major concern for this whole design. Let me therefore come to the next like we will discuss therefore the next issue which we had left in the previous turn we have finish with mesochronoms we have understood what is synchronous design?

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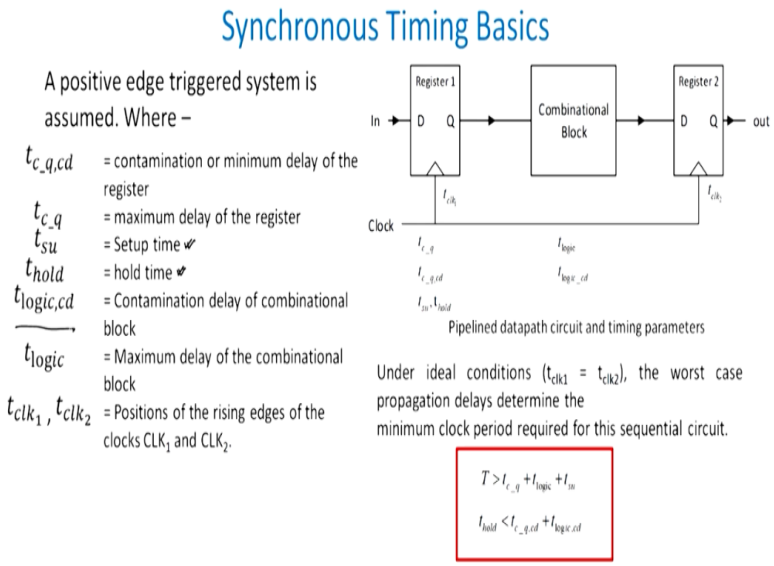

And let us look into synchronous timing basic I discuss with you yesterday only on the previous time that you will have a setup time right you have whole time setup time therefore time taken before the rising edge of the clock when the data should be stable how did you define the whole time is the time after the clock it as passed till which the data as to be held stable upper your evaluation right so this much time you have give what is contamination delay with is t logic cd is basically the delay of the combinational logical block right.

And you might have two input NAND and two input NOR and even have a XOR whatever you have that delay be input and output of that logic is defined as the t logic cd comma CD we say. So Cd id the logic which you seen in the t logic which you in front of you right therefore called logic block now combinational logical block delay can be measured or extracted if you know individual delay of each element right and typically the delay as I have discussed discussing combinational logical block strong function of the input data right.

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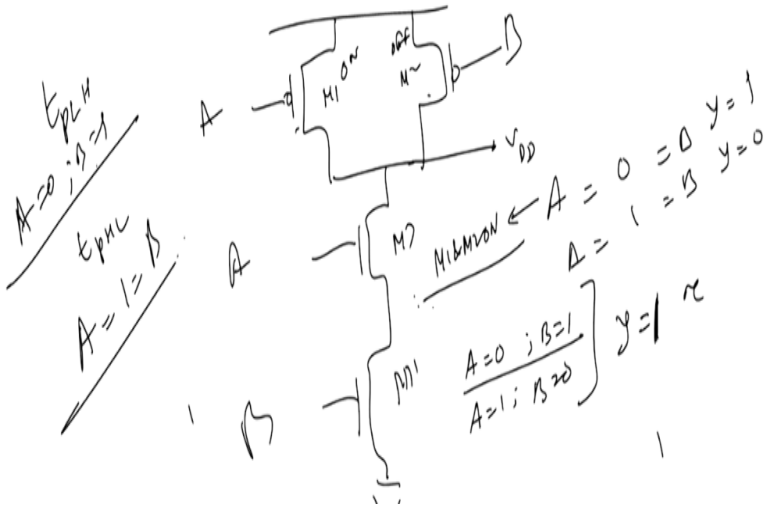

So how you input data is been fed based on that also your delay will be larger or smaller I will give an example which have already given to you in the previous class that let us suppose I have a gate structure in which this is there I have this thing right this have two so this is basically your gate A, B and this is A and this is B so when A and B are both 0 right this output will be equals to VDD right so this NAND gate basically.

And when both are equals to 1 right then y will be so y will be equals to 1 and y will be equals to 0 fine. So this is already now to have let us explain anything more than that but le us see what happen if A equals to 0 and B equals to 1 or A equals to 1 and B equals to 0 in both the cases you will see that the output will still to be equals to 1 because one of the transistors on in that case but then the path resistance will be higher because initially in this case both the transistors.

Let us suppose M1, M2, M3 and M4 both the transistors M1, M2 were on and therefore the overall resistances in this path was much larger because these two are in parallel whereas when A equals to 0 and B equals to 1 you automatically have only one on and one off and therefore this path resistances is slightly increased as a result what will happen though you will get one but your tau will be typically larger tau will low to high right.

So therefore it is data depended so when I say that your t logic cd is the contamination delay of combinational logical block it might be true that this might be a variable depending upon the type of data and type of logic implementation you are doing on the block set right so generally

what we try to find out is we find out the worst case delay available to me as in previous case if you look the worst case delay of tp low to high and tp low to high is basically 1 is also 1 when A equals to 0 and B equals to 1.

So we try to find out the delay under such a criteria that your worst case delay is always measured right for tp HL high to low is only one path available and that is equal to A equals to 1 and B equals to 1 this is no other way you can actually do a tpHL. So tpHl is very straight forward tpLH is not straight forward but depends upon the data you giving how what inputs you giving it all depends upon the fact that what is the effective W/L ratios of individual transistors.

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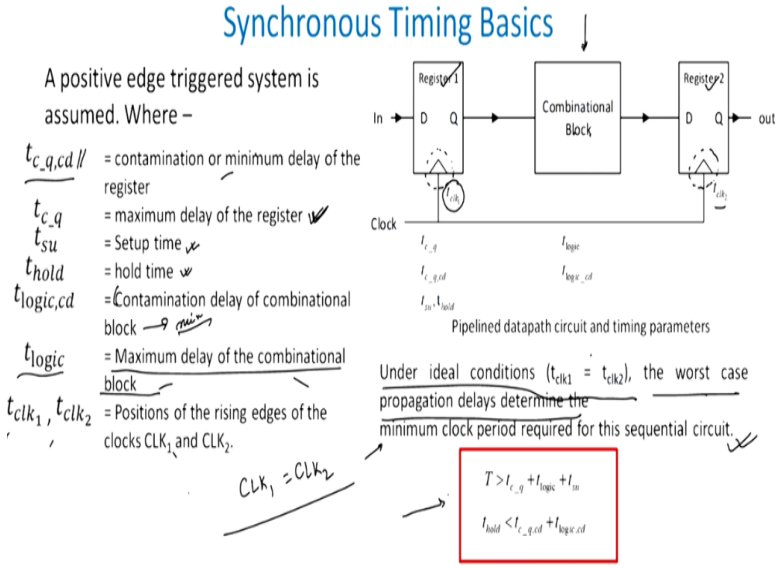

But if you assume A equals to 0 and A equals to 1 or vice-verse will A = 0 and b = 1 will your tpLH will be strong function of the and we try to find out the worst case in delay. So please understand this logic which you see here is basically the this logic is basically my worst case delay right the maximum worst case delay which you see. this is basically contamination delay and t logic is basically maximum delay of the combinational logical block right.

So tc logic is basically contamination delay primarily meaning that depending upon the input delay will changing whereas t logic is maximum delay which is the worst case which is available to you t clock 1 and t clock 2 if you see which is this and this are basically positions rising edges of the clock 1 and clock 2 right so this are the position of rising edges of clock 1 and clock 2 so you have two clocks clock 1 and clock 2.

So the rising edge point is basically clock 1= clock 2 typically I assume there are no problems the clock 1 = clock 2 with the rising edge perfectly balanced with respect each other. Let see if you have therefore which I have discuss here on the left hand side of the slide ahh let us look at ok we have discuss setup and whole time is this also another time which tcq which is basic the maximum delay of the register.

So you will always have a register available with you and the maximum delay of the register will be defined as a tcq and minimum delay of the register will be tcqcd right so contamination delay similarly this worst case this is basically a maximum delay right and this is basically your maximum delay and this you are here this basically the min delay minimum delay right. So your min delay or max delay similarly in your min delay or you have max delay here so you have min max delay available in your logic diagram.

So if you see timing basics here we do have therefore two registers here register number 1 and register number 2 we are combinational logical block which is basically a block between register 1 and register 2. So this is combination logical block and the combinational logical primarily consist of only combinational logic this stage of time. So it is not time basically clock driven it is data driven right now as I discuss with you tclk one is rising edge and see since edge triggered I have put a triangle here right.

And similarly triangle is here also which is basically showing that it is basically edge together and tclk 2 right now under the ideal contusion as I discuss with you tclk1 must be = tclk2 right.

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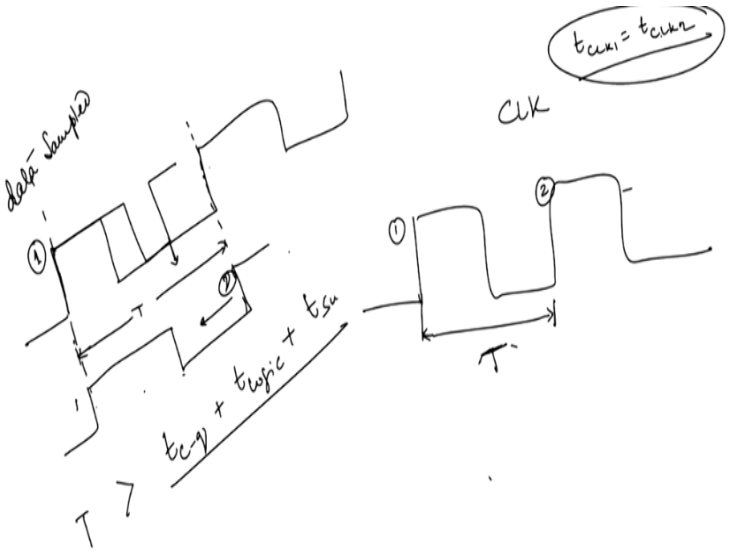

And the worst case propagation delay determines the maximum minimum clock period required for the sequential clock design right I think I need not to explain you because that is what we are find out we try to find out the maximum propagation delay right then open upon that will be minimum of clock frequency which you see available to you right. So this let us look at red colored square box which here made here what as tell me is that the timing of the clock capital T.

Which means that capital T is basically the clock period which you see so I have a clock period so clock period between this part rising edge to the next rising edge this is capital T at the clock right this is clock for the clock which you see the difference between the two rising edges of the 1 and 2 rising edge the difference between them basically capital T right this capital T at least larger than right it should be at least larger then tcq + t logic + t setup.

I hope you understand this clearly we have already discussed in early also and the reason is something like this that as I discussed with you that t logic is what? T logic is basically the maximum delay of the combination logical block right so when data is passing through register 1 then going to combinational logical block to register 2 then the delay offered by the combinational of logical block here is equals to t logic right.

And please remember the register as to wait till setup time has been utilized for the data to be sampled so you add t setup to logic and then you will also tq delay which is tcq delay here which basically the maximum so since the maximum delay where in the register 1 so I have delay

which this place to this place delay I have the combinational logical block delay but also with at least the t setup for this to be true.

So if my clock period is anything less than that right then what will happen is by the time data reaches here your rising edge of clock already passed by right you are getting the point so that is the reason the frequencies limited by these three factors tcq, t logic and t setup iam suppose I am able to explain you I show it you by a diagram may be and so if you have a clock pulse which is like this have a clock pulse this is capital T.

Which is basically the time period of the clock pulse right this is capital T here and here now what I time to tell you is say at this edge your things are getting register right and assuming that both the clocks are ideal and tck so assuming tclk 1 is equals to tclk two right with this assumption I am assuming therefore the edge number one data is getting sample right data is sample now when the data is sample it takes tcq delay right + t logic delay.

Which is basically because of combinational delay and you have setup delay here right if you add this three delay if T is not greater than this if T is less than that then what will happen is that this will shift somewhere here so if this is smaller then this goes like this and then this so it would have been here but your data would have been ready for sample only at this particular point fine so what has happen that you have missed.

The rising edge of the second clock for the data to be register which second clock this is between the registers. So this is one and this is second one which you see in ideal case your registering at one node and you will be registering at two node but would timing have been shorted this two node have shifted in the left by the time your data would have be ready to evaluate you actually have no data to evaluate right.

Sorry you do not have any clock period you do not having rising edge clock available to do any sort of sampling in this case. So with this we therefore come out the t should be get tcq + t logic + t setup. The other aspect is this one the second one but t hold shoud be less than tcqcd which is the minimum delay of the register + t logic cd this is minimum contamination delay of combinational logical block you remember what was the t hold?

T hold was the time minimum time the clock pluses accurately passed the time taken from the data to be stable now if that time period let us suppose is larger than these two values which is tck, tcq.cd and tlogic.cd which is basically the same of minimum delay of your clock of your register and the combinational logical block then what will happen is that your data will be starting to move across even before this is actually passed you getting my point.

So let us suppose t hold was actually larger than this two objects right if it is true then what will happen is that the data as to way till much now so your time was this much but you want happen was even before that the data starting of fluctuate right because you have not violated tcq and t logic.cd as a result you have to minimum delay of t hold in order to ensure that these logic are properly working.

And it is synchronous timing diagram available to you so these are the few details with you should be very careful about as for as logic are concerned and so the idea here is that if you cannot make any one of them 0 because of reality there will be some values available you but try to make as minimum of possible to in order to enhands the frequency operation of a devices with this let me come to the next problem area of a sequential logic and that is clock skew.

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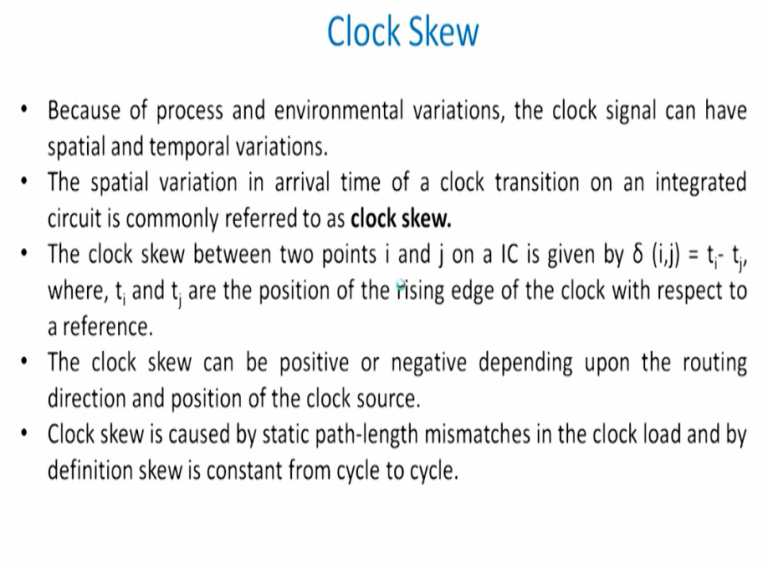

We will discuss about clock skew and clock jitter so first of all we take up of clock skew into consideration what is clock skew? Let me explain to you what is clock skew and then we will be discuss clock jitter what happens is when you routing a clock skew.

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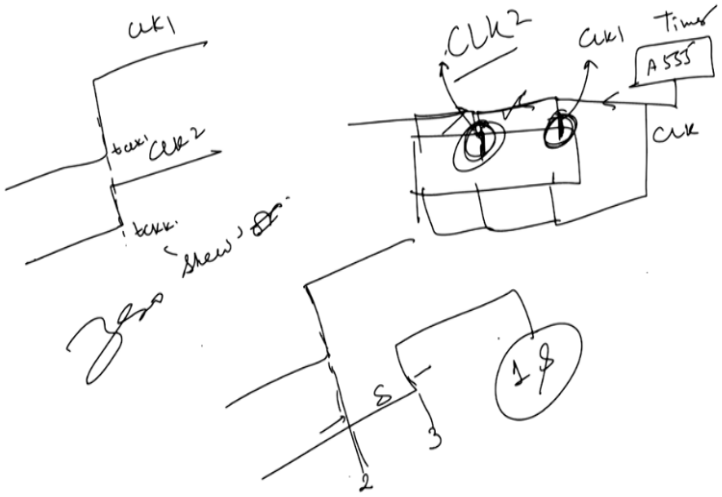

See generally as I discuss with you in the previous turns also that if you have a chip generally the clock is stable let us suppose 555 right and you have 555 timer here. And you routing the timer you putting it inside the clock I am showing it in laymen sort of language and therefore you routing this clock across this path right what has happen let us see what problem is there when you are routing the clock across large lens of paths right.

Then let us suppose you want to see a clock here or even here but please understand because of the length of the interconnects are not equal you might have extra RLC elements in this case as compared to this case. As a result there might be a problem of will see skew first jitter later on the primarily of skew and I will explain what is on about it skew if look back something like this.

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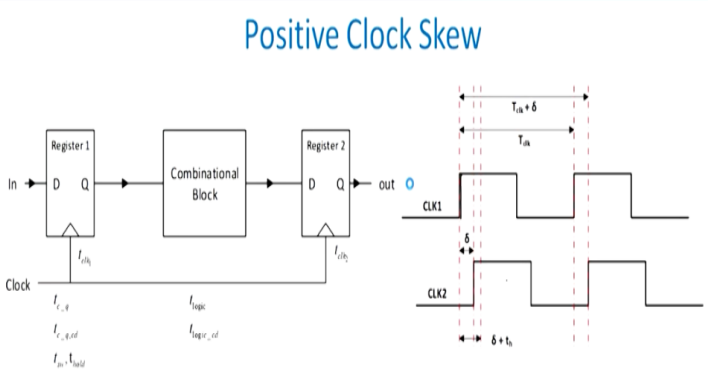

Timing diagram to study the impact of positive clock skew on performance and functionality.

The rising clock edge is delayed by a positive δ at the second register.

Skew basically means that say this is clock 1 right and what has happened is clock 2 which was basically suppose this is clock 1 and let us suppose this is clock 2 by virtue of the fact that this is clock is further away from clock one more interconnect length has been covered by clock 2. What will happen is that clock 2 will come in temporal domain in time domain at bit late right that what I am showing here that if you look very carefully clock 2 is arriving after the period of delta into the system right after coming a period of delta into the system.

And therefore as you can see it is will also have it time period shifted by factor of delta so capital T is this same for both the cases but there will be a temporal domain shifted to right by clock 2 this is known as clock skew right. This is known as positive clock skew if clock 2 appears after clock 1 in the same time domain and it have negative clock skew if clock 2 appears before clock 1 right and so it will be very consumes what is data flow? I will give an idea for example let us suppose the data is flowing from this direction then this will be more delayed as compared to this one this whereas the data is flowing from this direction this will be more delayed as compared to this one.

So depending upon the direction clock flow you can actually see or understand whether the your skew will be positive or negative right that the reason we put this positive, negative skew in the very detailed manner in this case. With this idea let me show you what the previous slide in will go there so because of the process and environmental variation the clock signal can have a special as were as temporal variation special means in space.

It might be shifted or in time domain may be shifted in the right to the left now the special variation of arrival time of a clock transition on a integrated circuit is commonly referred to as clock skew.So if you look very carefully is this diagram the rising edge of clock as actually shifted to right this is skew so when this shifts to the right all other data points will also shift to the right and this is positive clock skew which you see.

So this is what I define as positive skew right so let me discuss with you therefore what is the clock skew and therefore as I discussed with you special variation as defined as my clock skew let us suppose that you do have so let us suppose ti and tj right are the position of the rising edge of the clock with respect to a references I have the references and ti is basically the rising edge with respect to references and tj is references of the second clock.

Then the differences between ti and tj is basically my del my clock skew. So clock skew is define as ti - tj I will show you a diagram show that so let us suppose I had this clock 1 I had this clock 2 clock 1 and clock 2 right there externally I get t clock 1 is excitably goes to t clock 2 so both of them then the skew is 0 but if you have a clock 1 here and clock 2 shifted in time domain in this much manner.

Then you always have a positive skew is available here right and this positive skewed results because of the environmental changes process variation, temporal variation on so on and so for so that what the reason here and we define it to be the difference in time domain so this differences in time domain suppose this is appearing at 2 seconds and this appearing in 3 seconds the 2 second is basically the clock skew for this circuitry ok.

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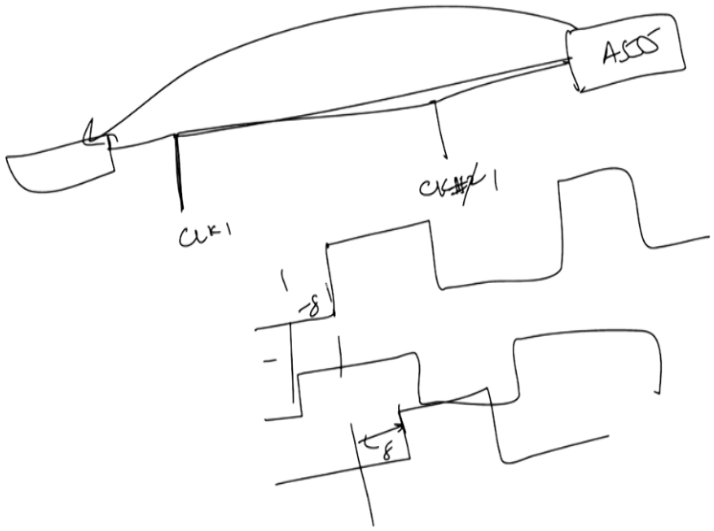

As i discussed with you the clock skew can be both negative or positive right and will depending upon the routing direction and position of the clock source I think this is clear to you I suppose for example I will give you an idea let me give you an idea to make it clear let us suppose I have a clock 1 here and clock 2 this is clock 1 and this is clock 2 here right and I have a signal A stable multiple vibrated 555 here which is current source then obviously clock 1 will be delayed to respect 1 to clock 2.

If I draw clock 1 here right I draw clock 2 will be coming ahead of and if this the reverse would have been this is clock 1 or let me reverse the case and put it here then clock 1 will arriving late clock 2 will be arriving delay right. So this is known as positive skew and this is known as negative skew fine that is the difference between the positive skew and negative skew this think is there now this is clock skew is caused by.

As I discuss is know the path length mismatch in the clock load and by diffraction is there constant therefore skew is constant to clock two issue remember to closed it this issue here the first is that depends on the path length nor to the master clock to the next clock phase it is the total length with matter so if the length is not equal you will always the getting a clock skew also if the clock loads are high with means that the clock loads are variable hen also you get a what is known as the clock.

So the clock skew is primarily which is basically depending on the process and process and environmental variation it can be positive and negative depending upon whether the clock

direction and the clock in the opposite direction and so on so for and it is also cost from cycle to cycle so once you fixed the value of delta which is the clock skew you no generally effect to change over the various clock cycler right it remains almost constant for all clock cycle for matter so these are the basic concepts of the clock skew and in the we will discuss this part in next turn when we take a combinational logical block and the clock skew here right thank you very much.