CMOS Digital VLSI Design
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Module No # 07
Lecture No # 32
Sequential Digital Design – VIII

Welcome to the online certification course NPTEL CMOS digital VLSI design and today we will start off with sequential logic design module number 8 we have seen the previous slides of previous presentation that we can have a two single phase clock and we can replace it by multiple clock from multiple clock so there is no problem overlap coming into picture and there might be also a issue that the clock load will reduce therefore the power dissipation will go down.

So this are the few advantages which we can already seen the but we will start of we will start off with the slide which we were left in the previous turn and let us see how it works out in this case. So if you look at this this is basically if you look very carefully this is basically a circuit which is used pulse generator here right hmmm.

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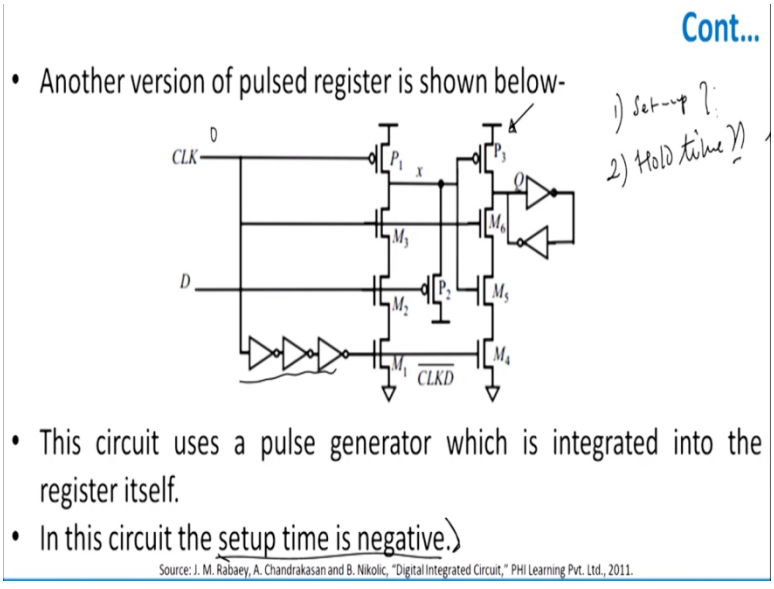

So it uses a pulse generator in order to substantiate for example let us suppose clock = 0 here you get the P1 will be on when P1 is on so when clock = 0 right your P1 will be in on state right and

in the same instant of time M3 and M6 will be off right as a result X will have a value almost = VDD. So that is sort of a pre-charge sort of issue here and therefore X value so this value will go up to VDD right.

Now if D value is equals to let us suppose 1 then P2 is off and whatever M6 is off this part of the transistor we have register is off and whatever VDD is stored here whatever the Q value is also stored at this point is also there but in this case if FD = 1 then M2 becomes M2 is switched on right M2 is switched on but since P2 is off VDD is does not have a path to discharge and therefore it initiates its values = VDD now when clock now if we if clock = 0 then this will be 0 this will be 1 this will be 0 this will be also = 1 which means that M1 and M4 will switched on right when it equals to 0.

Now when if it does a o to 1 transition clock this becoming 0 will occur after a finite duration of time that is the whole crux that means let us suppose I name it as point Z then point Z will go from 1 to 0 after 3 inverter delay why because this delay + this delay + this delay. So after this inverted delay i would expect to see go from 1 to 0 by that time please understand M3 and M6 will be on and M2 will be also on and therefore your M5 will become (()) (03:27) this equals to VDD right and therefore this will get evaluated to point number Q here right.

And this is the basic idea which I am doing but this could only happen between the region when your this point is 0 or so this is the finite duration between 1 it goes to 1 to 0 within that finite duration there will be small glitch generator this glitch and this glitch only you will be able to expect to C the output going as you just cross the glitch and go to a region where again clock goes to 0 at that phase of time Q will hold the original value of its data which is which we are suppose to do.

Since if you look at Q is basically made up of to inverters coupled back to back and therefore depending on their actual W / L ratios the value of voltage will be either stored here Q bar as or as Q whatever you want to do it right. In this case the circuit uses a pulse generator so this part is basically the pulse generator part which is integrated with the shift register itself so the pulse generator and resistor are equally done.

What people have done is that they have actually increase the number of inverters here odd numbers of inverter so you can have in place of three you can have five inverters so that you allow the width of the glitch to be large when you allow the glitch to be large then you allow the this register which is this one to be transparent for longer duration of time and therefore you are able to do it right.

So the setup time here in this case will happens to be just these three inverters so as long as you are able to have your data fixed in the input side more than the delay of this data you will actually have your data available to you and that is therefore as I discussed with you will be negative direction I will leave as a excise to be find out why is it in negative direction which means that why set up time in this case is basically negative right and I will leave it in excise to you.

Also leave you an excise to you to find out what is the actual value of the time right and what is the actual value of the whole time in this case. So hold on set up time for this case you need to find out right let me I have left one small thing we should take care in this case that we have actually discussed with you in the previous case discussion on.

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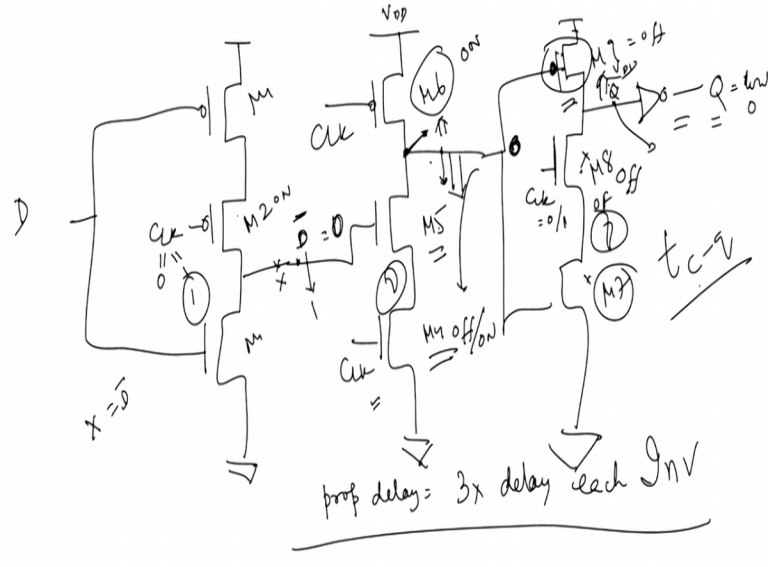

Two single phase clock I will just show you another single phase clock design and show to you that how it works out so this is your clock right and this is what I get as D right and then this is M1, M2, M3 then I get same conceptually the same thing but just a simple design where you

drive it by another clock here and then you drive it by M5 so this is basically M1, M2, M3, M4, M5, M6 right and this is driven by a clock here right.

Then the output this goes to another clock here and then this is M6 so this is M7, M8, M9 right and you been given a clock here CLK and this is fed here and this is fed here this is (()) (06:49). So this is fully of logic which is basically I guess so what you get is Q bar and you get Q here if you look at this logic here when clock = 0 right then M2 is on and therefore at this point I get D bar fine when clock = 0 it implies that M4 will be off and M6 will be on.

M6 will be on primarily means that this M6, M6 will be on means this voltage will go high or this will be evaluated to the high value this goes to high clock will already goes to 0 implies that M8 will be switched off so this will be switched off and therefore whatever happens here this inverters stores the initial value fine. So when clock goes to 0 right M2 is on right when M2 is on this X suppose let us I name it X becomes equals to D bar right X = D bar.

Since clock = 0 M4 is off right but M6 is on when it is on irrespective of the state of M5 the voltage here will go to VDD which is this one right go to VDD as it goes high there is problem here as it goes high since clock = 0 M8 is switched off right but as a clock goes high even if it M7 goes on nothing happens and therefore what is happening when M9 is off and therefore what is the initial value stored at Q bar will be stored and therefore what you get is basically holding the value.

Let us say what happens when clock = 1 when clock = 1 this switch is off the value of D bar which is stored here right so when clock = 1 this switch is on right and therefore this so you have a depending the value of D this will be evaluate either too high or too low. Suppose it goes to low then at clock = 1 then this becomes on if this goes low this acts as a inverter pair and therefore this will appear as high here and therefore this will appear as low here so this will be low here or 0 will be appearing here fine.

Similarly let us assume that this does not change the state which means that M5 is still giving let us suppose D bar here is basically 1 sorry 0 if it is 0 M5 Is still off M5 is still off means it will originally hold a value if now D bar goes to 1 then M5 is on M4 is on now which means I have a pull down path available this voltage here goes down a low value so this becomes 0 here.

Well as it becomes 0 here this this clock is getting again on this 0 means this is switched on this is on also sorry this is PMOS I am sorry PMOS here this switch is ON and as a result you will automatically go to 0 fine. So a so there is one small problem which is there which I should point it out to you at this stage that since this is PMOS under the condition that I have a 0 here right though a clock = 0 initially you might have chance that this will allow this Q to be pre-charge to the VDD right.

So you require a certain amount of (()) (10:13) circuits to remove the voltage here so we have to keep that in mind otherwise that works fine exactly like a this thing and the propagation delay in this case the propagation delay is basically equals to 3 times that delay of each inverter so this is 1 inverter number 2 and number 3 so add this delays I get the total so this is basically tc to Q delay also known as the total propagation delay of the system that is what we have learnt from here right.

So let me therefore come to the original issue let us see how it works we have another type of register which is basically known as sense amplifier based register what is the sense amplifier based register here.

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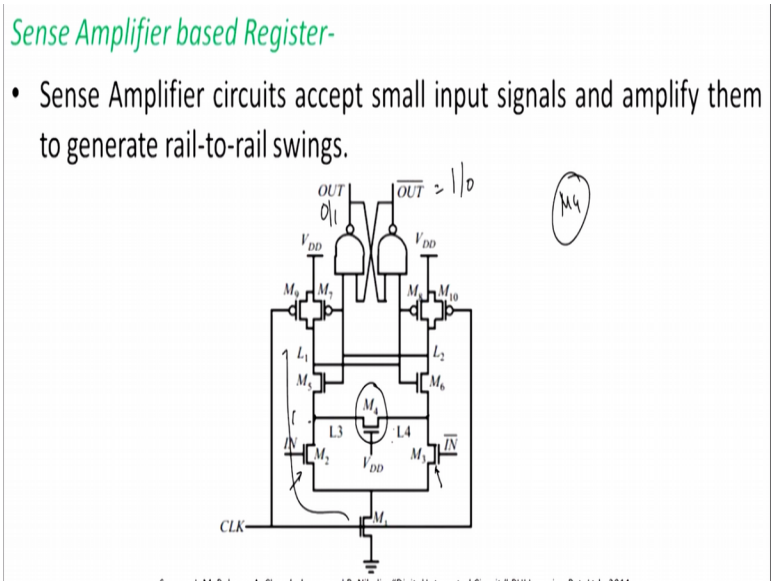

It except what does it do is basically except small differential inputs so I have giving input to M2 and to M3 and I have giving small differential inputs which is basically in and in bar here so their

differential inputs there 180 degree out of phase and we are trying to generate a high swing out of this small differential inputs right that is the reason why we are using this amplifier based register.

Sense amplifier is generally used in memory design where you are actually in memories actually where you are actually trying to sense either 0 or 1 is available and then try to latch it to VDD or to 0 at a very fast phase exactly same thing this this circuitry does to you what it does is basically M if suppose in his high and in bar is low M2 will be on and on the current will be routed to through this arm and therefore M2 will become on which will result in this voltage going up and this voltage going down whereas M4 will do what M4 will try to equalize these two voltages as much as possible.

When this voltages goes up this switch is on M5 and as a result this becomes 1 and therefore out becomes equals to since it is gate out will becomes equals to 0 and therefore out bar will be equals to 1 right. And you can hold this state until and unless you reverse happens that n goes to low and in bar goes high then this will go 1 and this goes to 0 what is the implication of M9, M7 or M8 or M10 help you to swing do a positive feedback and regenerative feedback loop and helps you to improve the P to the circuitry to give you a rail to rail swing.

So rail to rail basically means gives you a VDD to 0 to VDD swing but only problem with this is this it is so heavily lay out dependent as well as highly large number of transistor are used here so the lay out area is also very high and the parasitic are also very high when the parasitic are high the though it gives you a rail to rail swing but the delay associated with it is very large in this case. There is a requirement for M4 is the this this one you need to shorten the transistors for all practical purposes right.

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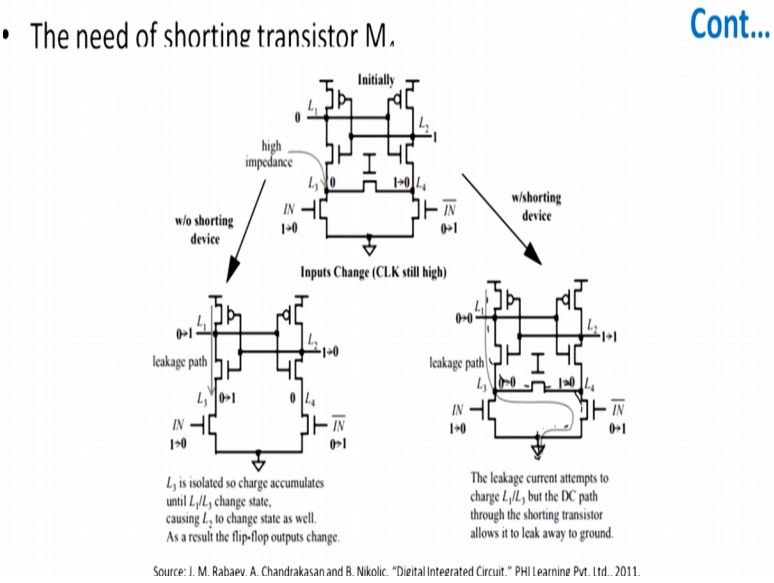

You need to shorten why we why we need to shorten it something like this see if you shorten mean your channel length should be reduced drastically in this case. Now if you shorten it then your resistance offered between source and drain will reduce and therefore all the voltages which flow between this path very close will actually be done such a very fast phase that 0 to 1 and 1 to 0 transition will be very fast.

So therefore try to keep your M4 at the barest minimum right and this is the first thing I am going to detail of this one at this stage because it is slightly require the bit of more understanding at this stage and therefore a design tool is that keep M4 as the shorten stage right with this we have finish the sequential logic designs and that whole about 8 models we have covered in sequential logic design it is basically understood that it is idea of temporary storage static sequential as well as dynamic sequential we also look into the category of dynamic logic.

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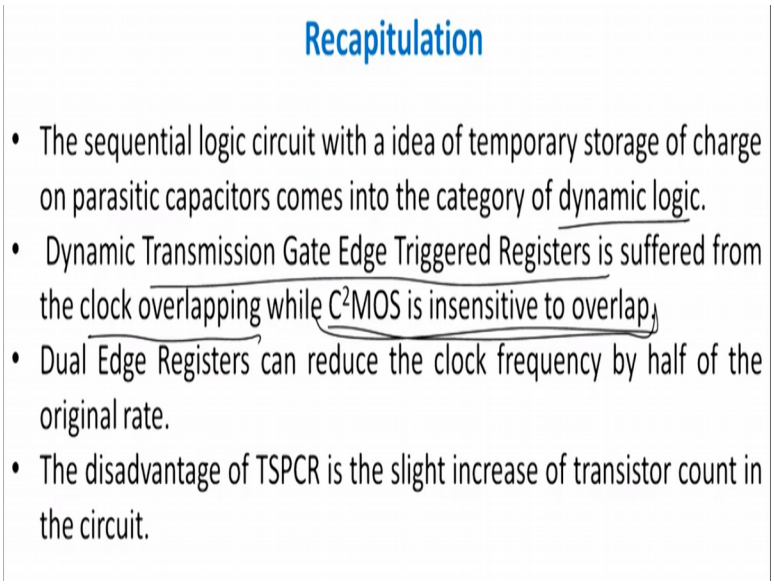

Using TG transmission gate we had discussed H triggers registers and we see that if suffered from clock overlapping 0, 0 as 1, 1 whereas C2MOS is insensitive to overlap that we have also seen that C2MOS is almost insensitive to overlap but the problem is that clock looks a very high and not only that the frequency of sampling is also relatively low because you are only sampling at the positive edge trigger.

Then we move from C2MOS which is single edge trigger to double edge trigger which is also known as dual edge trigger and this can reduce the clock frequency by half of the original rate so you can actually work with double the clock frequency effectively. Obviously the third the fourth type of which we went was rather than using clock and clock bar why it is also advisable you use a single phase clock right since phase clock can be used.

And therefore we went for TSPR logic which is true single phase clock register and there is small increase in transistor count there is one problem and the second problem is that since the clock load is reduced drastically there is no overlap it gives you a slightly better result as compared to the first two gates we ended up our discussion with sense amplifier base shift register wherein we use two nan gates and positive feedback regenerative loop to improve the timing issue and we say certain design issues (()) (15:54).

With this e have finished the sequential logic design all the modules and associated with that we will be giving an numerical problems related to some design problems also related to this thank you very much.