CMOS Digital VLSI Design

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Module No # 06
Lecture No # 30
Sequential Logic Design – VI

Hello everybody and welcome to the NPTEL online certification course on CMOS VLSI digital VLSI design and this module we will be styling on the sequential logic design Module number 6 as a review of what we have done till now in sequential logic we have understood the difference between static and dynamic logic we have also understood what is the timing issues in the sequential logic and then methods for which the timings can be the performance can be enhanced for a sequential logic at least for the static cases right.

Now we actually we will be now discussing the as I told you to in the previous module now this module we will be discussing primarily on dynamic logic design. Now what was dynamic logic design just to reframe your memory was primarily a design which output node will have a value so the static was static design was whenever you switch off you power supply main power that data store at a particular node geos of right

Whereas in dynamic case whenever you will always have a finite time till which node will store a data right and you can increase the time decrease the time but once that time is gone you cannot refresh the memory right. So this was the basic difference between the dynamic design and static design as far as sequential logic is concerned to give a brief example of that we have discussed in our previous turn.

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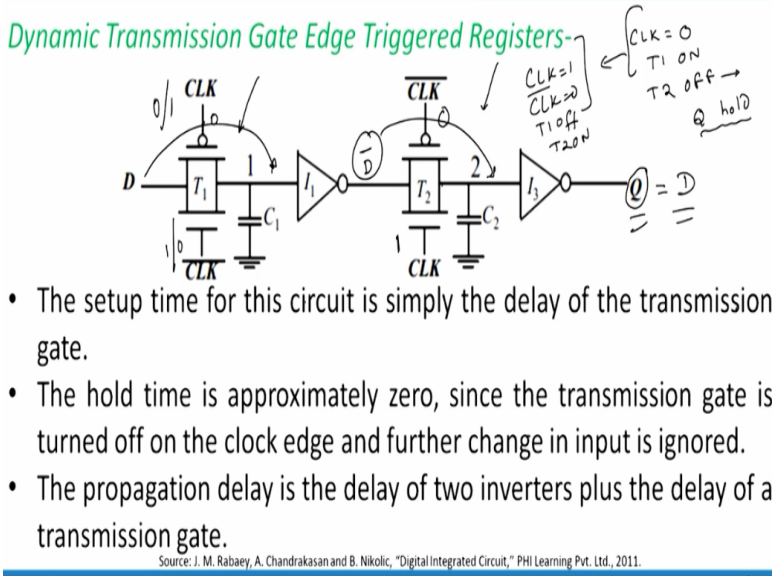

We see that the we see that you have two latches here and this one is termed as master and this one is termed as slave as you can see therefore when clock let us suppose equals to is equals to let us say 0 then clock bar will be equal to 1 so t1 will be one but at the same instant of time t2 will be off and therefore d will be evaluated at node 1 so D will be evaluated node 1 right and then d bar will be appearing at this particular point but since t2 is off your Q will hold the original value of the profile.

So Q will hold till the next phase of clock comes so you can understand that the dynastic comes from the fact that the data holding capacity of Q depends upon the period of the clock when your clock goes to 1 and clock bar goes to 0 from this state to this state so this is the holding period of your data clock Q. So by simply changing by time when the triggering takes place you would be able to change the holding period of data at particular point of Q in the clock.

Now if you look very carefully therefore when you shift from clock = 0 to clock =1 then clock bar = 0 then clock bar = 0 means this is 0 and you get this to be equals to 1 right this to be equals 1 sorry this to be equals to 1 which means that t2 is switched and this is 1 this is 0 right so t1 is off so at this stage t1 is off and t2 is on right which means that t2 is now able to carry forward this D bar forward to node 2 and then node 2 I3 which is basically a static CMOS inverter will again invert it back and therefore Q will be equals to D.

So after 2 clock pulse minimum when the clock goes high to low you will have this Q attaining the new value of D. So your D will be overwritten over that right over the previous value of Q

what is the setup time of the this clock is nothing but the delay of this transmission clock so how did you define your setup time therefore the set time in this case will be defined as the time taken for the data D2 go from this point to this point 2.1 right because you see very carefully.

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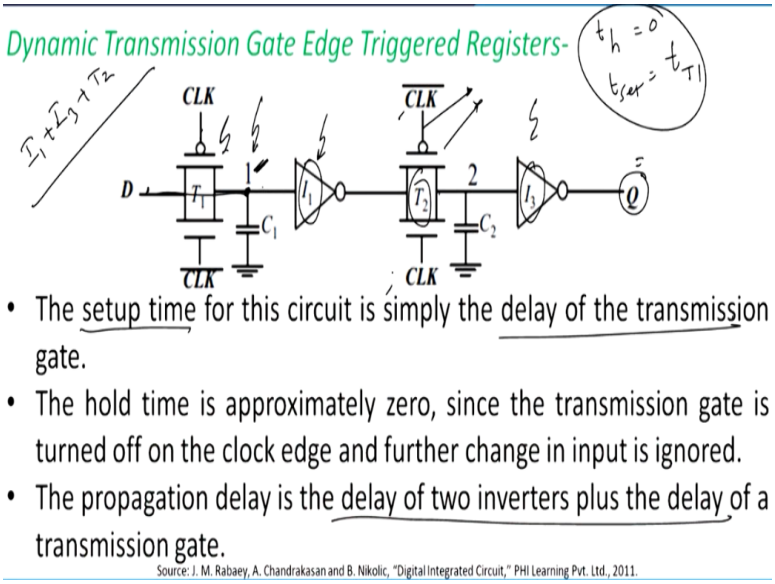

Once the data is available at 0.1 at node 1 sorry your since your t2 is in off state in no way this data at 0.1 right will be transmitted to Q right and therefore the delay of the transmission gate happens to be the setup time of the circuit. So if the delay is large it means that you have to wait this much amount of time before the next data I can come in and overwrite next data right and therefore we define that to be as the setup time of the of this gate is triggered registers.

The is 0 because t1 and t2 are mutually exclusive with respect to each other in terms of getting on so any data which is available on the output of T1 the t2 sees to it only when the next rising edge of the clock happens or the edge of the clock happens and therefore the whole time t hold is basically = 0 so your setup time = t of t1 which is basically this inverter and t hold is equals to 0 but then the propagation delay which you see is basically the delay of two inverters which inverter this inverter + this inverter + this delay of t2 so a data which is available by node 1 can be visible at Q only a after a delay by this static inverter I1 + I3 + T2 so you will have I1 + I3 + t2 so you will have I1 + I3 + t2 as the overall delay propagation delay of the system.

Why do not you include t1 because t1 is already got into the setup time issue so you are only left with that delay between node one and node Q right and that is that gives you an idea about ahh

what is ate edge triggered ahh triggered design right ahh now you see that there is a problem which will discuss next slide the problem is something like this that there is problem which will discuss next slide.

The problem is something like this the problem as we have discussed in the previous turn also that you might have a condition when clock and clock bar might overlap with respect to each other you might know as might ask my why it is possible it is possible because see these clocks are actually routed these clocks are actually routed through a long distance where and then it come to drive t1, t2 , t3 and so on and hence so forth.

So these wire which seems to be small in reality actually a very large wire right it is a large wire it is coming from a large area because your lock are generally off chip and therefore the routing interconnect are very long and there might be condition when special domain or temporal domain these clocks might not be very exactly complementary of each other and there might be a overlap of either 00 or 11 let see what the problem area is.

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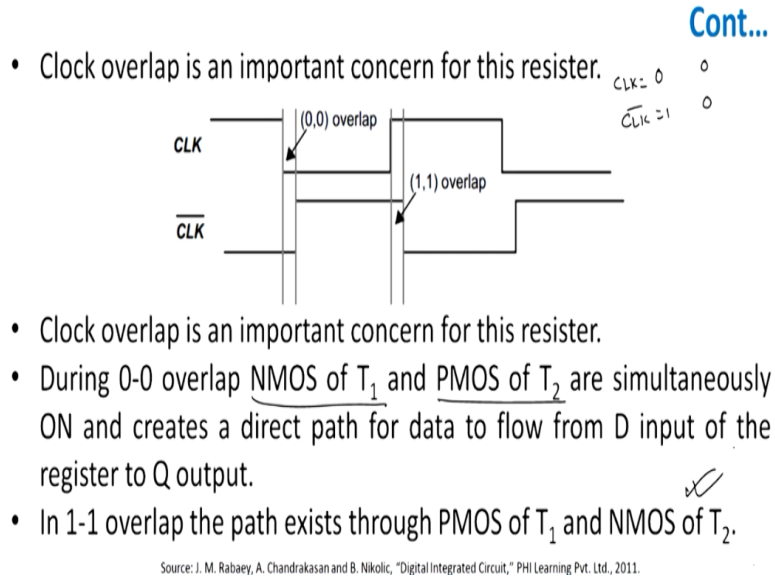

Let us suppose your clock at clock bar overlap at 00 which means that clock should be ideally if it is o then clock bar should be equals to 1 and ideally if clocks equals to 0 then ideally clock bar should be 1 but what i end up is having is 0 clock is also clock bar is also equals to 0. So both are 0 so if you look 0 then NMOS of T1 and PMOS of t2 are simultaneous on will just show you NMOS of t1 right this is the NMOS of t1 and because clock was and clock bar = 1 and what and

so this is NMOS of T1 and PMOS of t2 which is PMOS of t2 is what PMOS of t2 is this one right.

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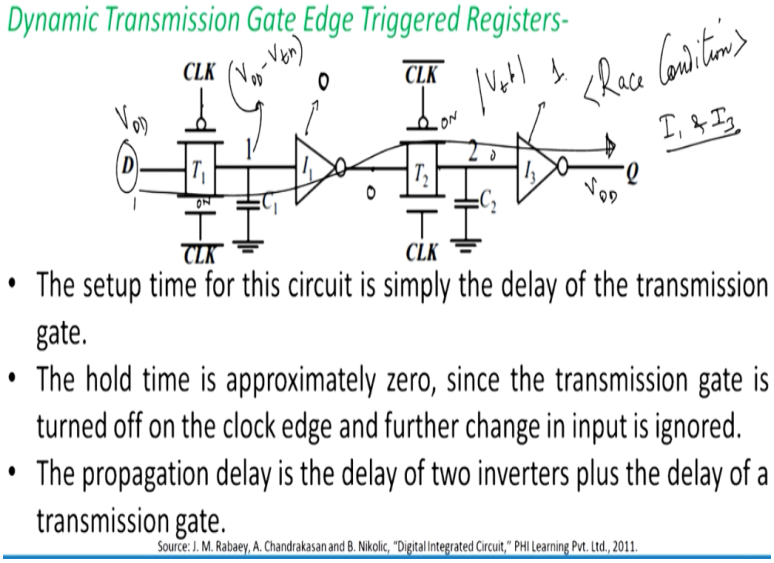

Since clock =0 you will have this also 0 therefore PMOS will so you will have a direct path or you will have if this is on if this is on right then you can have a direct path this and through this to Q this is known as race condition you can have race condition available so what is the race condition your Q is totally transparent and any value of data which you put here will be available at Q right I agree with you that since NMOS is on and PMOS is on anyone which is going through it will also see that threshold voltage drop at t1.

So if I feed a data here which is equals to VDD then 1 which is the node 1 if only NMOS is on I will get VDD = vtn where vtn is the threshold voltage of NMOS right and then it passes through it and then becomes 0 here 0 here and then this 0 is been pass through mode of PMOS so it looks like mode of vtp right and mode of vtp is 0 it goes to 0 and comes out as vtp the only saving point here is since you have static inverters which is I1 and i3 here these static inverters are actually helping you to give you a rail to rail swing.

So these are forcing you to go to fully 0 or to fully one so this i1 is allowing it go to fully 0 and 3 is allowing you to go to only one because these are static inverters so as long as the voltage input voltage is below the switching threshold of the static CMOS you do have a very fast swing at either 0 or to 1 right. The cost to pay for it is of course you spend some amount of time you evaluate the signal right and that is the problem are of this register.

If there is a 00 register in overlap then you have a problem that you make those design transparent having a race condition and therefore during that 00 overlap period you allow Q to be transparent with respect to D and therefore any change in D will reflected to Q this is 00 overlap. The same concept applies for 11 overlap as well when there is 11overlap you will have just the reverse happening that this will be on PMOS so PMOS of T1 of T1 and a you will also have NMOS of t2 they both will on under 11 overlap condition.

So on one overlap condition they will be on and again the same procedure will be followed and then race on condition or a race conditional available t you and therefore it will be transparent to each other DNQ transparent to each other which I have written in here exactly what I have written it here. So how do you go about removing this thing best method to remove things is do not let overlap happen at all so let them be far apart from each other so that so possibility of an overlap earlier or we can also have clock as discussed in the previous module where the clock phases are defined in such a manner that somewhere in middle you do have clock phase is high and then it goes low and it goes it goes high here right and it goes high.

So whenever these are low you ensure that your so this is X and Y two clocks then you ensure that Y goes only high when between the phase difference between the 2 when the clock goes low right and this we have already designed it in a previous example of previous slide right what we do now is we will just discuss.

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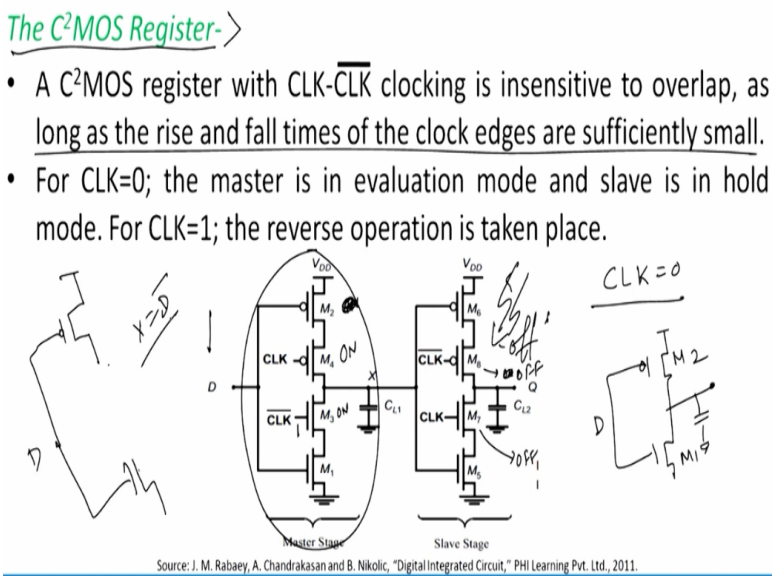

So we have now discussed therefore that clock overlap is an issue so as along as you are not able to design a very good clock you will always facing a problem with 00 and 11 overlap fine and this will result in obviously bad data to be evaluated in the output side to remove it people thought and came with an idea what is known as C2MOS register so we will have a look at C2MOS register this is having a clock and clock bar loading exactly like the previous case.

Right but quite interestingly we will see that even if this overlap between clock and clock bar there is no chance of transparency available to you unlike the previous case okay. Now this is with the condition that which have written here in the slide itself that as long as the lies and fall time of the clock edges at sufficiently small right means if the rising edge and the falling edge of the clock is relatively fast that means the rise time and fall times are very small then only this register will work fine we will see as you move along.

Let us look at the fact when clock = 0 let us suppose right when clock = 0 then you see M2 will be on state right clock 0 means M2 will be on state your M4 will be also on right M3 sorry yes clock equals to 0 implies that clock bar = 1 and therefore M3 will be on right and this will be on. So this will be on which means that you end up having a effective circuitry of M2 and then M1 this is D and this is M1 and this is M2 why it like this because both M3 and M4 are in on state so whenever clock equals to 0 M3 and M4 are on state and therefore the first part which is the master stage is in the evaluating mode.

But in the same instance of your slave is basically the off state right the reason being that when your clock = 0 M7 is off right and M8 is basically your is on right for clock 0 so clock bar 1 so this will be also off I am sorry so clock = 0 primarily meaning that m7 will be on and clock = 0 primarily meaning clock bar will be equals to 1 which means M8 = on which means that if you look at the equivalent circuit equivalent diagram for this one this will be a open circuit right this will be D and this will be whole this will be open here and then you will have M5 sorry M5 available at this auricular point M5 will be available. So this whole thing will be open here right.

Why it will be open because you M8 andM7 are on so a slave stage will be basically on open or off and evaluation stage will be open and therefore whatever the value of D is there you will get X = D bar right is it okay now let us look at the fact when your when X = clock = 1. When clock = 1 then M4 is off and M3 is off but M8 and M7 both are on and therefore your slave starts to evaluate right and the master is in the off state now maser has not evaluate.

So whatever the latest value of X was there will now be available to Q so Q will be equals to X bar so ideally since X = D bar therefore this will be also equals to D so whatever the ideal value of D was available to you will be available to you at this stage at this stage here right. Now let us look at the fact that why does this C2MOS register is not basically a clock overlap sensitive means even if there is a clock overlap you will never get a direct path between input and output.

That was see that was problem in the previous case and under the condition when your overlap you have direct path of available between input and output what I am trying to tell you is that even there is an overlap here I would not expect to see for direct transition between input and output just to appreciate that point or to get back the particular point let me show you how this is possible.

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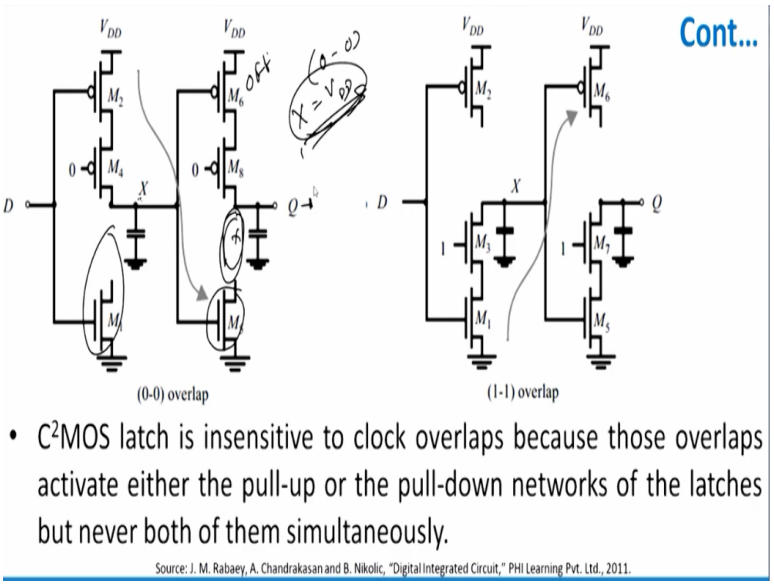

(refer time: 17:15) Let us look at the point when you have a 00 overlap let us suppose was 00 overlap. 00 overlap is basically means that your M4 will be on right but M5 will be off under the 00 overlap condition M5 will be off as a result if your D = 0 right in any case M1 will be cutoff but M2 will be on and this VDD will charge X so X will start to go up am I clear I will explain once again what I am trying to say.

What i am trying to say here is that let us suppose you do have a 00 overlap right so clock = 0 clock bar is also = 0 so when clock = 0 M4 is on your NMOS will be off because it is given clock bar so it will be off once this is off the pull down which is this part is not looking properly and what happens to pull up if D = 0 then M2 will be on and VDD will appear at X and therefore X will equal to VDD. When this =VDD this will move forward this will move and since you have the 00 overlap your pull down network here also cut off your NMOS will also cut off.

How did you get cut off because you just look at this point at this point if you put 0 here M7 will be off state when you put 00 cut off so what happens is that under 00 overlap M3 and M7 go in the off state at 00 overlap if this is true what I am trying to say then even if X = D bar whatever it will be D or D bar it will be in fact it will be exactly equals to VDD because there is no D here VDD primarily means that this will switch on M5 and switch off M6 which means that even if this switch on since there is no driver transistor here Q will be actually holding it original and there is no path for the Q to discharge also.

So Q will be holding the original state available to it so even if there is 00 overlap with you can sure that the data at Q will be storing it is value provided there are no leakage paths available for the data to vanish right either through sub threshold leakage or through direct leakage it is through sub threshold leakage you have it but even for direct leakage you can expect then not to overlap.

So this also 0 0 overlap let us look at 11 overlap and see how the critical aspect of 11 overlap work if there would have been 11 overlap just the reverse would have happen that in that case M4 and M8 right both are at off state right so even whatever the value of D is say D = 1 let us suppose if this will be pulling down M1 and M3 is = 1 because clock = 1 then this X goes to 0 right as X goes to 0 it pulls M6 to VDD but as it pulls though it node goes to VDD but your Q is never attached to it node and therefore Q holds the state previous state whichever the state you cross fine.

So under the condition of 00 overlap or a 11 overlap you are still not able to have the transparency between D and Q right and this was reason that both pull up network and pull down network do not work simultaneously right they will always work complementary with respect to each and that is the reason why do it. however there is one small issue which I should point you at this stage.

That let us suppose by some problem or some means your X as actually = let us suppose X was actually = 1 let us suppose right so if it is 1 then when D goes to 1 so there will be a if 1 this would have been 1 so M5 will also on and there might be finite chance that the Q can actually go to ground this is quite critical in 11 overlap condition so let us be very clear about it before we start explaining of understanding it the idea here is that whenever you let us suppose by some means that initial value at suppose let us equal to 1 right X was equal to 1 I put D = 0.

So D = 0 means the M1 will be off no problem but D = 1 M2 will be off D = 1 primarily implies M1 to be in on state right so I have a path for X to go to ground and therefore X will either will go to 0 so 1 to 0 transition it will take place but please understand at the same very same instant of the clock as gone when there is a overlap M5 is already in on state right M5 is already in on state which means that Q has already gone to 0 even before my data pulls my M1 and X to

ground my M5 becoming on by virtue of X = 1 as pulled the node Q to ground and therefore Q goes to ground.

So irrespective of value of Q is storing here Q is always = 0 but this can be avoided provided you make this path delay much smaller than compared to this path delay between these two path or between sorry this path. So try to make this path delay relatively less as compared to this so by the time this tries to go to 0 X is already gone to 0 then the cutting of M5 so M5 will be on off state right.

So 00 is quiet easy and simple to understand and it is quite easy to evaluate also but 11 overlap will have certain issues is related to it and that issue have pointed Q out here in this case here. So understand please these are all non-ratioed logics here which means that the W/L ratio ratioed at least for 00 overlap has got no implication over the low to high or high to low transition or even a setup time violations.

So with this we have understood what is C2MOS shift register and how it works out in general how does it work out right and that is we have understood in this slide we have also understood that it is basically a non-ratiod logic because in any case whatever the value of gate voltage our threshold voltage is less than threshold voltage that will switch of the transistor and that will be no direct path from VDD to output or from ground to output at any point of time well that is more clear at 00 at 11 it is not clear because it is 11 you will have repeated fight M3 M1 pair and M5 M7 pair right in this slide which will try to make the value of Q go either to ground or X to the ground right.

One thing which I should point out at this stage is that there are certain issues are chances even when the gate voltage is less than threshold voltage you might have the threshold current which might make you X node go slightly lower than what we expected to be. So X was = VDD this might actually ending having 0.7 VDD 70% of VDD is available to you because there will be sub threshold so it is always advisable to refresh it every time you do it right and this refreshment time is quite critical in understanding the total speed of operation of sequential logic.

So we have understood 00 overlap we have also understood 11 overlap let me come to what we known as dual edge trigger till what we were doing we were either sampling the data at the rising

edge of the clock or it is falling edge of the clock and the rising edge of the clock then we define is to be the positive edge design at the falling edge of the clock it is defined as the negative edge trigger design right.

So let us look at so therefore you see your sampling approximately in the sense that 1 clock cycle your sampling will be 1 right because for pull up once and the pull down once which means that the speed relatively is low right.

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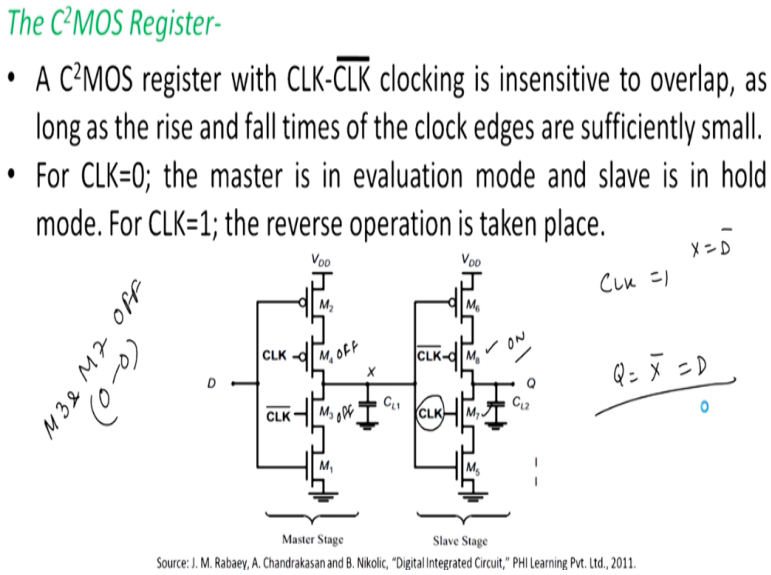

In this case but if I do a dual edge register which will be discussing now which you see in front of you this is basically a dual edge register this is basically a dual edge of the register then it sample the data on both the edges with so both the edges of the clock so it samples the data at the rising edge of the clock it samples the data at the rising edge of the clock it also samples the at the falling edge of the clock.

So therefore this is also known as a dual edge trigger design or dual edge trigger design register the advantage of this is at every low clock frequency right very low clock frequency if you do a dual edge trigger right you increase the speed slightly to a larger extent and you power dissipation levels are not increase the drastically beyond the particular point right. And as a result

so power dissipation are low without compromising on functional though put up the resistors which means that whatever through put is expected from the system.

You will always get it but my power dissipation will be low and the reason to power dissipation is low is that you are operating an relatively sole low frequency that you do not worry about dynamic power dissipation on. Now it consist of two parallel registers which is this one and this one so these are two parallel registers which is this one and this one so these are two parallel registers and this two parallel registers are basically multiplex by a tri-state driver here.

So this is my tri-state driver 1 this M4 and M1 is common M2 is replaced by M10 both right and that how it is works out will see how it works out now when we discuss the power edge trigger dual edge trigger design we have therefore understood what is now a what is what is basically a your previous let me recapitulate what we did today we just add a look at 00 and 11 overlap issues we had looked into what is known as C2MOS register and how it works how is it insensitive to overlap such long as there is a rise time and fall time relatively smaller as compared to the clock edges.

We have also seen what is the concept of clock overlap why is it overlap and this is apply to a simple dynamic transmission gate logic design and we have seen in C2MOS logic that you have to make the pull up and pull down transparent of each other they should not know they should be transparent of each other means they should be opec of each other chance when the pull up is all pull down is switched on vice versa we have also seen to remove it we do it we do a C2MOS logic latch and therefore it is insensitive to variation in the values available to you and then we will also discussing the dual edge trigger shift register right so we will do that in the next module as we discuss ah in the next module for dual edge trigger register right thank you very much.