CMOS Digital VLSI Design
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Module No # 06
Lecture No # 27
Sequential Logic Design – III

Hello welcome again to the NPTEL online certification on CMOS VLSI digital design. We will starting the sequential logic design module three today and we have already seen the various differential of sequential logic. How is it different from combinational? And now we will be entering into the basic fundamental principal of sequential logic. So let us to get first of all the basic bi-stability principal because this from where we start the whole issues.

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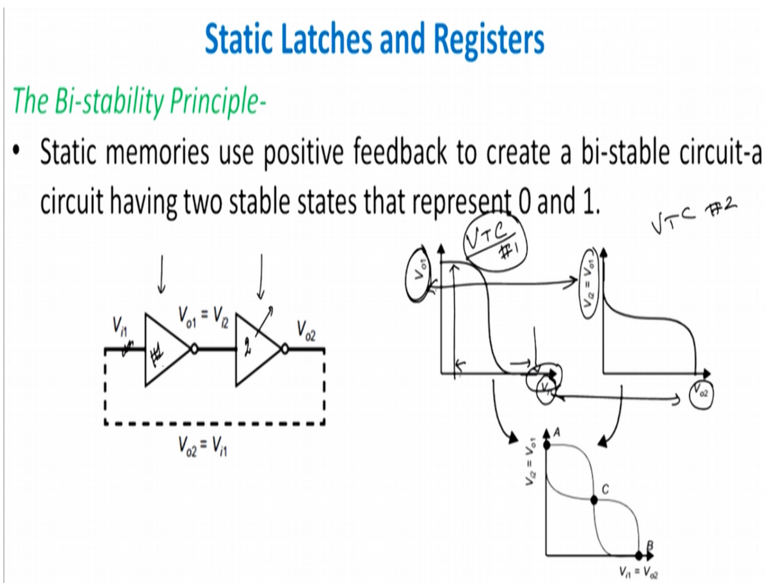

So let us suppose we got two inverters static inverter CMOS inventers and they are cascaded in this manner as you can see in the figure they are cascaded in such a manner that the output say this is the number 1 and this is number 2 then the output of 1 this is Vo1 is exactly equals to Vi2 which is the input of second one.

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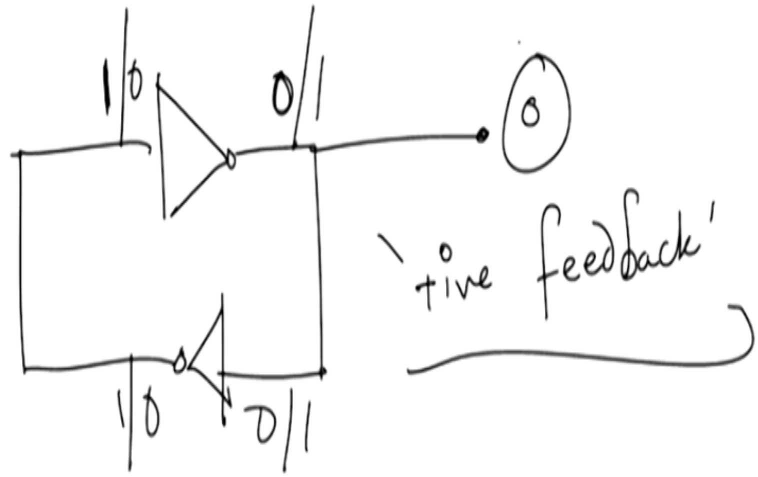

And the output of second one actually equals to the input of first one right so it is sort of a cross coupled sort of a inverter or simple inverter where they are you added this and this right you have got 1, 0 it will be 0, 1 and therefore if you are able to write a data here as 1 and this is the 0 you can actually obtain 0 here like this and it will remain there forever until and unless you change this to 0 and then this will become 1 and then this will be 1 and this will be again 0 so this is known as positive feedback regeneration loop.

So I have a positive feedback loop here this positive feedback loop helps me in storing this data for large amount of time right. So most of principal in sequential logic it based on fact that you are able to do a positive feedback and you are able to store the data for longer period of time this is what the basic principal is all about.

So let us have look into the fact that if you have two inputs which is so if we have one input Vi in 1 then there are transfer voltage transfer characteristics VTC for one inverter which is this 1 is basically number 1 and this is VTC for number 2. So if you look at VTC for number 1 it is basically V input by V output so VTC is voltage transfer characteristics which plots output voltage with respective to the input voltage right.

So and the X axis you have got Vi1 which is the input voltage right and on the Y axis your Vo1 which is basically output voltage. So you can seen here Vin is low V out is high when V in is low V out is high and when V in is high V out is low so it be as an inverter which is already we have done that quite often. But the best part of it is now is that the second inverters input will be first inverters output.

So what I do is so what basically Vo1 right is basically Vi2 am I correct Vi2 is input for this one. So if I have got input on my Y axis this is what I am writing Vi2 equals to V01 and therefore outputs is equals to Vo2 right and this Vo2 is exactly equals to Vi1 which you seen here so these two are equal right. Whereas Vo1 and Vi2 which is these two are equal right now if I look very closely and if you want to have a look into it all the closely let us look what happen?

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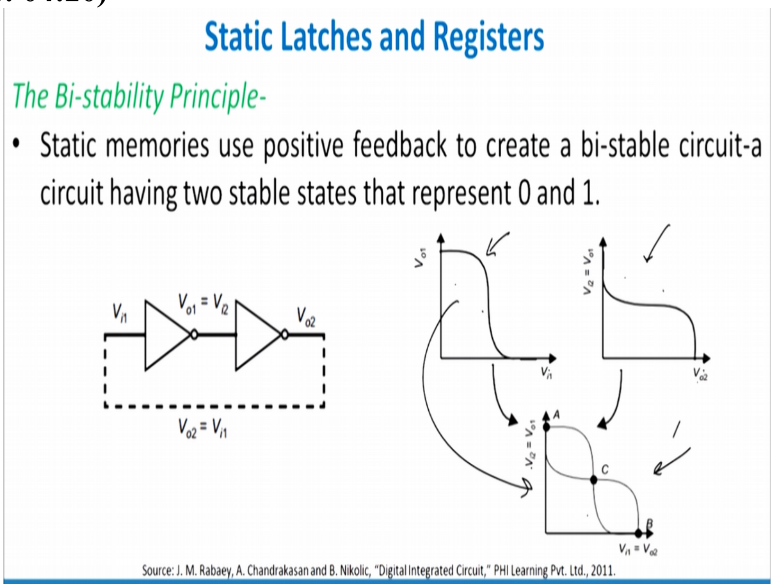

If I just take this and this together means this plot and this plot if I take it together then i get plot which is something like this and why this like that because if you look very closely you are if you take this and plot it here I get Vo2 from the X axis and i get this curve exactly like what I get then if I take this curve in this axis since Vi1 = Vi2 Vo2 therefore I can simply place this over to this one right and as a result you will have three intersection points between the two curves. If you have I will explain try to explanation you via another network or via another loops I have got two inverters in cascade.

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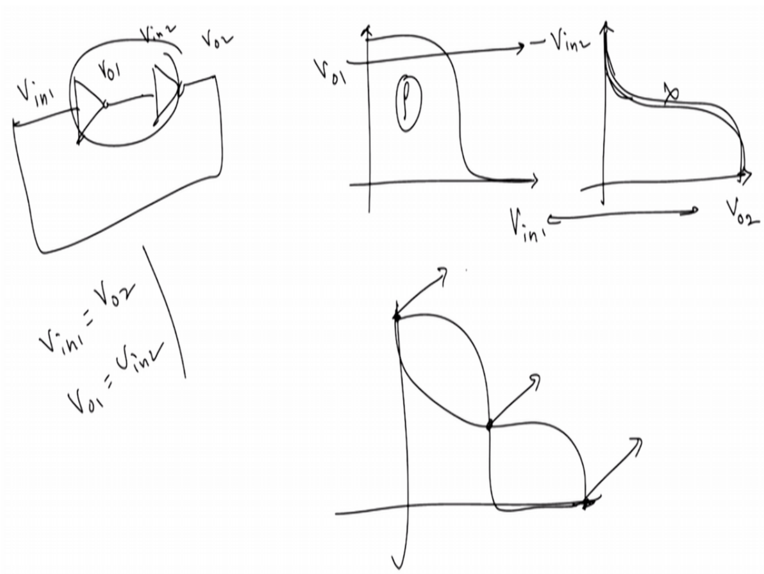

So if I have got the first one which is here let me draw for you so I have this so this is Vin1 this is Vo1 and this is Vin2 and this is Vo2 right and we have got a feedback loop so I get Vin1 = Vo2 and Vo1 = Vin2 fine these two are always there see if I plot here Vin1 versus Vo1i get a curve which is something like this. Then if I plot a curve of Vo2 here output versus input which is Vin2 right I will get a curve which is something like this right this is what I am saying right.

So you get something like this obviously now since this two are equal and these two are equal I can simply take up this one and place this over the first one which is this one and what I get here is basically one I get like this and the other I will get like this and therefore there are three points where there to cut and these are the three points where the both the voltage will be equal and therefore these are the three points where the where this network will operator it.

It cannot operator it any other voltage node only at this node and this node let me term it as A, B and C I do not let me see how it termed as okay it is A, B and C right out of this three nodes two are stable nodes and the third node is unstable node right i will explain to you how it works out. Let us look node C, node C if you look very carefully you will see that if you look at node C if you give a small change in the input right let me say I give a small so it will be easier to explain you here.

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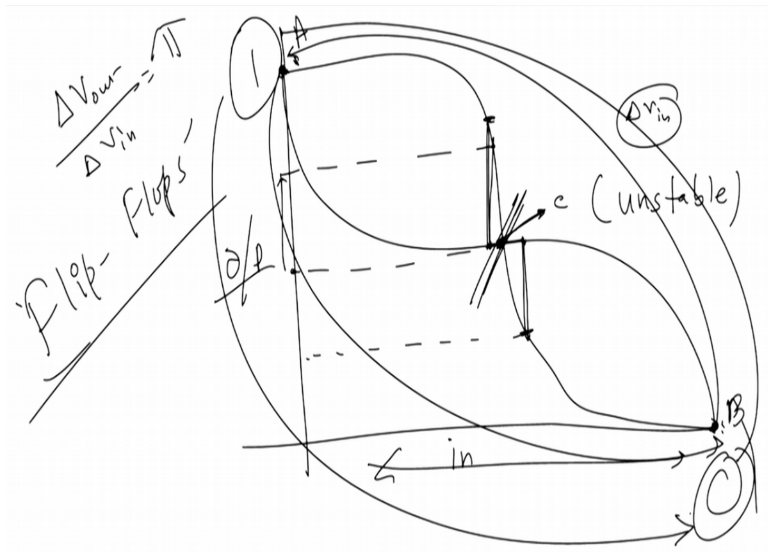

So let me now let me draw into the bigger fashion so I am drawing it like this right and the it goes like this lets come like this I have got another one approximately like this it comes okay. So a one point here another point here another point here this is my let us input and this is my output. So you see if in this case if I even if I am biasing my device here at this point which is C and even if I give a small change delta Vin right then this will initially output was here.

Now your output will be somewhere here or even if we go to right if you give a small change here lets us suppose till this much point your output will changing such a larger value. So this is your new value of output if you are in the if you are going in the lower Vin direction this will be output if you are going in the higher Vin direction this will be your output.

It either of the two cases the output I shifted from this point to this point just by even a small change of delta V which means that del V out by del Vin is very large which means that if you are biasing device here it sort of access in amplifier and a small change at any one of the locations input location will result in a very large change in output and therefore C point is really at unstable point.

This highly unstable point because stability will come only into the picture when for the small change in Vin you have still a maybe if not smaller at least equal change in Vout. So your gain will be approximately equals to 1 right but in this case if you look at point number C you end up having a higher in stability there and therefore this C point is unstable because a small change in input here will give you a large change the output voltage here right same thing happens in this side as well as in this side.

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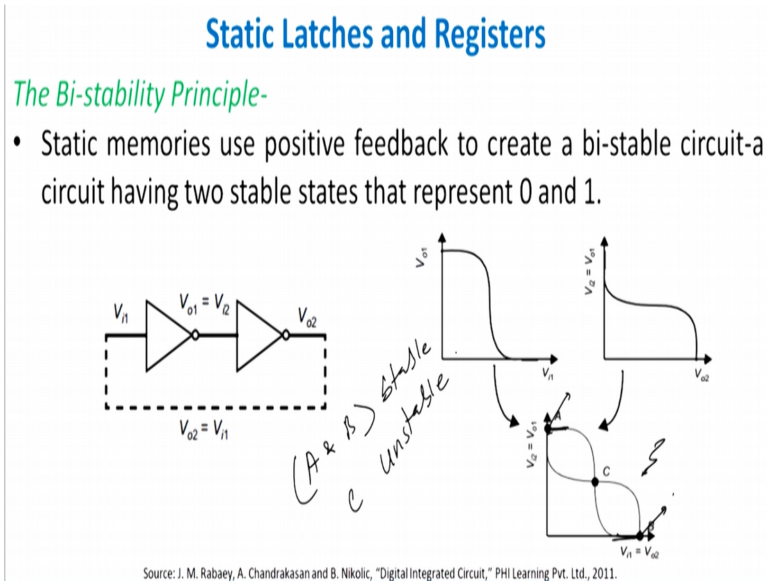

So this is both side you see a large chance and as a result become unstable but let look at the point number A or at B fine and let see how what is our influence our overall picture. Let us suppose I have biased devices at point at A right and then I am giving a small change in the input side you see that if you look at for example if you look the curve now here even if you do a small change in the input which is this one let us suppose right your output will not change drastically.

Because this almost a flat curve here similarly it is almost a flat curve here so even if you change by a small amount you will actually not see a large change in the output and therefore point A and point B are stable point. So A and B are two stable points right and point number C is basically an unstable point therefore if you want to bias this into a system I need not bias at point C only need the bias point A and B right. Point A is where input is low output is high point B where input is high output is low so that was I am talking about.

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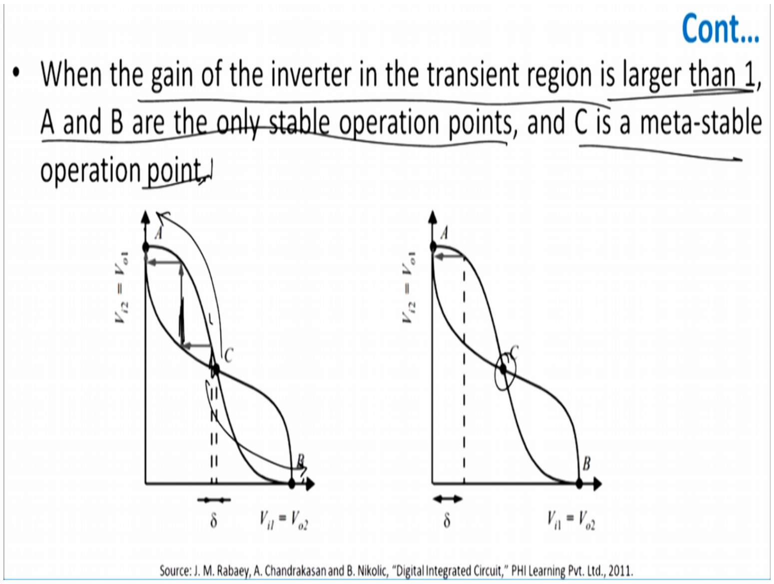

When the gain of the inverter in the transient region which is C is larger than 1 A and B are the only stable operating points and C is a meta-stable or unstable operation point which is see right as I was discussing with you a small change in C will show a change in V out. Similarly a small change in here will result in larger value of V out here right. And therefore any change will drag this either to A or this to B.

If the differential gain in the transient region is larger than a then if the devices is operated at point number C and if this small change in the input it will either drag into A or to B with the two stable states if the input is low it will drag into A if the input is high it will drag into point number B right. And therefore A and B are the only stable operation point C is the unstable point as I discussed with you just.

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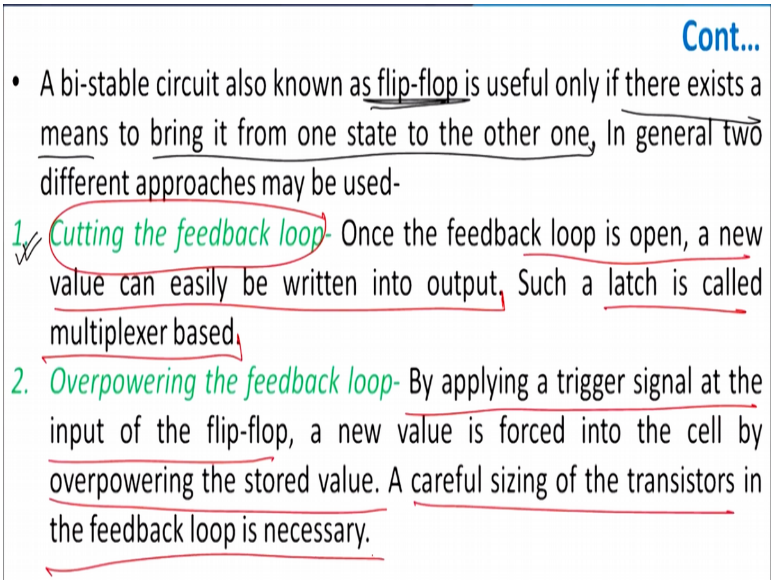

Now therefore a bi-stable circuit is also referred to as flip-flop right why it is known as flip-flop because since there are two stable state let us suppose A and B then by proper application of voltage i can switch between point B to A or from A to B without going to point number C is this concept conceptually clear that therefore we refer to this as flip-flops.

They refer to as flip-flop why? Because you are flipping a data from either 1 to 0 or 0 to 1 by application of potential right and that is what it is written here there therefore that exist or means to bring so is useful only if there exists a means to bring it from one state to another to one. Which means that from bringing (()) (12:43) another one I require to give a potential change where I am able to do that I am very happy with that.

Two thing which you should be very carefully about therefore that if you want to bring one state to another state both the states there are two ways of bringing back from one state to another one is that you cut the feedback loop right since it is the positive feedback once you cut the feedback loop you can easily change the input because see the feedback loop is helping you to stabilize point A and B that is what we have discussed just now.

So the output for second inverters was feeding into the input of the first one so if I am able to cut off that basic this one basic. So if I am able to cut off this let us say I am able to cut off this part right I am able to cut it off then I get easily write a new value of Vin1 here so I get (()) (13:46) a new value here. So this methodologies is actually refer to as cutting the feedback loop the first cutting the feedback loop this is the one which you see.

So once the feedback loop is open, a new value can be easily written on to the output. Such a latch is called multiplexer based latch so all your multiplex mugs based latches will have there feedback loop open and I can write from external source or either output or the input of the latch. The second thing is by apply a triggering signal by what we generally do by apply a triggering signal at the input of the flip-flop new value can be forced into the cell by overpowering the store value.

But the problem here is which means that suppose you are storing a 1 which is basically say 1 volt and I want to convert into 0 so I have to do something by which is 1 volt goes to 0 right. So I have to overpower it so what does it mean that I have to apply current or a voltage which is larger than that or I have to sink that voltage or current to 0 then only I will be able to sustain a change right. So therefore it is very important that do a careful sizing of the transistors in the feedback loop.

So let us suppose I need 0 I want to force into change to 1 it primarily means that my feedback loop should be strong in enough to override that 0 by an external source. And therefore you have to should be very carefully in sizing the transistor or W/L value of the transistor evaluation of transistors. So I did two methods of in design a flip-flop the one is which caring a feedback loop right so one is carrying the feedback loop straight forward we are doing it and it is also mugs based design which we are doing it and once you gut the feedback loop we can do anything you want to do at the input side and change the values from 1 to 0 or 0 to 1.

Then second is over powering the feedback loop means that I do not touch the feedback loop but I do have substance which is able to overwrite the feedback and I am able to change the state of A and B by doing certain changes in the input voltage available to you okay. So this is the overall scheme which I wanted to do just put to you in front of you. So let us look at the first case which is basically the mugs based latch.

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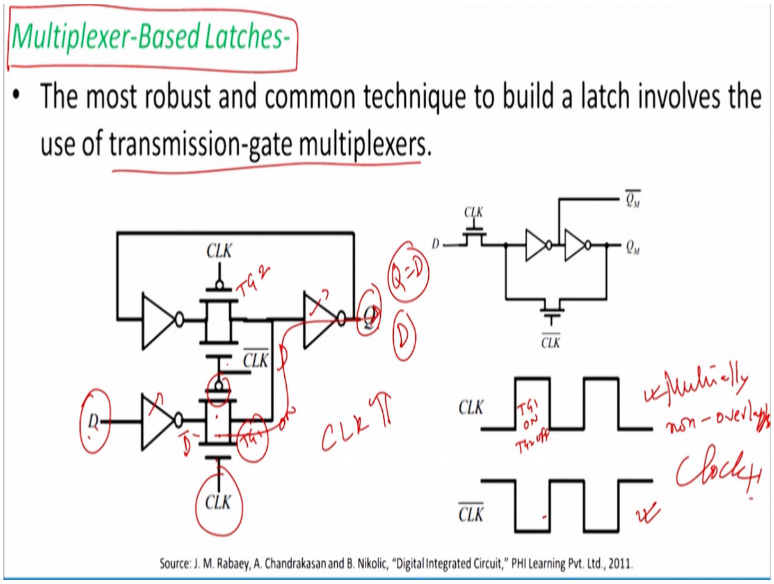

So this is basically a multiplexer based latches. So this is multiplexer based latches which will be stating currently and we are going the most robust technique which has been used and it used for they are actually using transmission gate and we also use an NMOS to past transistor logic. We have already understood what is the transmission gate? Transmission gate remember if you remember a previous discussions.

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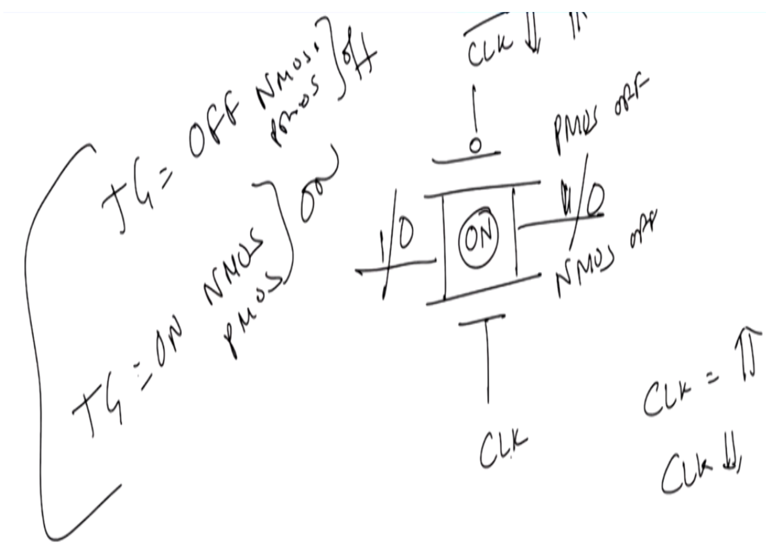

I just to remind you right transmission gate was primarily something like this that you had a PMOS. And you had an NMOS in parallel to each other and if you give a clock here you generally give clock bar here or vice versa which means that the clock is let us suppose high right and the clock bar is low and therefore this transmission gate is ON when clock is low clock bar is high PMOS is OFF NMOS is also OFF so the transmission gate is OFF. So TG will be OFF right when both NMOS and PMOS are OFF and TG transmission gate will be On.

When both NMOS and PMOS are ON fine so this is the current scenario which people has been using it. So depending on the clock state I will be able to either switch ON the TG or switch OFF the TG unlike in past transistor logic this one is a very good transmitter both 1 and 0. So if I have a input here output here so I will 1 so I will get actual 1 here if I was 0 I will actually get 0 here depending on the clock cycle right.

So let me come to this transmission gate multiplexer and show to you what is the transmission gate multiplexer is all about. So if you look here hmm this is have a D right this is basically a D right and this output Q so this is my data in and this is my output and I have clock here and therefore it is (()) (18:05) clock bar here and since this is clock bar i have a clock available at this particular point here right.

Now let see what happens if so this is the clock and therefore this clock bar then this is also known as a mutually non-overlapping clocks so this is mutually non overlapping clock. Now let us see what happens when clock goes high so the clock goes high let us suppose i name it as TG1 and let us name it as TG2 when the clock was high then clock bar goes low and therefore TG1 is ON so when clock goes high and clock bar goes low TG1 is ON agreed.

But so therefore so clock goes low TG2 is OFF agreed why TG2 is OFF? Because this is basically connected to the NMOS clock is anyway high. Which means that PMOS is off clock bar is low NMOS is OFF so this whole thing is OFF therefore this is OFF. So what we have does is D does a D bar here D bar comes here and D bar of bar is D. So Q = D is appearing in the output side since this feedback loop is cut clear understand since the feedback loop is cut whatever D is here Q is available here which certain delay by delay given by two inverter delay by 1 TG delay transmission get delay I am an clear?

So let me explain once again and I will explain once again to just make you clear those who are doubt in this areas have. I have two clocks 1 is clock and another is clock bar then mutually therefore non overlapping if they are mutually non overlapping then when clock goes high right when clock high then TG1 becomes ON why? The clock goes high why because NMOS gets ON and this PMOS gets ON both gets ON this becomes high but let us took at TG2. TG2 clock bar goes high clock bar sorry clock bar goes sorry clock was high so clock bar is equal to 0 and therefore this NMOS is OFF and this is also PMOS and therefore PMOS also because clock is high.

So TG2 is OFF and therefore TG1 is ON and therefore it transfer into D, D becomes D bar here D bar transmitted here and through this close to Q fine. So whatever your therefore your latch your system is basically transparent which means that it allows the voltage at point D to go to point Q this is conceptually clear now at the point when your clock bar is high so we go to this state.

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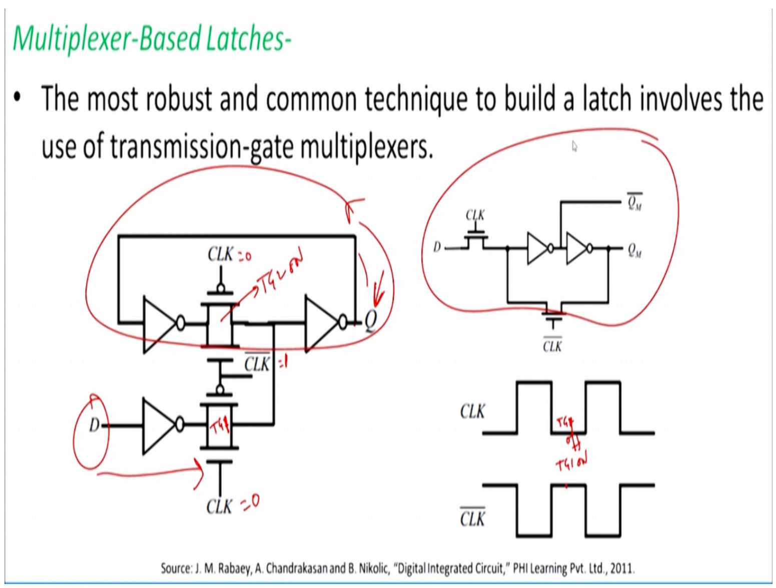

When you clock bar is high right then clock is low so this is 0 this is 1 and this is 0 so which is 0 so TG2 is not cut OFF so TG2 so in this case TG2 is OFF but TG1 is ON it is ON. So if this is OFF it does not sample any data from D data from D is not sample by TG2 so this blocks the TG and therefore it is basically trying to block the input cycle but by switching ON sorry this is TG1 by switching ON by TG1 so by switching on TG2 ON I have made this loop non activated therefore the last value of data which was stored in Q just before the set up time will actually will be rotating there will be a feedback loop available to you and you will be storing the data here at Q till the next clock cycle comes into the picture am I clear?

So the idea here is that if you have a mugs based system it actually known as mug based system then depending on the state of TG1 and TG2 transmission gates I get either transmit D to Q and that is basically a transparent mode or if I do not want to do that I can store it in Q for infinitely long duration of time at least the time for the next clock to the arrive right and then new value of D will come into the picture and you will automatically get value of the D available to you right.

So that was the reason I told to you this is basically TG based we can also have a NMOS logic based design which is front of you which this one right so this is NMOS of logic design which you see this is the NMOS logic design.

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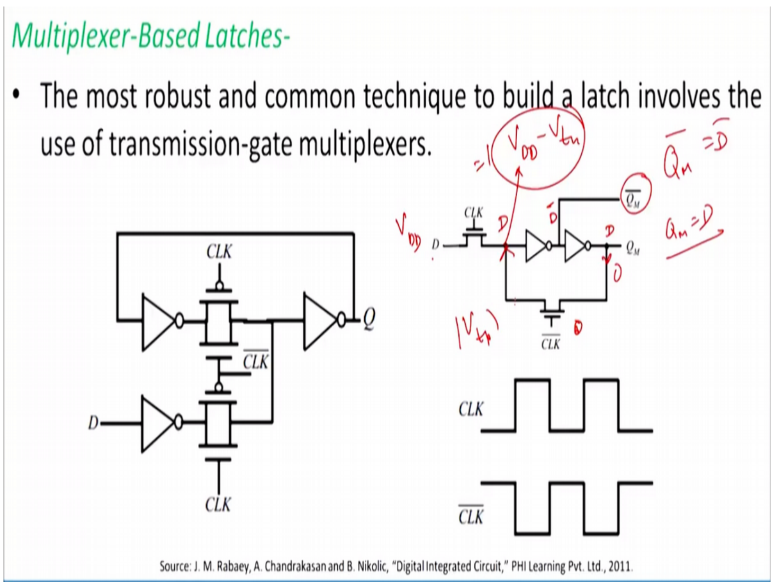

And if you look here so D will appear as D here not D will appear D bar here. So therefore I get QM bar from here and D bar will appear as D and therefore QM = D right QM bar = D bar but this D is because when the clock is high your clock bar is low when no means this is ON therefore D will actually help you to do a positive feedback loop right and you are able to sustain the same diagram here.

But let us see what is a problem in such scenarios? The problem in such a scenario is when you remember when I was discussing with you the NMOS logic NMOS or PMOS for example NMOS is not a very good transmitter one means if I get a VD here which equals to 1 I will achieve here VDD - VTH in threshold voltage of the device where VTN is the threshold of the device.

So you will have voltage level falling similarly a PMOS is not a good transmitter of 0 and there will be so if this is 0 here there will be mode of VTP appearing at this particular point. Which means that if you use an NMOS logic there will be signal degradation in the output side in case of NMOS or 1 will appear as 1 -VTN and for a PMOS it will appear as mode of VTP a 0 appearing as mode of VTP.

So whenever 0 is passing through an NMOS no problem or if 1 is passing through PMOS no problem. But if 0 is passing through a PMOS I will automatically get a mode VTP change as well as if 1 is passing through a NMOS I will get of VTN shift in the value of voltage in the output side. So signal degradation or signal integrity comes into picture when you have mugs based latches with NMOS past transistor logic right and that is what that is why we generate to do not like do it or we do not have like to have such a design available to us.

One more thing which I might include is a okay it in this i will discuss maybe in next time next idea but we have understood the mugs based latches or the multiplexer let me come to the we have done therefore the latch based design we will now come to what is known as H trigged one and therefore.

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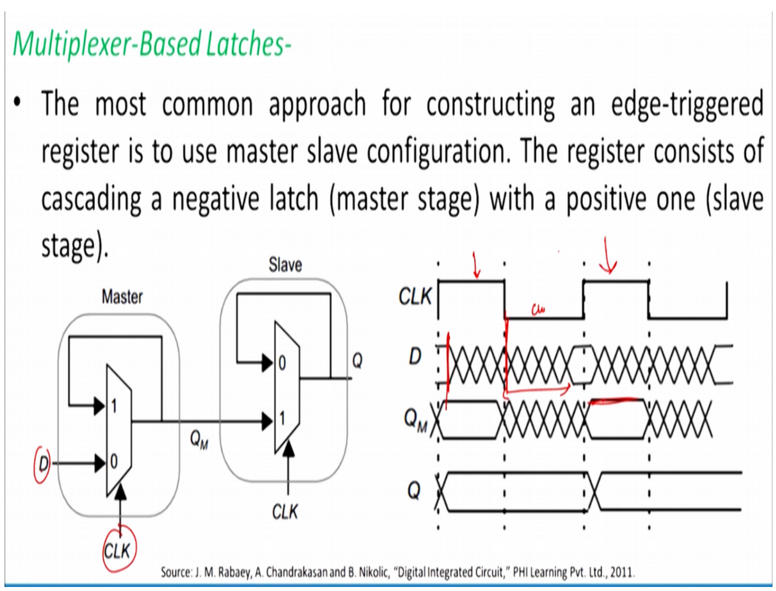

Let us suppose I have got what is now master slave configuration of H trigger register so it is basically master slave it is very simple and straight forward. What does it do that for that the master excepts the data right as it excepts the data if the slave is transparent when the slave will produce the data in the output side depending on the value of data available in its input. If you do not want the output to come out just switch off the slave and the master will evaluate only the value of input to the output. At a particular instant of time if you want to again evaluate it open the slave transparent and shifts to Q.

So D to Q delay will be available to you in this case right now if you look at the first case which is basically the master part if you look here when the clock in this case you are giving clock low so what happening is that in this case when the clock is high right let us suppose you have the data you shifting in the whole time as been met at this point and then you move to this much of point because the positive H trigger design right.

Then QM will follow whenever the clock is low when the clock is low and this D will be 0 and therefore you will follow the system has the clock become high when the clock goes high then the data will stable at QM right and even if the data is rotating it is hence stable when clock equals to high right. So we have therefore we will discuss this part in the later section but we were actually understood what is mugs based latch available to us.

And how i can design a mug based latch using there are many configuration will see but primarily this configuration we will be concentrating on which is master slave latch and then see how we can approach the other latches in detail manner fine ok thank you very much.