CMOS Digital VLSI Design
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Module No # 05
Lecture No # 21
Combinational Logic Design- X

Welcome to the NPTEL online certification course on CMOS digital VLSI design let us start from where we left earlier. We were looking at the various problem areas of dynamic CMOS logic and the third problem we will be facing is basically known as capacitive coupling problem.

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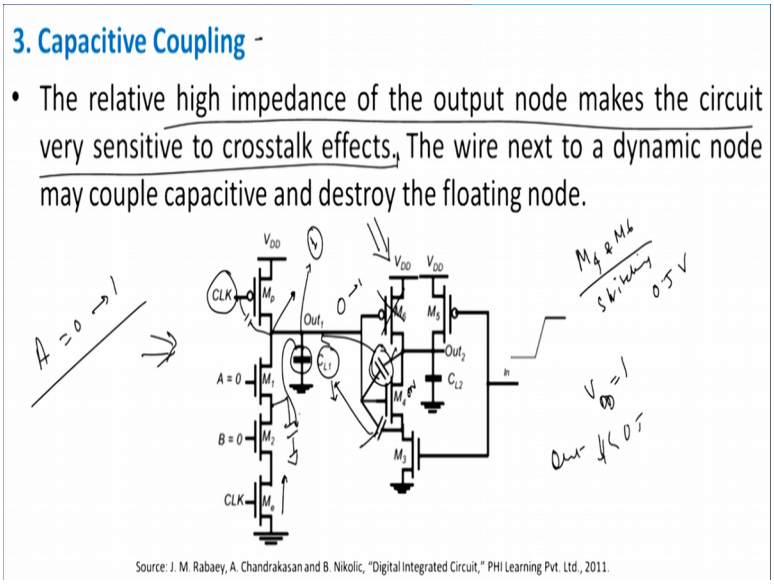

So the capacitive coupling problem which is denoted here we can see so the problem which we face was that your output impedance right as I discussed with you in the previous turn that output impedance is in the static CMOS logic is either CMOS connected to VDD or to ground it is never kept in floating node whereas in this case during the evaluation mode night have chance at which your output node might be a floating node right it would not be a low impedance available to you.

Which therefore makes it prone to large amount of crosstalk noise and therefore this is what is written here that relatively high impedance of the output node makes the circuit very sensitive to cross talk effect right. In fact if you are driving for example logic here by a dynamic logic which

is kept here even a small change here for example if this let us suppose the switching threshold of M4 and M6 the switching threshold of this one is let us say some let us say 0.5 and you are using a VDD of 1 volt is it okay.

And the out here actually out 1 let us suppose it falls downs to less than 0.5 volts then what will it will do is that it is this M6 and M4 will see a voltage here as interpretative 0 rather than equals to 1. This is the first problem the second problem is if you look at M4 and M6 M4 will have Cgd here which is this one and therefore this Cgd will add up with this CL1 and therefore the overall capacitive loading will also be large.

You please understand therefore that if there is a capacitive loading between the slot at the PMOS and the output which I discussed with you I might discuss with you in the next turn when we do clock feed through but you might have a case where you will have this clock at the pre-charge PMOS talking with you output here right. And therefore if this CL1 gets added up with this capacitance here and here the clock as to actually drive a heavy load right and therefore the lock power actually becomes very large.

Apart from the dynamic power dissipation of the system your clock also gets loaded so clock factor of the clock loading also increases drastically. So what we are trying to look therefore is that let us suppose you have entered into evolution phase and clock equals to high right but A = 0 and B = 0 so this out will actually hold it its value equal to 1 here right. If it is 1 it will actually switch of M6 right but it will switch on M4 right and as I switch is on M4 they will be heavy capacitive loading on CL1 and CL2 right.

So you might ask me that therefore even if this is happening sine CL is not getting charged does not matter whether it is getting charged or not very true but then if this is a finite probability that A goes from 0 to 1 you still have the no discharge so let us suppose A goes from 0 to 1 right then the charge which was located here will now be shared between this and this. So there will be charge sharing phenomena taking place here will come to that later on.

Which means that if during the evaluation phase right your pull down network is not activated even if it part of it is activated you might have a small chance that the charge accumulated at the loading capacitance might be reduce due to charge sharing mechanism and it might effect your

overall mechanism of the thing. With this knowledge let me come to the forth problem of dynamic logic and that is basically clock feed through problem as I discussed with you in the previous in the previous turn let us.

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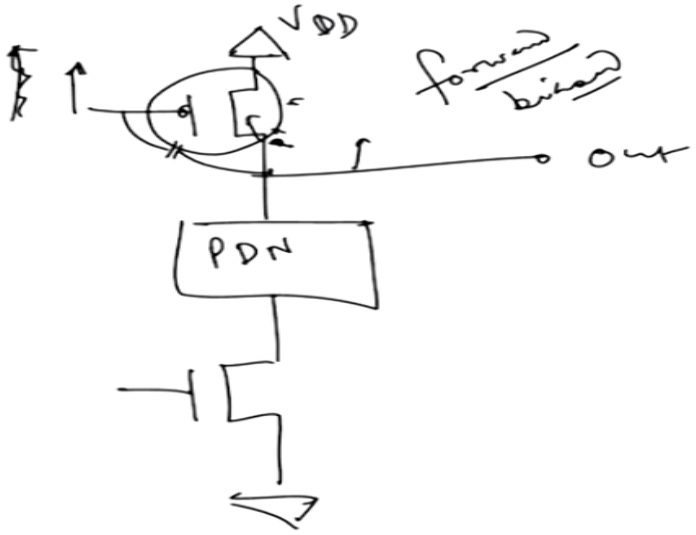

Let us suppose I have a I have a clock feed through I will explain to you clock feed through so I have PMOS here I have PDN I have PDN here and then I have a NMOS which is there which is basically my evaluation this is my pre-charge case and this is basically the VDD we have just connected here and this is the output which you see. Now if you look very closely here this is basically a PMOS so basically a PMOS.

So PMOS primarily means I have a n type substrate I have a p typed source p type drain p type source in this case so if you look very carefully if a clock goes high right ideally if you if the clock is not going high it is typically at low stage it is relatively low. So let us suppose something happens here right those are if this is capacitive coupling between this point and this point here the voltage here will also shoot up right and as a result there might be a scenario where this p+n region gets forward biased.

And this is this is quite dangerous in terms of operation so whenever you have this this phenomena is not clock feed through so when clock which is given to PMOS gate actually the capacitive coupling with the output side you might end up having the reversed bias PN junction of PMOS actually converting into a forward biased pn junction and therefore the large current

actually starts to flow you getting my point? Which means that though you did not want the PMOS to switch on you still have a finite probability that the PMOS switched on that period of time. So that is what we are talking about when we discussed here.

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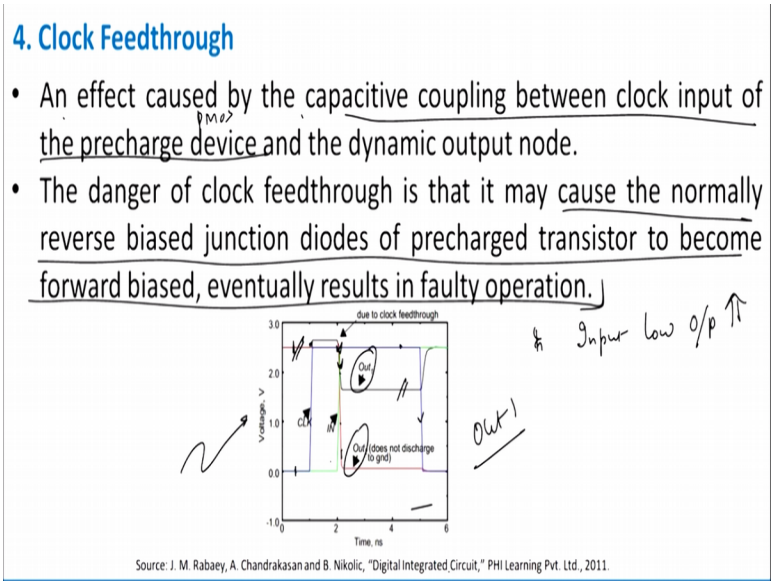

So the an effect which is by the capacitive coupling between the clock input of the pre-charge device is what the PMOS and the dynamic output node as I discussed with you just now that the problem is that normally reverse bias junction diodes to the pre-charge transistors will become forward bias and therefore there will be a problem in the operation.

To show you that look at this figure which is in front of you if you look at this figure this is time versus voltage the blue the violet of the blue curve is basically clock the green is basically input and you have got two output out 1 and out 2 which is then I will explain to you what these are and this is primarily because of clock feed now let us look at when the clock goes when you have evaluation phase when you have evaluation clock is low and output your output is basically high right.

So which is perfectly fine as far as understanding of dynamic logic concentered but when you input is input you're your clock input is low is low right your output is basically high and this is what you are getting here as the clock starts to rise you will have a push in the voltage here. So the voltage goes straightly higher then the VDD value right and because of clock feed through it

goes like high. It remains high till the clock remains high and then the clock starts and then the input starts rise the output will start to fall.

Because let us suppose A and B are both high and you have a AND gate available to you then when A and B are both high the pull down network switch is on evaluation your evaluation phase an then the output voltage starts to fall down and therefore that is what is happening here the output one starts to fall down right and this is what is happening here forget about this black curve will discuss that later on but look at the red one right.

The red one actually does not even fall to 0 why does not fall to 0 the reason being that you did not but some of the charges initially will lost by virtue of charge sharing or even by some other mean. So you had some decay of charge initially which you cannot recover and therefore the voltage does not actually go to 0 voltage in any of the situation. So now you see what is out 1 out 1 primarily the voltage at the output of node 1 which is discussed with you earlier and it even does not cross the value it does not even cross the value of 0 out 1 will which means that the out 1 is the value of voltage when you clock is basically going to high.

So your clock is still remaining high you see this blue curve which you see in front of you the clock is high right the clock is high primarily meaning output should be actually falling down depending on the input. So let us suppose your input was not was not high in that case the output will be going down to below value. So it should ideally latch to value = VDD it does not it falls to value = out = 1 out 1.

So even under the criteria that you're a and B are both equals to 1 and you are designing a NAND gate output value of the voltage will not go down to 0 but slightly above 0 as I discussed with you now this the first scenario observation the second observation is that when your output is held at 1 and your inputs are actually given as 0, 0 or 0, 1 or 1, 0 in either of the three cases the pull down network is not getting activated and therefore ideally I should go to VDD in reality no and therefore outfalls to out 1 which is slightly less than VDD right.

So these are the two full scenario's available to you as far as this clock feed through is concerned right.

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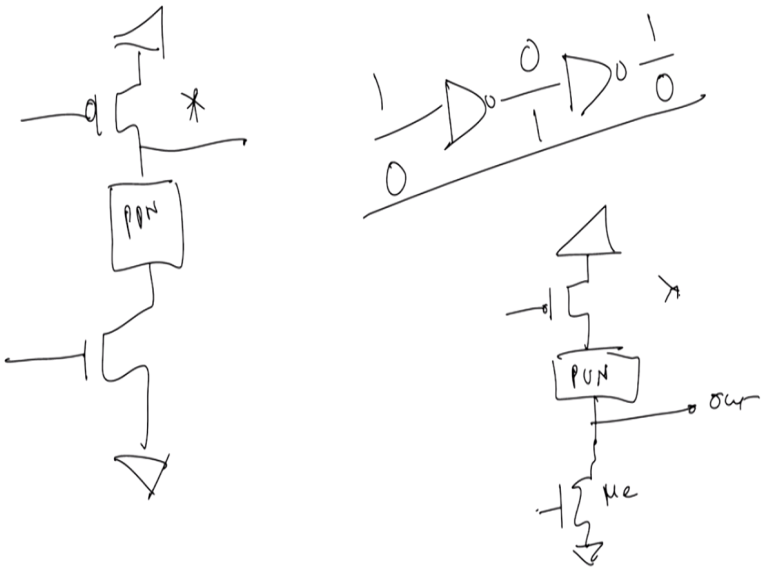

Another thing which I should include here before I move forward is quite interesting part and people have been doing it quite often is that I just now discuss with you that we are using a PDN right we are using a PDN here and then I have got a PMOS here and this is this right and this is this fine I think it is clear to you and sorry this and then this and then this is it.

The another concept is that see if I can simply make it something like this that I have a PMOS here I also have a PU pull up network and then I take output from here and then I have got the evaluation transistor just check it out that this will also work for me exactly in the same manner as this is working these two are exactly the same right. So this is basically using NMOS logic we are trying to find out the dynamic logic and you can also use a pull up network to do but preferable we do the first one which is using NMOS logic.

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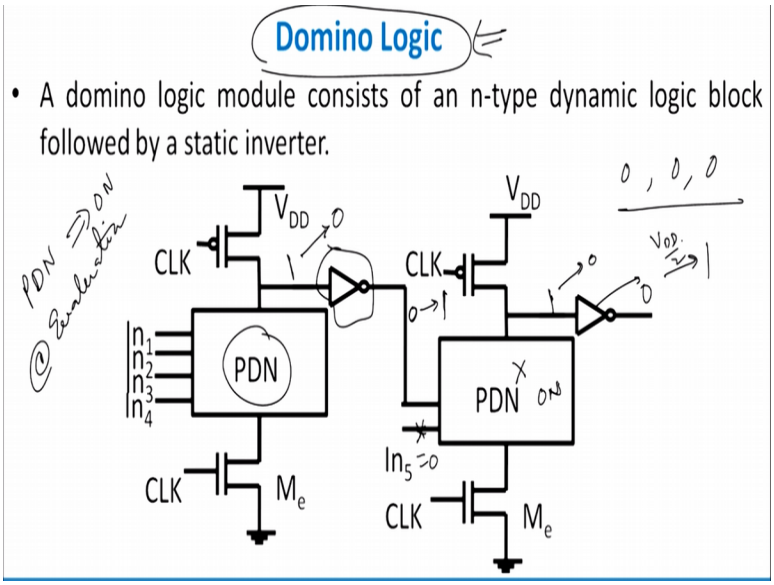

Let me come to the domino logic here domino logic is basically what at N type logic block. So n type means you are making the PD and NMOSFET that means you are not touching the PMOSFET you can get P type when you have PUN on the pull up network with the Boolean expression. So the Boolean expression is PDN here so we have one input we have one PDN network here and it is basically connected to a static CMOS here.

So I have a dynamic logic here and it is cascading to a static CMOS logic at this stage right and that is what it is known as domino logic and I will explain to you what why it is known as domino we can explain we can explain to you later on but let me explain to you basic thing. Let us suppose your clock was going to 0 so into pre-charge phase output goes to 1 right out goes to 1 this goes to 0 if this goes to 0 the PDN is cut off let us suppose.

Because let me suppose there are no input so input 0 is 0 and it is goes to 0 PDN is 0 primarily means that again this is 1 this is 0 again this is 1 this is 0. So all the output of my domino logics are all in 0 state fine now let me do one thing that let me say that my In1,In2.In3 and In4 are such that in evaluation phase that my PDN is on at evaluation. So when my PDN is on in evaluation this one goes to 0 and therefore 0 goes to 1 as this 0 goes to 1 suppose PDN goes on as I goes on 1 goes to 0 and therefore again 0 goes to 1.

So you see not about domino basically you remember is basically small domino's small cubical structures which are kept in line if you just push one of them it is basically a cascading effect and

it pushes other in a row right that is known as domino effect same domino effect happens here that is the reason it is known as the domino logic that you have a static inverter which converts it to a high logic..

See the advantage here a static inverter output impedance is typically very low and therefore noise immunity is much better in domino logic as compared to anybody else right fine not only that since it is the static inverter it is noise margins also very symmetric and high.

So NML NMH for this case will be approximately equals to VDD / 2 approximately if you are assume it to be ideal NMOS device and PMO device and CMOS transistors typically VDD / 2 is the typical sort of NML NMH which you get so the noise margins are typically very high and as a result you will have a lower signal higher signal to noise ratio will be available to you. So this was basically the domino logic diagram which I showed to you so this is basically a PMOS NMOS followed by a static inverter.

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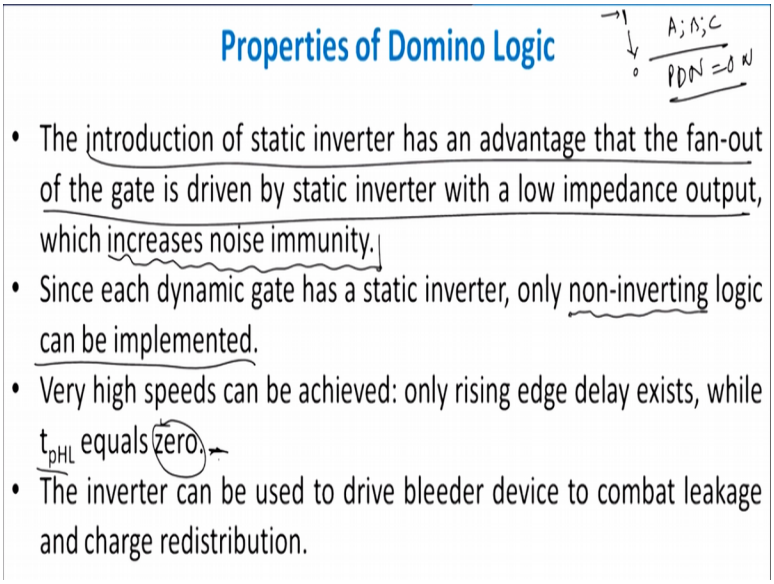

So as I was discussing with you the introduction of static inverter as an advantage that the fan out to the gate it static inverter which is basically at low impedance node and therefore increases the noise immunity. So that is known as important issues as got there but you see the problem area the problem area is since each of the dynamic logic is cascaded with a inverter the output of the inverter again is primarily a inverting mode.

So you have you will have a only you will have non inverting mode can be implemented you can always put another CMOS inverter to be inverted very high speed and the reason of the high speed is because the output load effective sees only two devices or three devices a the output node whereas in an inverter static inverter it sees all the transistors TGD so on and hence so forth. So it is very high speed which you see right interesting property here is that tpHL actually = 0 right what is tpHL?

It is basically high to low delay which you see right now high to tpHL can only occur provided output to be held at 1 and then you go from 1 to 0 but 1 to 0 can only happen in evaluation mode and that too in condition that A the inputs are such favorable that the PDN is on or the pull down network is ON right under these tow conditions you will have 1 to 0 transition right.

So if this is not happening your tpHL high to low will be always = 0 right so that i what I am trying to say that you will have a always equals to 0 here. So these are the few properties of dominos CMOS logic one way to solve this non inverting problem of domino logic is a that you solve it by re organizing the logic using simple Boolean transformation.

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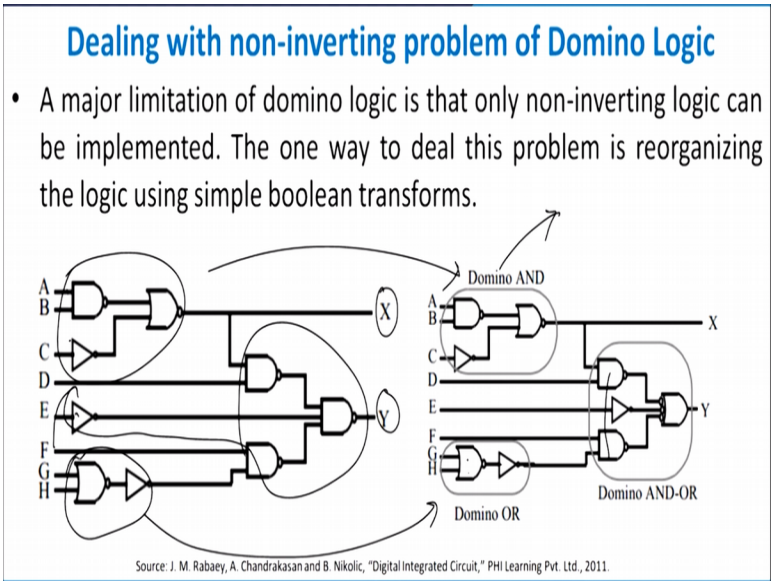

For example let us suppose you have this big circuitry with convergence fan out coming here and final value is X and Y where X can be given by A, B, C and you Y will be function of all A, B, C, D, E, F, G and H right now this whole thing this E sorry yes this this is basically a domino logic I

can therefore convert this into a domino logic I can take this and this together and have to domino logic and domino and domino AND OR operation.

So this is basically AND- OR which is basically AND operation right and this is domino AND operation because this is an NAND forward by a gate we have a domino AND operation because you have a AND gate available here and therefore you can convert a simple logic which is given by this into a domino logic and you can still forward together right so though we do not use too much of domino logic.

Now a days the problem in comes of problems of cascading another way of doing is that we have already discussed this point earlier it is basically DCVSL logic we have already done DCVSL where what we do is that we take the design and it is complementary design then we ran a positive feedback network in order the achieve the output results available to you.

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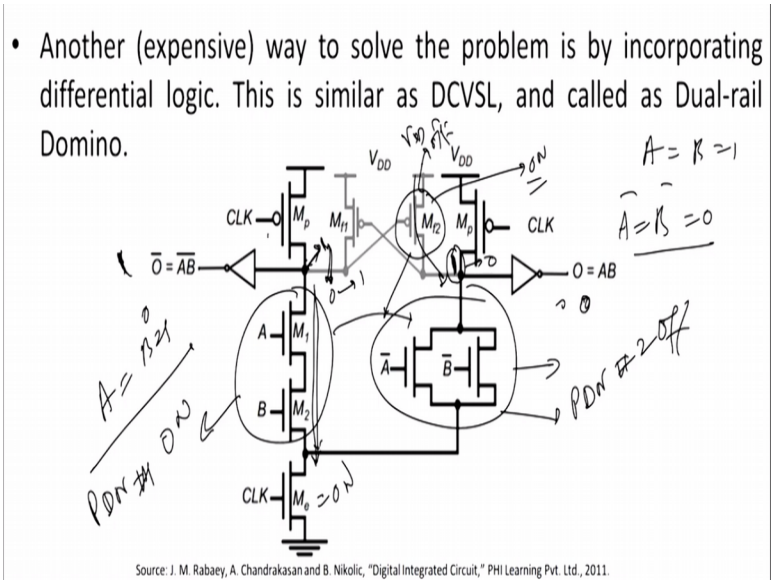

So if you see here for example in this slide you will see that A and B are in series here that primarily means that A and B will be parallel to A complement and B complement will be in parallel to each other. So when you are into pre-charge phase clock = 0 Mp switches on this goes to high primarily meaning that this feedback will be switched off so this will be switched off right this will be switched off clock goes high this is also equals to 1 right this is also equals to 1 so both are equals to 1 here it is holding its state at 0 , 0 input is 0 output is also 0.

Now when the evaluation phase depending on the value so let us suppose A and B are both equal to 1 this so this will not happen nothing will happen here nothing will happen in this case but this will actually pull down the value of the voltage from 1 to 0 here and it pull down M2 starts to get on right Mf2 starts to get on and therefore this 1 will do up so you see when both A and B are equals to 1 right then A complement B complement = 0 this primarily means that your this PDN PDN2 right is off state.

Whereas PDN1 is basically an ON state when this is ON state it tries to pull the transistor or the voltage here back to the ground because my clock is 1 Me is ON and therefore I have direct path between this to the ground and therefore it falls down 1 as it starts to fall down to 1 and it crosses the mode value or the threshold value of Mf2 where Mf2 is this turn then this switches ON right and therefore this VDD which is kept here will try to charge up this node.

So even if this node actually has some delay or some leakages will be actually compensated by this VDD actually trying to pull up this value. So this pulls to full of so this becomes equal to 0 and this basically equals to 0 to 1 so this becomes 1 here So 1 here and I have a 0 here right in the next phase when you go to pre-charge again the same thing happens that you are able to sustain this to again to 1 and this again goes to goes to 0 again is it okay?

So this is a this is an why I say is it is an expensive proposition because when you use the DCVSL will actually end up having larger area so the advantage which you got out of domino logic you are actually losing in terms of this DCVSL right but the idea is typical very good where you use a dual voltage supply here differential output to be available to you right. So this is one thing which you should know so let me end up this dynamic logic course with what is known as the Mp CMOS.

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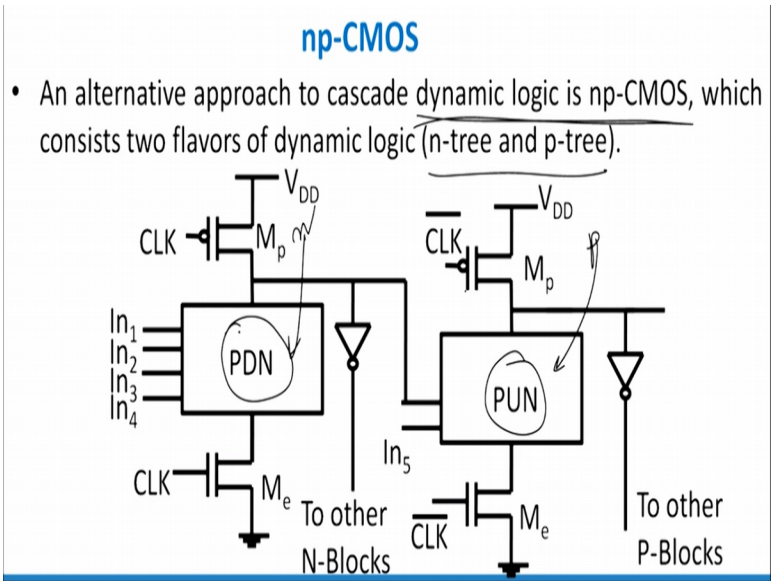

So what I told you was that I can therefore replace the PDN by having a PUN and this is basically cascading n-tree with p-tree. So if I have a NMOS here NMOS based PDN right and I have a PMOS in pull up network and if I simply cascade this to together then I get what is known as dynamic logic or np CMOS logic so this is basically np why? Because this is an n this is p because this is made up of PMOS this is made up of NMOS right and you will have dynamic np logic available to you.

It has got a lot of advantage but generally PMOS is are not used np logic is not used in np CMOS logic is not used in because PMOS is mobility is typically very small so the delay is relatively very large in case of PMOS right and therefore though your NMOS will have a smaller delay but you will face a problem of latency when you come to second figure which is this PUN figure right and there will be a problem in terms of latency or the signal as to wait since certain period of time in order to do some job right and that is the problem area of a np logic.

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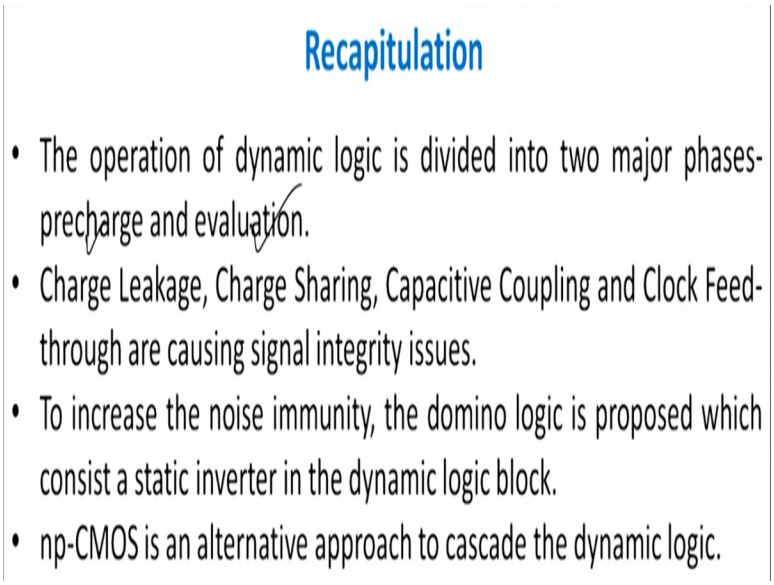

With these definitions understanding let me recapitulate what we have learnt in dynamic logic so this till today what we have learnt is will finish of our dynamic understanding of fully combination logic from next time onwards we will start with sequential as well as logical efforts as I discussed with you dynamic logic is divided into 2 phases one is known as pre-charge another is known as evaluation.

Pre-charge is one when the clock is low and our PMOS is switches on and therefore the output node is charged by VDD to 1 what is the evaluation force the evaluation phrase is when clock goes to 1 your pull down transistor Me which is evaluation in NMOS transistor switches on and depending on the values of A, B, C, D the input I can have either a 1 to 0 transition or output node switches to a floating to a low impedance node and it holds the value of 1 there.

We do a problem of four things specially in terms of signal integrity issues charge leakages, charge sharing capacitive coupling and clock feed through. So these are the four basic problem areas of this thing in all the four cases there is drop in the voltage of the output which results in a in a smaller value of voltage in my output as I discussed with you to increase the noise immunity of the domino logic is proposed which consist of a static inverter and dynamic so I was static and a dynamic both of them are cascaded to form a domino logic.

Finally we were saw an np CMOS logic where my pull up network was basically by PMOS and pull down network is primarily because of NMOS right so this this is what you have learnt till

now as far as combinational logical blocks is concerned and we have learned various aspects of combinational logical block and next time onwards we will start with either sequential logical block and we will see how it works out fine right with these words I thank you all for a patient hearing and thanks a lot thank you.