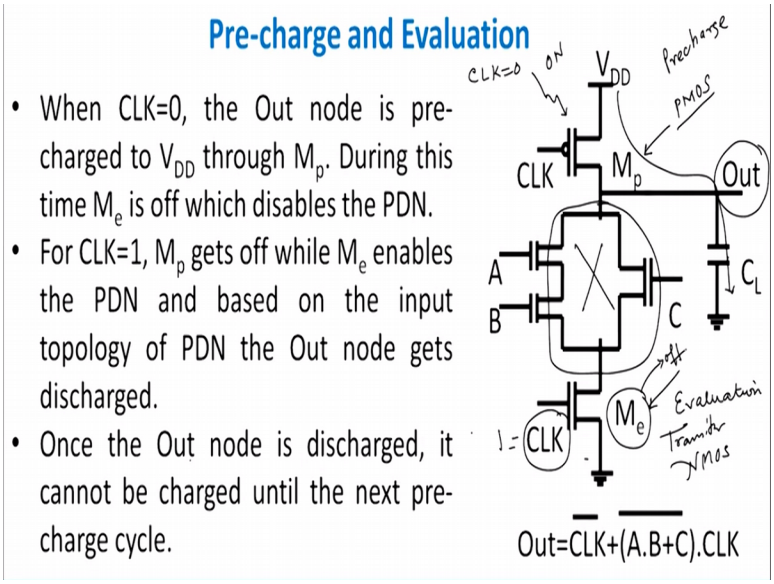
**CMOS Digital VLSI Design**
**Prof. Sudeb Dasgupta**
**Department of Electronics and Communication Engineering**
**Indian Institute of Technology – Roorkee**

**Module No # 04**
**Lecture No # 20**
**Combinational Logic Design- IX**

Hello everybody welcome to the NPTEL online certification course on CMOS digital VLSI design and we will be looking at combinational logic design part 9 we will be having a look today let us see how it what we have done till now. So I will just recapitulate what we had done earlier. We had finished off with static CMOS logic wherein we were looking at the fact that whenever you have the complementary sort of MOS available to you then depending on primary inputs give to the pull down network or pull up network your logic behavior is settled right and it is evaluated in the output side.

What do you have been doing for the last turn as been that we have been looking into what is known as dynamic logic and the name dynamic logic is because it is clock dependent logic and we will see how it works.

**(Refer Slide Time: 01:23)**




We have seen in the previous discussions if you look at the this basic CMOS architecture here which is available in front of you if you look basic CMOS architecture then this part which you see is you CMOS basic part right which is basically realizing the CMOC logic right. So it is

exactly like the pull down network of the static CMOS logic right so the difference between dynamic and static is that or the similarity between the two is that the pull down network is exactly the same for the dynamic logic as well as static logic.

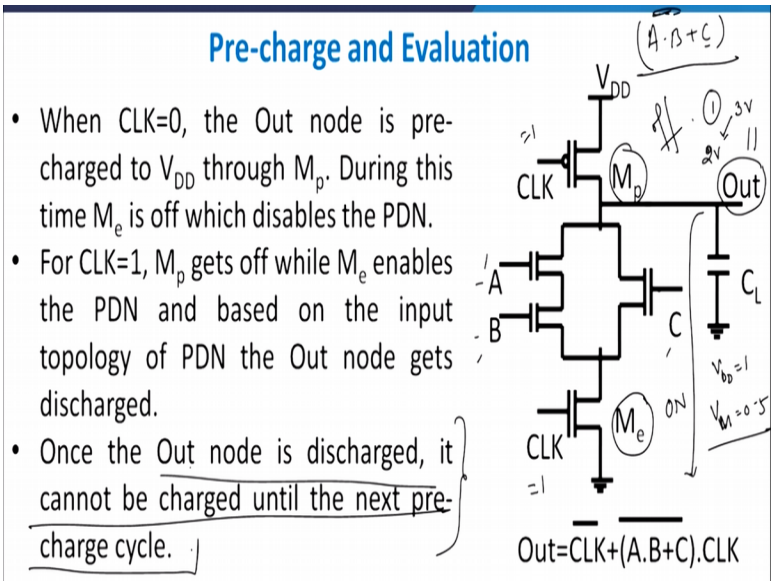
What the differences? We have already seen has been that we have got two transistors Mp which is here and we have another transistor Me here this Me is known as Mp is basically a PMOS transistor and it is basically a PMOS right and it is also known as and it is known as evaluation transistor and it is basically and an NMOS device which is available to you. Now if you look thoroughly into this when clock goes to 0 then this PMOS switches on.

When clock equals to 0 right your this PMOS is ON right and when this is ON this clock is 0 implies that this will be off which means that Me will be off right when Me is off and Mp is ON your V out starts to charge from VDD through this CL and the CL will charge to the maximum value which is equal to VDD. So this phase is known as pre-charge phase so we have two phases here first phase is known as pre-charge in pre-charge phase irrespective of the inputs which you are giving which means that irrespective of the values of A,B or C value at output will be always equals to 1.

So in the pre-charge phase there will be always a 0 to 1 transition in the output side provided earlier 0 was stored at output node. So if earlier 0 was at output node in the pre-charge phase what will happen is that when the clock is switching on the PMOS VDD will charge CL to input and out will go to VDD and therefore out will do a 0 to 1 transition fine I hope this is clear to you what does clock at the evaluation transistor to do?

It actually tries to disable to pull down network right why because when a clock is high your Me is switching off so irrespective of the values of A, B or C your out node is actually disrupted from your ground node right so therefore there is question of output node getting discharge to ground this is for the so this this whole process is basically your pre-charge process or pre-charge phase. Let us look at the next phase when the assume that the clock = 1 so when clock = 1 just the reverse thing happens and what does it what does it happen is something like this.

**(Refer Slide Time: 05:00)**




When clock = 1 right this Me becomes on right and then when clock = 1 then Mp becomes off when this becomes off depending now this is important depending on the values of A, B and C the output node can actually go to ground right.

So if your a so if it is A dot B this is Rc if anyone of them is high right if C is high and A and R A and B both are high then only output will actually go to ground provided Me = 1 or the clock = 1 which is in the your Me which is the pull down transistor is getting 1 which is therefore which is very important that they have to understand that the 0 1 to 0 transition in the pull down network can only happen is basically a conditional condition approach which means that it depends upon the values of A, B and C whether the output node at all will actually pull down to ground or not this is the second thing.

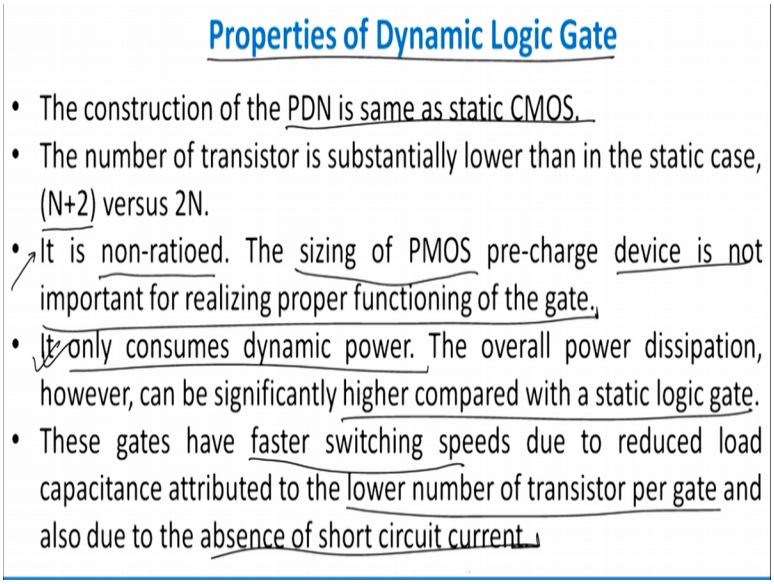
Third thing is please be very careful when the voltage lost at the output node is lost forever right because it has to wait till the next pre-charge cycle for the output voltage to go to VDD. So if you have got some VDD right some output voltage at this particular node at this output node suppose you have you are suppose to node 3 volt right and by some problem some means or other this is come down to 2 volts then we cannot recover this extra 1 volt until and unless you go from evaluation to pre- charge phase.

So the problem is dynamic logic is that your logic might be lost so what I am trying to tell you is let us suppose your output voltage starts to fall down by some reason or other and it goes below

0.5 let us suppose by some means or others then the output will be read as the actually as 0 rather than 1 right and that bigs the logic just go different and therefore we are not able to understand the concept of logic in this case.

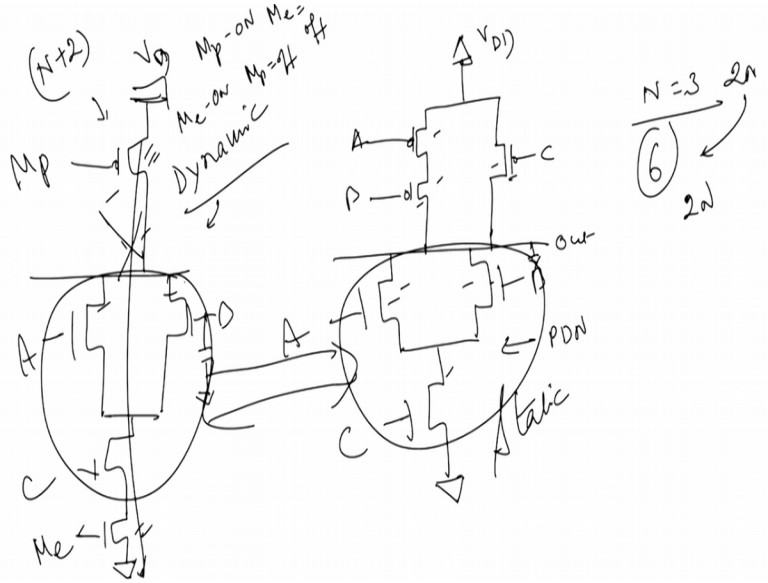
So that is the point I am writing in the third part here please look at the third part here that once the out note is discharged it cannot be charged until the next pre-charge cycle arrives. So whenever the next pre-charge cycle arrives you will not be able to do it.

**(Refer Slide Time: 07:47)**




So this is this is the dynamic logic in front of you as I discuss with you what are the what are the properties of what are the properties of dynamic logic gate the first property is that it is of course I have discussed with you just not. It is construction of PDN is same that of static CMOS right it is exactly the same.

**(Refer Slide Time: 08:05)**




So if you have a logic Boolean expression A + B right dot C then the pull down network A or B will look something like this right A or B will look something like this and then there will be a C here. So this will be C this is A this is B right so this will realize to you so when you are doing the static CMOS logic you will get something like this ground this is your out.

When do a dynamic logic when you are doing a static logic this will be PDN right this will be the PDN what will be your pull up network. The pull up network will look something like this the pull up network will be that A and B will be obviously in series right and we have as we have discussed earlier A and B and therefore C will be in parallel to both of them right and all will be PMOS in nature.

So this will be C and we discuss this point as = VDD this is the static realization what happens in dynamic? Dynamic will be exactly the same as static the pull down network right sorry pull down network I am sorry you will have pull down network here and therefore it will look exactly the same as the pull down network this is A B and C right A, B and C but the pull up network will be just composed of 1 PMOS right and there will be also 1 pull down evaluation transistor so this is our Me and this is your Mp.

So you see the difference the difference is that you will have this network exactly the same as this network right agreed but what is addition here is basically your PMOS here and then NMOS here which is not there in this network. So what we have done therefore is that we have been able

to therefore make it a dynamic logic therefore the number of transistor which we are using is nothing but for an N input logic for dynamic logic I will be using n+2 transistors.

Whereas for static CMOS logic I was using 2n transistor I can show you from this diagram itself say n was equals to 3 here right because number of primary inputs are 3. If you look at the static dynamic actually this is dynamic right if you look at static you have got 1, 2, 3, 4, 5, 6 transistors right. So it is basically 2n number of transistors which is available to you if you look at dynamic you have 3 + 2 so it is basically n + 2.

So for all dynamic it is n+2 here and for all static it is basically 2n so number of transistors are relatively higher in case of static CMOS as compared to dynamic CMOS. Of course it is as I discussed with you it is non-ratioed logic what is the meaning of non-ratioed logic it is non-ratioed primarily means that the sizing of the PMOS right which is the pre-charge device is not important for realizing the proper function of the circuitry what do I mean by that look at the point number 2 a bullet number 3.

So point number 3 or bullet number 3 if you look you will be very it will be very clear to you that whatever be the W/L ratio of your pull up device which is basically PMOS device I does not matter your still charging the output to VDD. So even if you make the W/L ratio larger you will be having larger current available to you and therefore you will be able to charge the output node faster.

But you will be even if you lower your W/L ratio though your current will be lower but still you will be able charge your output node right. So so therefore this type of logics are known as non-ratioed logic which primarily means that the aspect ratio of the pull up device does not change the functionality of the dynamic logic right.

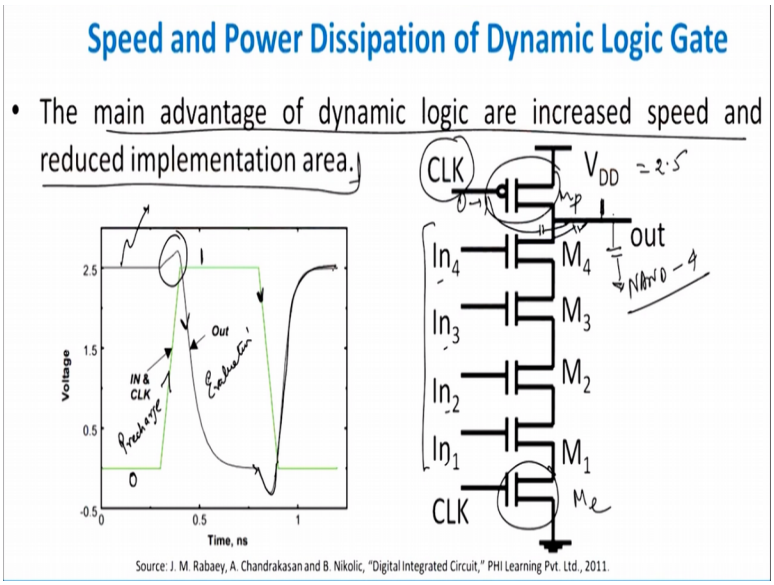
And that is very important as far as the dynamic logic is concerned only which you change is basically time taken for the output node to charge to 1 or form 0 that is what it is very important. As I discussed with you it will only consume dynamic power why it will consume dynamic power let us see why did you consume dynamic power. If you see look at the dynamic here you see if you look very closely at no point of time you do have a static power dissipation.

In dynamic logic at no point of time you have static power dissipation why you will ask me the reason is very simple see when Mp is on right your Mn is off or Me is off and when your Me is on your Mp is off right. So at no point of time you have a direct path between VDD and ground right. So there is no direct path when there is no direct path your static power dissipations are almost 0 right and therefore you only have dynamic power dissipation in this case.

You do not have to any static power dissipation and therefore and but the problem is that dynamic power dissipation can be relatively high as compared to static power dissipation compared to overall power dissipation even it is compared to static logic gate. The last point is at these gates have much larger or faster switching speeds because if you see very clearly that your if you look very carefully the output load is basically here and unlike the previous case the output load actually chase here 1, 2, 3 device where as it here it just sees 1, 2, 3 device.

So I can understand therefore that the load capacitive load which is given to the device is actually slightly lower in case of dynamic logic because it is directly connected to lesser number of transistors which results in a smaller delay or the delay switching speeds as switching speeds are or faster in case and therefore you see that it is a lower number of transistor per gate and also due to the absence of short circuit current. So short circuit current absence will give you a lower power dissipation in static power dissipation lower number transistor per unit gate will give you a faster design or much lower much faster design available to you so it is relatively faster in this case.

**(Refer Slide Time: 14:35)**




As I discussed with you the main advantage of dynamic logic are increased speeds and reduce implementation are right and the implementation is reduced because we have actually reduced the number of PMOS transistor drastically lower you are working with 2n now it is just n+2. So all your PMOS transistor are actually being removed please understand also one important point that if you do not for example when you doing a static CMOS logic if you do not make your pull up network effective W/L ratio 3 times that off the pull down network the you will always get a skewed output and your tpHL will not be equals to tpLH.

We have discussed this point during out earlier studies whereas that is not true in case of domino logic in case of sorry at the dynamic logic right. If you look here this is quite interesting this is basically a 4 input sort of AND gate available here in dynamic so it is basically NAND AND NAND 4 actually NAND 4 so I have got 4 inputs 1, 2, 3, 4 right I have a clock. So this is your evaluation clock Me and this is your pre-charge clock Mp irrespective of the values of n1 to n4 that clock when it is going to 0 output will always stretch to 1.

When your clock is this green color is basically your input clock so when you clock is actually = 0 right the output is latch to 2.5 volt which is equals to VDD if this is 2.5 volts this figures shows me that this is latch to 2.5 volts. As the clock gets up and the input also raises from 0 to 1 the pull down starts to get activated and therefore the output voltage starts to fall so I should expect this to see the output voltage transfer fall and that is what happening here and then it goes to this stage and it it falls down.

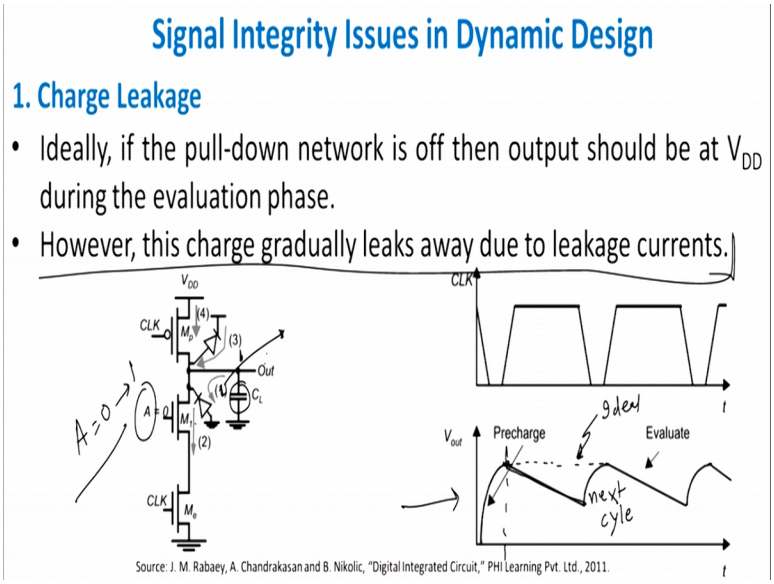
But let us see what happens when the input goes from 0 to 1 this I basically 0 to 1 exactly like in the previous one case your glitch here and the reason being that the output node the CL here right you have CL here what is happening primarily when the input so output was equals to 1 right input clock was equals to 0 but clock goes from 0 to 1 as it goes from 0 to 1 I discuss with you there will be a capacitive coupling I will show it to you just show the thing that there will be capacitive coupling between input and output I have discussed this already previous starts.

But there will be a capacitive coupling between the input which is basically the clock here and the output and as a result the voltage at the output but actually rise beyond VDD and this is what it is happening if you see very closely here it is rising beyond VDD. The reverse is just happening when you go this is this is your pre-charge phase so this is your pre-charge right a when the clock goes high this is my evaluation.

In the evaluation phase therefore when the clock goes down or the input the clock and the input same in this case when the clock on the four inputs go down again the same thing is happened that this will be down linking capacitive with this point and as a result the output voltage might actually swing below 0 volts and then it goes to again VDD when there is pre-charge phase concerned to each other which means that unlike the static PMOS case here the output load capacitance seen lesser number of transistors.

And therefore the over shoot which you see in front of you because of 0 to 1 transition is also lower in this case as compared to any other case right. So this is what we have seen as far as dynamic logic gates are concerned.

**(Refer Slide Time: 18:32)**




Now let me come to the signal integrity issues in a static CMOS logic as compared to a dynamic CMOS logic. Now ideally if your pull down network is off right which means that there is not pull down path available for the output voltage to go to ground then the output voltage should be exactly equals to VDD during the evaluation phase right. So you have pre-charged it output voltage is stored at VDD right now you are giving you an inputs but let us suppose those inputs are favorable to make your path available between the output and the ground then in that scenario what will happen is that the ideally the voltage at the output should be locked at VDD or stored at VDD.

However but this is the ideal case because a please understand the output node is primarily at certain sage of time it is in a bad state I will tell you why? When you want to evaluation phase if it might be true that the output node might not be connected to ground. So please see the difference between a static CMOS logic and dynamic logic in static CMSO logic the output is either connected to the pull up network through pull up network to VDD or through pull down network to ground right.

So the output is either connected to VDD or ground and therefore it is basically it is a your high impedance available to you. What happens in dynamic logic is during low to high transition (()) (20:09) connected to ground but between high to low if one have to do the transition you are not able to do it the reason it is the conditional issue that all the PDN has to be switched on in order to have a 0 to 1 transition or 1 to 0 transition in the output side this is the first thing.

The second thing is I am assuming for the timing that the output voltage will be stored at VDD right in reality you will have some leakages taking place you will have some leakage current taking place through the NMOS and as a result what will happen is that there will be some leakage taking some leakage taking place as a result voltage will start to fall. So you see if you look at the diagram here the pre-charge phase is the voltage goes up goes to approximate = VDD at the age of my pre-charge the voltage held at VDD ideally how it should look like. Ideally it is more transition in the output ideally it should look like something like this.

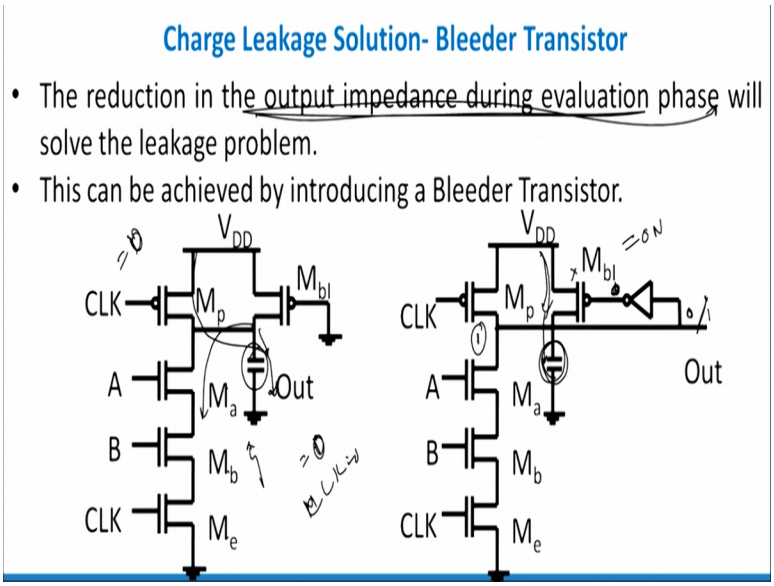
This is the ideal value which you should get right so irrespective of the sort of input the ideal value will lock it to VDD but in reality you might get some charge leakages available which will make the voltage slightly fall down till how much time? Till the next cycle of pre-charge comes right this is the next cycle of pre-charge right. So till the next cycle of pre-charge comes the voltage stops to drop down right and the voltage lost once during any of the phases is actually gone you cannot retrieve it at all from the next phase right.

So that is the major discussion of the problem area of a dynamic CMOS logic which people are responsible or what is responsible you see the first thing which is responsible is this this one current is basically your so this current which you see in front of you is primarily so when so when you will have let us suppose you have one stored here right one stored here and let us suppose A was initially equals to 0 but goes from 0 to 1 then I will if A goes to 0 to 1 then if then there will be direct connectivity between CL of the output node of M1 right.

So that I will tell you is that with such a condition so this is basically NMOS right and this is basically P type this is basically n+ type. So you will have a forward bias diode between the drain junction and the and the MOSFET bulk right now this will be basically a reverse bias. And what will happen is let us suppose because of this large voltage of the output side suddenly there is a current flow between the output and input of the M for example M3 right.

When such a thing happens what will happen is that there will be current flow and therefore the voltage of the output will start dropping. Once it tries to drop I would not be able to recover the voltage any further and that is the problem area which we face in the dynamic logic.

**(Refer Slide Time: 23:14)**




So what is the solution? The solution is very simple and straight forward that we use what is known as a Bleeder transistor right what is the Bleeder transistor I will show it you what is the bleeder transistor is all about so what is happening is that in the evaluation phase the output impedance will fall down right I want to look into the fact that output impedance does not fall down in the evaluation phase right why?

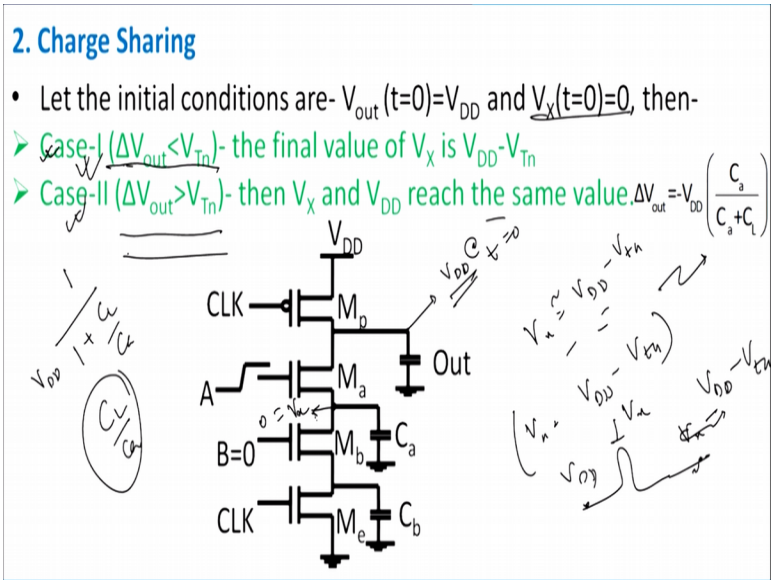
Because if you see you cannot sacrifice on the noise immunity at the output so if impedance level are typically very high at the out it will be very noise good noise (()) (23:53) or easily reject the noise whereas if the impedance is low at the output you have a problem and that is the reason dynamic logics are relatively better in terms of noise margins. Look at the fact what is happening here if we look at the figure here if you look at the figure when Ma and Mb are both = 1 right or both equals to 0 and my clock Me clock is equals to 0 then Me is off Mb is off Ma is off and clock this is equals to 0 which means that all the VDD will flow through this Mp and charge this CL.

As a result this voltage will be typically very high right but we get a problem I discussed with you this voltage start falling through Ma and Mb and voltage here will start to fall down. So what I do I put a PMOS in feedback network with a transistor what it will do is as this voltage starts to go down and down right because that is the problem area facing so this will go to 0 right this will go to 1 and therefore switch off this one.

Whereas if this goes to 1 this goes to 1 this goes to 0 Mb1 is switched on and therefore all the voltage through VDD will fall on to this your capacitances am I clear so I will just explain once again when you have a capacitance available with you and you have bleeder transistor in parallel in feedback network then whenever the output is 1 output is 1 here this ensures this is 1 which means that this is 0 if this is 0 it ensures that Mb 1 is basically switched on and therefore whatever loss at the Ma at this capacitor was thereby virtue of leakages will be made up from VDD.

So this this Mb1 is known as the this Mb1 is known as the bleed transistor fine this is the bleeder transistor which is in front of you.

**(Refer Slide Time: 25:55)**




Now let us see what happens when we are discussing charge sharing right so assume that initially your V out which is just known right is charged to VDD at t = 0 right. And Vx what is Vx? Vx is if this is V out here Vx is this voltage which you see in front of you right this is known as Vx right so if this is gone to VDD at Vt = 0 obviously your Vx will be also = 0 at t = 0 right and that is what it is written there.

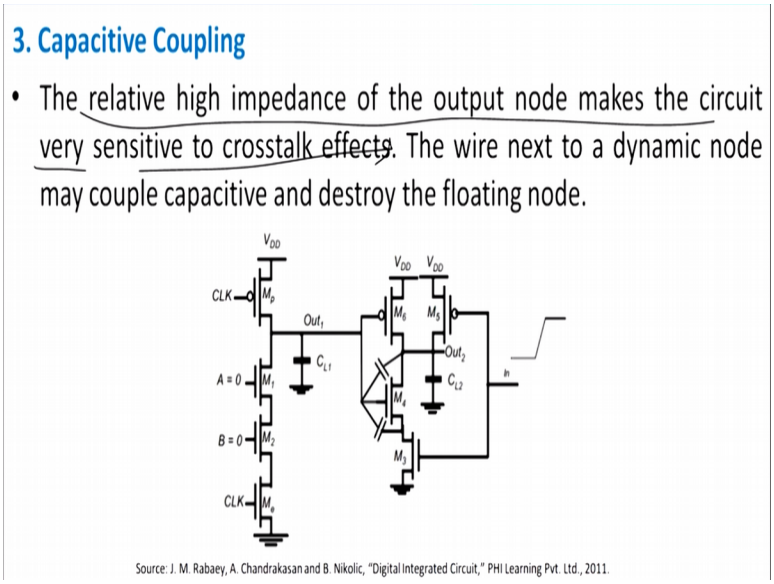
Then under the condition that del V out is less than del V tn under this case you will have Vx is approximately = VDD – Vtn Vx will be equals to equals to VDD – Vtn right I suppose it is very clear to you which means that if you add Vtn to Vx you should have the total VDD output in the output side this is the first case so the final output Vx will be equals to VDD – Vtn right and this

is very standard way of looking at that means if you have a MOS transistor available here and it is drive by a gate voltage say Vx then the voltage of this point will be Vx – your sorry voltage here will be V.

So this is VDD and the voltage at this point will be VDD – Vtn of this transistor right and therefore they will be a f1. Now the case one is different del V out is less than the del Vtn case 2 is del V out is larger than threshold voltage difference. So if this is a threshold voltage difference between Ma and Mb you will have a problem and therefore Ma is less than or equal or greater than Mb this condition with the delta V out will be always greater than Vtn right once this is true you get delta V out is equals to VDD Ca by upon Ca/ Ca the standard sort of algebra expression which is available to you and from here I can find out the values of this thing.

So if you have so it is basically VDD right Ca if you divide by Ca I get + 1 CL / Ca so depending on the value of CL /Ca I can actually shift either to the condition number 2 or condition number 1 right so this is as far as the dynamic logic concept is concerned and it is basic idea is concerned right.

**(Refer Slide Time: 28:33)**




Let me go to the capacitive coupling here right and after capacitive coupling we will talk about next case. As I discussed with you the relative high impedance of the output node make the circuit very sensitive to crosstalk effects. So if you have a cross talk in nearby circuitry nearby if

you have transition is taking place or whatever this circuit will start get effected and that is what it is known as a cross talk effect.

Now so that is the basic problem of capacitance so you have capacitive coupling when this capacitive coupling voltage they rises to high value when this rises to high value you have to careful that you do not have a high impedance node available at any point of time and as a result it either connected to ground or to VDD right so this is what we have learnt from our previous discussions. So I will just I think I will stop here and then you will take up a subsequent discussion in talk free to in the next class thank you very much.