CMOS Digital VLSI Design
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Module No # 04
Lecture No # 19
Combinational Logic Design- VIII

Welcome back to the eighth module of combinational design logic of CMOS VLSI digital design for the NPTEL online certification course before we move forward therefore we need to we had finished what we had finished the concept of static CMOS logic which primarily means that at every point of time the output will be either connected to VDD or to ground. So they cannot be any high impedance node available to you in the output side right.

So that is what you what was there but then the price you paid the price for having such a logic one was low to high swing when you are transistor up pull up transistors getting on again become a ratioed logic which means that it is the W/L ratio will determine the functionality of the chip of the logic. So that is the price we paid for it before we move forward one small portion is left actually of the previous case we can take up now. If you remember when we were discussing a inverter and we are trying to find out a delay we define something known as Elmore delay.

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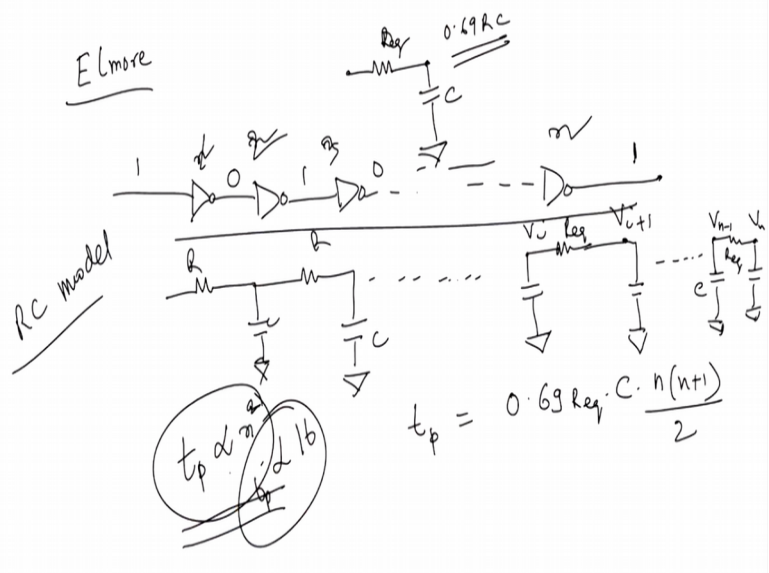

Elmore delay was looking from particular point if you see a resistance and it is corresponding cap here capacitance here then the delay at this particular point will be nothing but 0.69 R into C right. Where is the effective R equivalent here and C is the capacitance which you see right. So this is what you see has far as Elmore delay is concerned so let us suppose I have I have a inverter and I have pairs of inverter like this right and I have pairs of inverters like this and so on and hence so forth and its ends up here right for some reason it is like this.

So what we do is that we segregate into this small each one of them as a pair of resistances and capacitance so on and hence so forth and then we say this to be as Vi let us suppose voltage at high R equivalent and then you have got C here then it becomes V = I + 1th node I get some value here of C and then this grounded and then similarly I get V N – 1 at this IN – 1 node and then we have got C here available to me and finally we end up at V Nth node V the capacitive loading C here available to you with this between them it R equivalent.

So this is the RC model for a pair of cascaded CMOS inverter also known as buffer if you look at its graph or if you look at it delay I am not deriving here all in detail manner it is 0.69 R equivalent time C into n into n + 1 / 2. So this is the delay for the formula n is the number of stages or number of number of this is 1, 2, 3 so on and hence so forth till n number of transistor inverters are using when it is n square.

So you see tp is actually proportional sort of N square and that is quite critical whenever you are trying to find out the circuitry because if you buffer is basically 1 so if you see if you look closely this is 1, 0, 1, 0 so and hence so forth. So output will be also again = 1 right so generally such type of structures are always available to you at the input output interface right for impedance matching purposes for signal to be transferred with least amount of power loss we do impedance matching and to do that we apply a buffer between the input and output.

Once we do that between the input output part of the system while doing that so we get the very good profiling in terms of power dissipation and in terms of signal integrity then there is loss of hos speech and this lot of speech is by virtue of this tp proportional to n square. So if you use say for example force stage CMOS inverter buffer then I will get approximately 4 square which is 16 time tp of will be proportional to 16 times of the delay of the single gate.

Now this is quite interesting and quite difficult when we are actually dealing with specifically with Elmore delay right. So this is what people have been or people have been doing it for quite long time and then it becomes proportional to this thing later on as you move along we will see will try to find the solutions for this this problem right.

I leave as an open problem to you that can you find a solution to this problem that if you have a long chain of inverter can I do some manipulation in the chain of the inverter so that my delay is reduced drastically right think about it and this will be part of your assignment or you can do internet go through internet go through books and try to find out the solutions for this one right this is optimized solutions available for this one in any case right please try to do that.

We come back to today's this times the module which is available was and that is combinational logic design part 8 right and till now we were actually concentrate in static logic thereby saying that my output voltage output node will be either connected to VDD or ground primarily meaning that it will be connected to very low impedance nodes right this is the first time where we have seeing that you might have a position where the output nodes are not might not be connected to low impedance node. It might be actually connected to a high impedance node in general.

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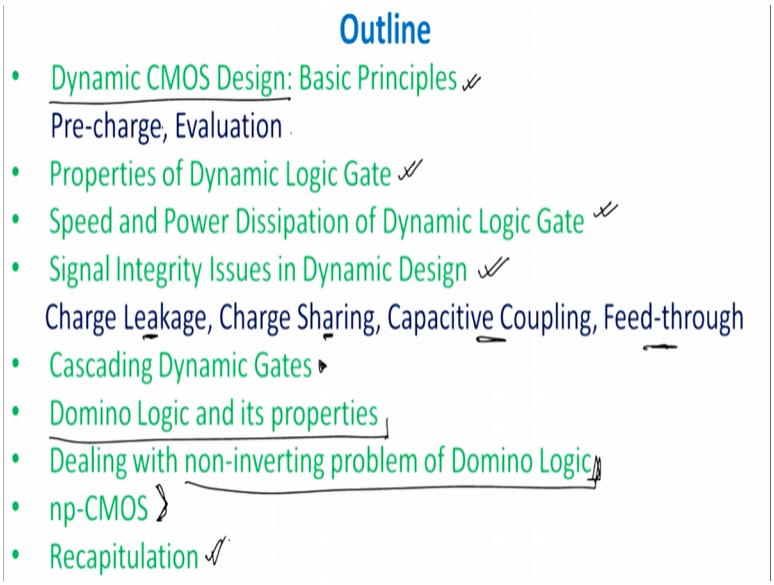

So we define so what we trying to do we will study dynamic CMOS design we study CMOS design you will get dynamic CMOS design and look at it basic principle of recharge and evaluation right what are the properties of dynamic logic design you will have a look then as with static design we will also look at it speed and power dissipation signal integrity issues we will be concentrating on for CMOS dynamic logic design out of which we will be looking into primarily four issues one is known as charge leakage another is charge sharing third one is capacitive coupling and the fourth one is feed through right.

And all these mechanism actually lead to signal integrity issues which means that if you have a signal available the signal might actually be the voltage level might fall down or may rise up whatever so you would not be able to have fixed value of voltages these four phenomena which is just now stated gives you have varied values of voltage of the available in the output side.

So we have understood how to cascade your static logic and when you cascade it we saw it that there will be a threshold voltage drop when you are passing one through an NMOS logic for all practical purposes. So how do you cascade a dynamic logic we will understand that as well so we will be looking at how to cascade dynamic logic and then important one family of dynamic logic is basically a domino logic and we will look it properties of domino logic right and then we will dealing with non-inverting problem of domino logic and very important problem about domino logic finally we will look at np-CMOS and then recapitulate the whole module in general sense. Recapitulate the whole issue in general sense right.

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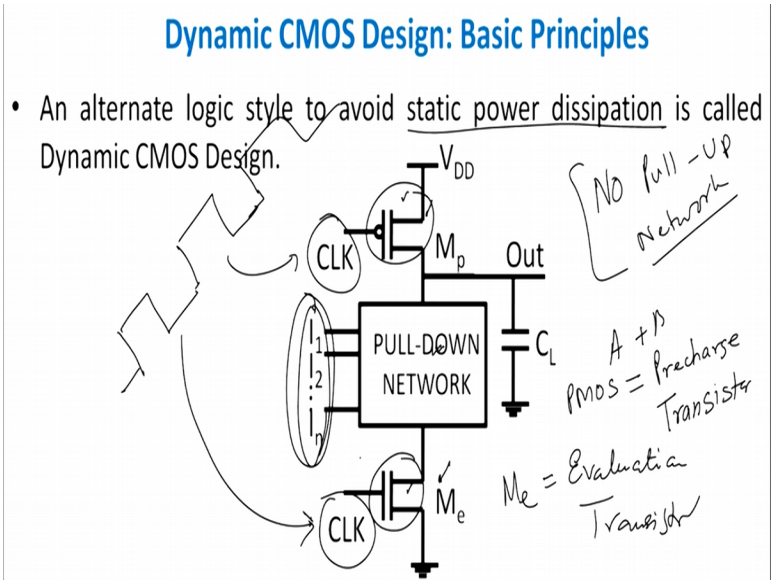

Let me start dynamic CMOS design here and this is basically a style to almost eliminate the static power dissipation if you go by my previous slides in my previous discussion you will understand that when I was discussing with you the power dissipation characteristics you will understand that current technology (()) (08:46) such that you will always have the static power dissipation on a rising trend.

So this is a point where if you want to reduce power this is a point where you should be able to hold back the power down right and this dynamic CMOS design helps you to do that right and helps you reduce the dynamic power sorry study power dissipation drastically or out of which the static power dissipation will reduce drastically here. Let us look at the first basic feature of a dynamic CMOS design.

The first basic feature is it is exactly like a static CMOS only thing is rather than applying input to the gates of PMOS and NMOS you start applying the gate to the pull down network so it do not have a pull up network please understand there is no pull up network though there is a mistake in my language but I do not have to design a pull up network it is already inherently present in the dynamic logic but I have to design the pull down network depending upon the Boolean expression which I am trying to achieve.

So let us suppose I have a I want to achieve A or B then I need to make it such that A or B here it will be always complementary in nature and therefore I have to put a either a CMOS inverter or I

can get a out bar from here. So I have so this is my pull down network right and I have sets of input available i1, i2, i3 till in and the PMOS is this is one this is PMOS and have got a NMOS here this is drive by clock. So I have a clock here clock is what clock is a sure transition cycle like this you will have clock generation taking place.

This will be fed here and this will be fed here clear if this is clear to you we define this PMOS transistor PMOS transistor as a PMOS transistor. So we define this to be as a pre-charge transistor right and this ME which is at the NMOS pull down case is defined as the evacuation transistor. So I have a pre-charge transistor here and I have evaluation transistor in the pull down network.

So please understand what you have done we have almost the same concept as the static inverter only thing is that at pull down stage we have put a pull down network with all the inputs available and i have applied a clock at evaluation transistor and the pre- charge transistor to make it go high or low whatever you have to do it we have trying to do that right that is what is happening when we discussing the dynamic CMOS logic right. So just to give you an idea therefore let us look what will happen in general.

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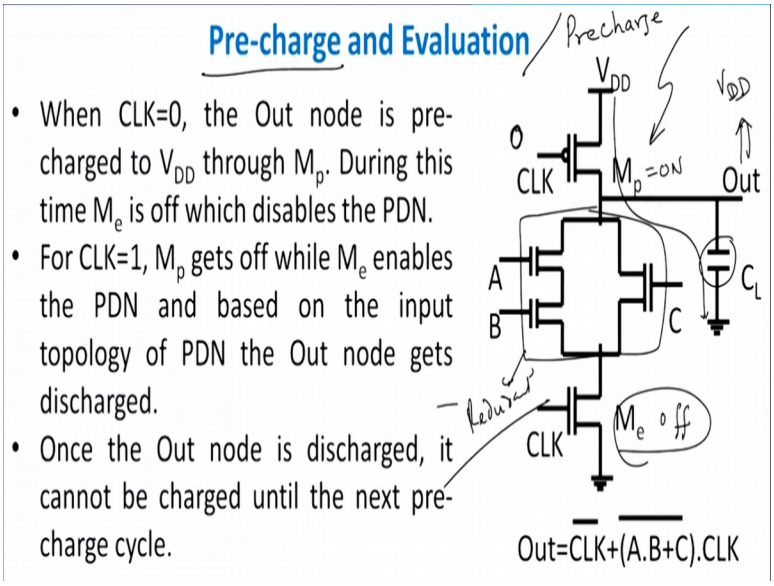

If you look at this structure in front of you which is thing one this is the structure in front of you and assume that clock = 0 right. So clock = 0 if clock = 0 then any will be in off state because it

is NMOS and this will be in ON state I hope all of you agree with me from this point and therefore this CL will be charged through this VDD to which value V out will got VDD right.

So during this this this cycle when clock is 0 and clock is clock is 0 and PMOS is ON and NMOS is off we define this to be as the pre-charge phase. So we have two phases pre-charge and evaluation we define this to be as a pre-charge phase so this in the pre-charge my MP which is the pre-charge PMOS transistor switches on my CL gets charges to VDD by virtue of the fact that there is a there is a low impedance path available and V out goes to VDD fine and V out goes to and V.

Since your Me is in the OFF state this network which is PDN is basically redundant is does not have any meaning whatever be the inputs of ABC even if it is ON even if A, B and C are all one let us suppose right if they are even a 1 so 1, 1, 1 will make A, B, C ON but then your since your clock is also 0 or your Me is Off therefore there is no pull down path available to you and therefore CL charges to VDD this is known as pre-charge phase right. Let me come to evaluation phase and explain to what happens in evaluation phase.

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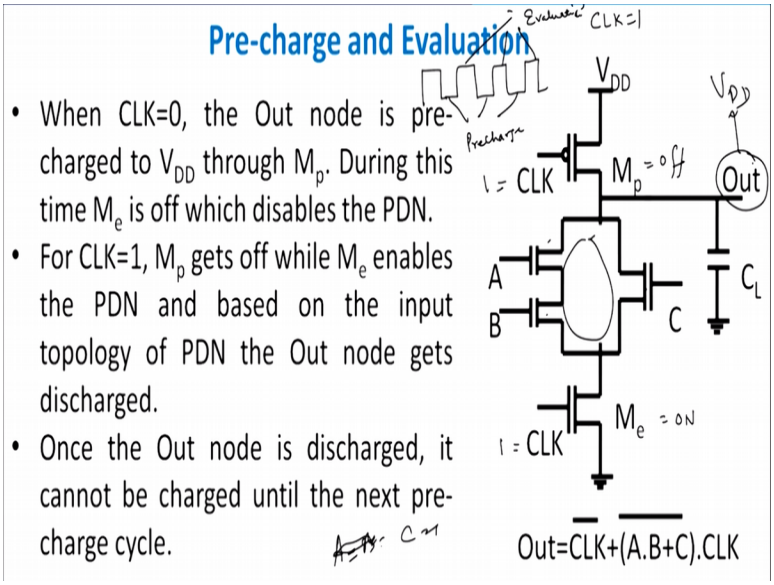

So in evaluation phase what we do is we make clock = 1 so I have clock like this 0, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1 like this so this is my when it is clock is 0 this is this all my this phase are pre-charge phase and my this phase are all evaluation phase fine. So when my clock goes high it this becomes 1 Me is turned on MP is therefore turned off because this clock is 1 right.

Please understand at that point of time this is charged to VDD fine now depending on the value of A, B and C my pull down network gets activated and either this VDD will go to ground or will not go to ground depending upon the type of the input pattern we have got and input type of the input topology you have got in the pull down network in the case that A, B and C are all equal to let us suppose C = 1 then if C = 1 even when AB is not 1 I will have path available between these two points VDD will go to out will go to 0.

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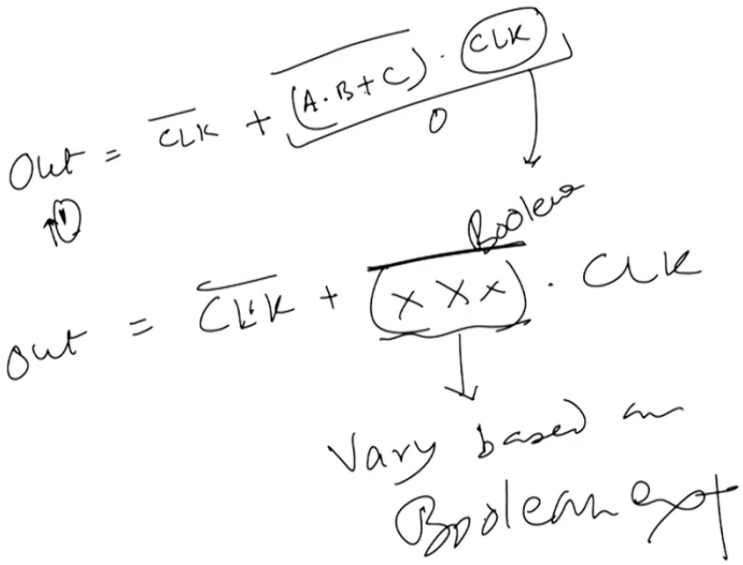

So you see out is defined in this manner out is defined as right I will just switch it is clock bar + is defined as clock bar + A right dot B + C bar of that into clock. So whenever your clock is high evaluation phase this becomes 1 depending upon the value of ABC this becomes high or low therefore it becomes we will get an output.

Similarly when the clock is low this vanishes does not come into picture because this will be all 0 and clock is low output will always be equal to 1 fine. So this is the Boolean expression for the for the this thing so the overall Boolean expression therefore will be out will be equals to clock bar + this whole thing will be X whatever not of that into clock but this will vary with the user vary based on requirement on Boolean expression right.

So based on the Boolean expression this value will change and you can automatically get a value which is there now please understand my basic issue here. The basic issue is that please

understand that once you have pre-charged your output node which is this one to VDD there is no way there is no way in which you can get discharge until and unless clock is high and your pull down network is activated means activating this is that allows you a path between output and input fine.

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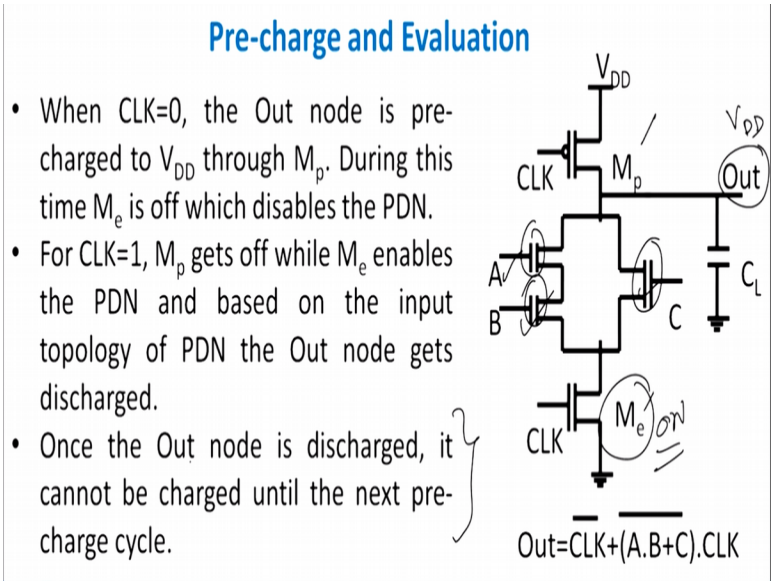

So this is the last part which I was trying to say that (once the out node is charged similarly once the output node is discharged there is no other way to charge it until and unless we reach the next recharge cycle are you able to get the picture. That once we until and unless we get into the next cycle once discharge cycle once discharge is gone. So the data once it was stored in the CL Me becomes high your PDN is active and the output goes to 0 and you finished.

So you have to wait till next pre-charge cycle to do it similarly if V out was equals to VDD and in the next evaluation phase you are not able to lower it by for whatever reason you still remain at VDD even when your go to the pre-charge phase right. So this is very important one should be pretty aware of this basic fact I think it is pretty simple and clear to you.

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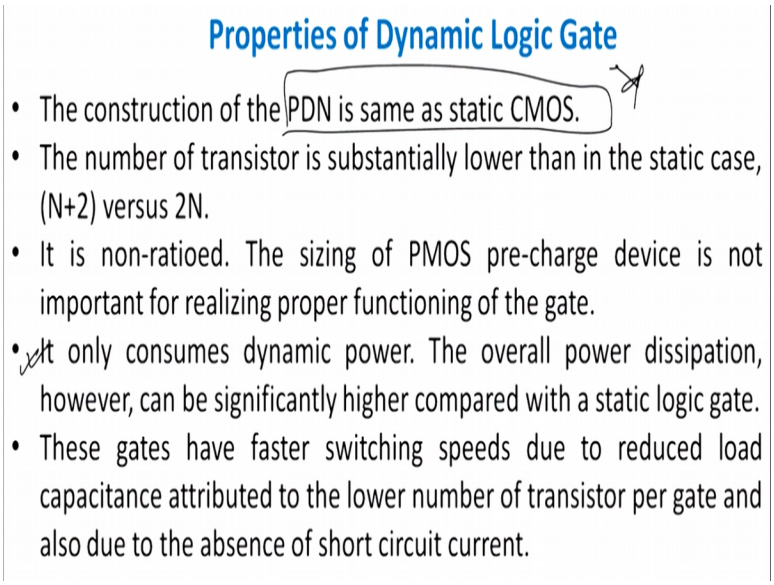

The construction of PDN as I discussed with you is exactly as same in the static CMOS logic alright very important so if you have understood how to make a PDN networks or pull down networks in CMOS logic it is just plug and play here nothing extra ordinary and nothing different from what we have learnt earlier.

However the number of transistors required here is only n + 2 why n+ 2 n will be required to do the PDN pull down network and 2 will be why because 1 will be evaluation PMOS sorry pre-charge PMOS and another will be evaluation PMOS. So you see you are only require n+2 times n +2 number of transistors whereas you require 2n transistors in static CMOS logic. The third part is it is basically a basically a non-ratioed logic and the reason is the sizing of PMOS device is not important in in understanding the functioning of the device of the of the dynamic logic.

So you make it large make it small as long as it is ON for particular value of the clock it will always charge the output to VDD so irrespective of the W/L ratio of the PMOS the output will still charge to VDD yes if you make it very large value of strong device then it will be charging faster if you make it a small device it will charging slower that is all but it will charge on the less and therefore you V out will always go to VDD irrespective of the value of W/L ratio of PMOS and therefore this is basically a non-ratioed logic unlike the other logic which you have seen in the previous past.

As I discussed with you if you look very closely there is no short circuit path available to you which was available to you in the static CMOS logic here since you do have a direct path at any

point of time between VDD and ground your static power dissipations are 0 why and I will explain to you why is like this see when your see at no point of time MP and MN are both ON or off together.

So either one of them is ON and another is off forget about even forget about pull down network VDN you forget about PDN just look at MP and MN they are not even switched on together or switch on or switching off together. So there is no question of VDD getting directly connected to ground and therefore your static power dissipations almost 0 is 0 in this case of a dynamic logic design right.

So what is written as the third point of third bullet here so the last point is that they have relatively higher switching speeds because the capacitive loading low in the previous case when you are doing static CMOS the PMOS is also getting loaded here only NMOS is getting loaded to a larger extent right and as a result your PMOS and NMOS are it is in the loading is very low in this case the capacitive is low and therefore switching's are much faster switching are much faster right.

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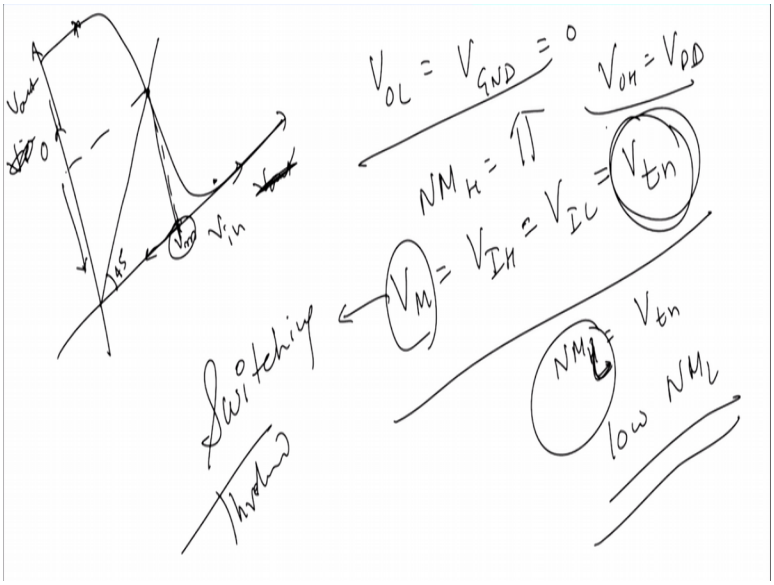

One more thing in this case is that VOL will be equal to VGND ground which is 0 approximately output low and the reason is that you are allowing the voltage at the output node to go to the ground node right and it is going very easily like obviously it will go very fast because you have high current to flow there and as a result it will always go to ground load.

Similarly your VOH will be equals to VDD so your NMH is very high noise margin is very high. However please understand your switching threshold = VIH = VIL and this is equals to Vtn please understand why I have writing this why switching threshold this is VM is my switching threshold switching threshold remember threshold switching threshold how do I defend switching threshold when I was drawing V out versus V in of a Vtc of a of a transistor of a CMOS inverter we define this to be as the switching threshold yes this is 45 degree on draw line this was defined as switching threshold.

So this is the value of input voltage let us suppose this is the value of your input voltage above which it will read as 1 output will be read as 0 output will be read as 0 and below which the output will be read as 1 right easier for your understand if you do something like this let it be Vin let this be V out. So V in is lower than the VM value VM is this value this value output is high and VM when V out V in is greater than this value the value of your V out is low which is this value right this value.

So this switching this is switching threshold now you see when I was discussing with you the past the dynamic logic here then I can then if you look at the if you look at the where you are in the evaluation phase obviously Me will be on as I discussed you but this will start switching A, B, C will start switching only when the input voltage is larger than the gate voltage of the individual transistors.

Am I clear so you have wait till the input voltage to the PDN crosses the value of threshold voltage if it crosses they become and suddenly there is a fall in the voltage. So that is the reason I was just now telling to you that my switching threshold will be always equals to the threshold voltage of the device which you see right which means that which means that my MNL rather than going to ground is actually latching to Vtn and therefore NML is not very low.

So it is it is very low it is basically low NML should also be high but it is not high and the reason is we have Vtn switching taking place here right. and that is the reason you will have always a low NML but high NMH in a static noise margin in a dynamic case of a CMOS inverter with this we finish off this particular section we will meet next time we will take up the next issues of the

charge sharing mechanism all those feed through and after you finish it we will come to logical effort next module will take up next time thank you very much.