CMOS Digital VLSI Design
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Module No # 04
Lecture No # 18
Combinational Logic Design – VII

Hello again welcome to the next edition of NPTEL online certification course on CMOS digital VLSI design. We will be starting the combinational logic design module 7 now in our previous module we have seen certain thing which I will just recapitulate and then we will move forward. (()) (00:45) We have seen that the if we use the past transistor logic your level voltage levels of folic and if they fall below the switching threshold of subsequent block or the subsequent gate then the your require to level of initial value right.

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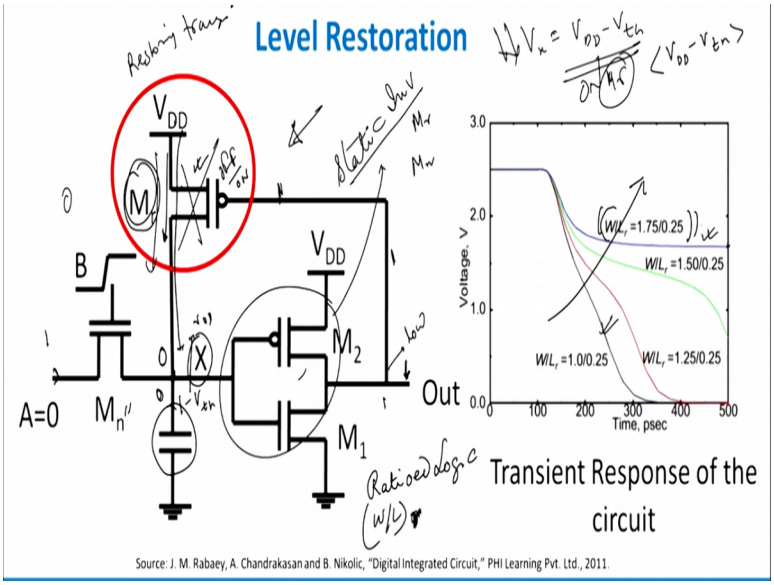

So you will try to make it above the switching threshold for that practical matter as you have seen in our previous discussion is that that this this if you look at this point if you look at this whole discussion here you will see that we have seen that you had a drop of VDD – Vtn we had seen already this drop available to us now as I discussed with you previously if this is therefore this is 1 then this is cut off and therefore this remains as 0 but if it is a 1 here I get 1 – Vtn right and there is a result this might be high a low when this becomes low this becomes ON and then

this becomes ON this VDD starts to charge this and tries to make it to reach to VDD and you already seen this point.

We have also seen that if W/L ratios are large right you have a change in logic therefore level restoring circuits which is this one is primarily ratioed circuit so it is a ratioed circuit primarily meaning that the aspect ratio of the pull up transistor is critical in the functioning of the level restorer circuit. So that is the important key switch to take over from here that this is basically ratioed logic right it is a a ratioed logic which means that W/L of P plays a critical role a critical role P means in this case the restorer.

But as you can see higher W/L we will imply a larger ID flowing through this path right and therefore faster restoration of logic at X this is understood but please understand critical issue but as you start to make the W/L ratio of MR larger and larger the capacitor will loading here which is this one will also start to increase because this X sees a larger capacitive load right and therefore as you make the W/L ratio large though the current taken to charge this to VDD is also higher but then the capacitance value or the capacitance seen at this node also raises so the capacitance value become becomes larger right.

And that is the problem are which come into picture with the larger W/L ratio so as you can see in this slide here the higher the W/L which I made the voltage was actually restored to its original value to a larger extent right expected also in a longer run we have also ensured that the sizing of MR right MR is this one and MN which is this one will try to make the logic at X change.

For example if MR is stronger as compared to MN restoring the level X will be faster whereas if MN is stronger as compared to MR DD storing will be more or degrading the signal will be much more important issue. So therefore W/L ratios are important and therefore it is also known as the ratioed logic indirect. This knowledge this idea we can actually therefore explain or understand that that this level restorers are generally used you can also have two PMOS was parallel to each other in the level restorer.

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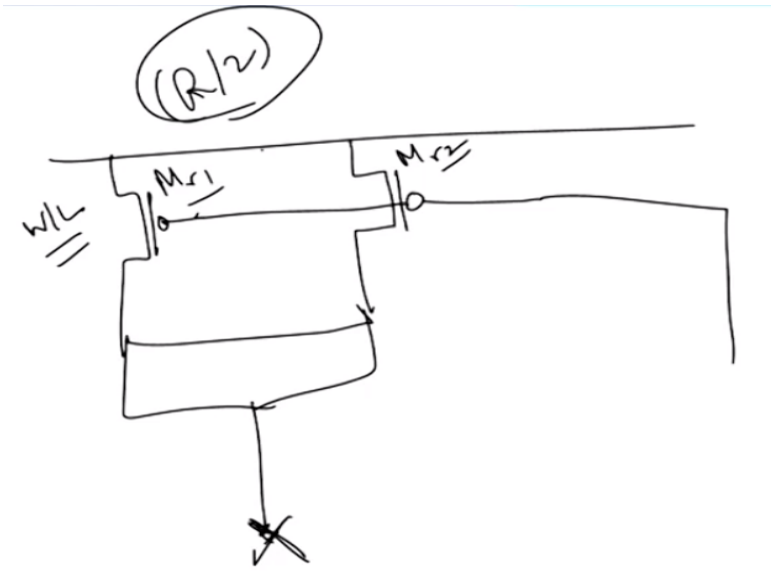

So this is the out feedback path which is coming and it drives better than 1 PMOS it drives to 2 PMOS's. So it drives 2 PMOS's what does it why is it advantages while driving 2 PMOS's is that the current's will be larger because the effective resistance in the pull path will be R/2 and therefore even with the lower W/L I would achieve a larger current flowing through the system and therefore the node X will be restored at the same time the previous case only thing will be you will have now larger smaller time to do that right.

So this implies that you have a reduction in the resistance available to you if you are restorers are so this is MR1 this is MR2 then MR1 and MR2 together will form a composite device which will be lower than potential at this particular point form a composite device which will lower the potential at this particular point at a very fast phase. Coming back to the concept of power dissipation.

Please understand the power dissipation here is very small and the reason means there is no static power dissipation almost 0 almost 0 the only problem is that the rate at which the data flow into the system will be actually limited by the tp of the delay of this inverter block right. So if your delay of the inverter block is very high then it takes a finite amount of time for the signal to go here switch on the value of MR and restore the level of X to higher value right.

So therefore the rate at which the date comes at this point will be finally determined in terms of level restorer finally working fine or not upon the actually the propagation delay of this inverter

block right. So with these are the key basic issues which people face or people have a problem when the dealing will level restorer circuitry.

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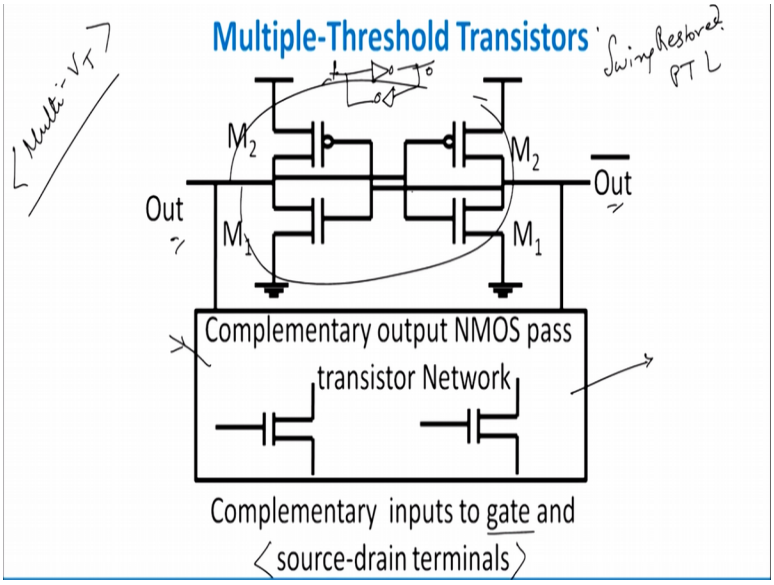

So level restorer is helpful for all your past transistor logics right we come to next turn that is known as a multiple threshold transistor concept here this is also referred to as the swing restorer transistor logic. So this is basically a swing restorer swing restorer restored PTL past transistor logic this swing restore past transistor logic and what we do is that we use VT multiple VT devices multi VT device rather than using single VT we use multiple VT right and the idea is something like this that.

So I have a pull up I have a two inverter this is basically two inverters connected back to back right almost like a memory unit. So I have got two connect inverters connected back to back and therefore once a data is latched here it will latch. So this is one this is 0 I think it is clear to you that these are basically two so it is basically something like this.

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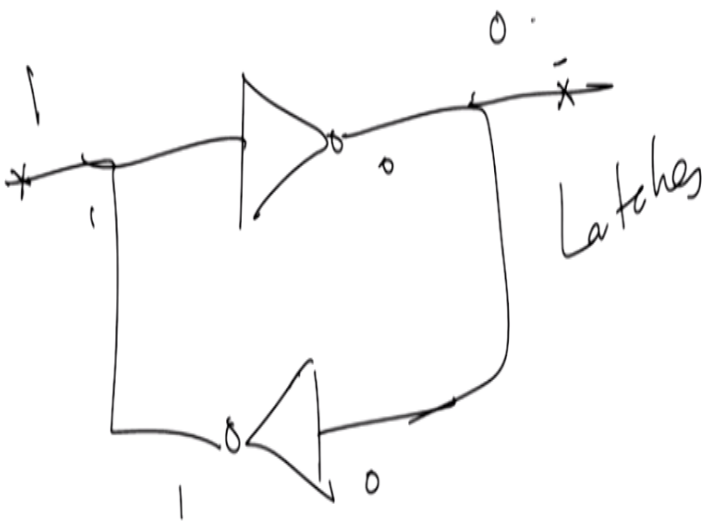

It is I have got one inverter here right another inverter is something here from the pull up case and then I have got if I have 1 here I will have 0 here this 0 come here I get 1 here I will get 1 here I get 0 here. So this is basically a latch right and this latches the values at this point as X as 1 and X bar = 0 and it will remain like this until and unless you overwrite it by a external source by a new value right.

So if you go back to the slide here this part which you see in front of you is primarily the PMOS pull up or the basically the inverter and it stores the data whereas pull down is composed of NMOS transistors obvious and complementary inputs are given to gate and source drain terminal right to gate and source drain terminal we give complementary inputs and complementary output is available to you out and out bar and we latch it using these two values.

So what primarily means what primarily this device does is that it tries to latch the value at a much faster phase in pull up case and latches it to the value which you have defined by virtue of the input signal given to the complementary pull down conditions. Let me show to you basic XOR XNOR complementary logic.

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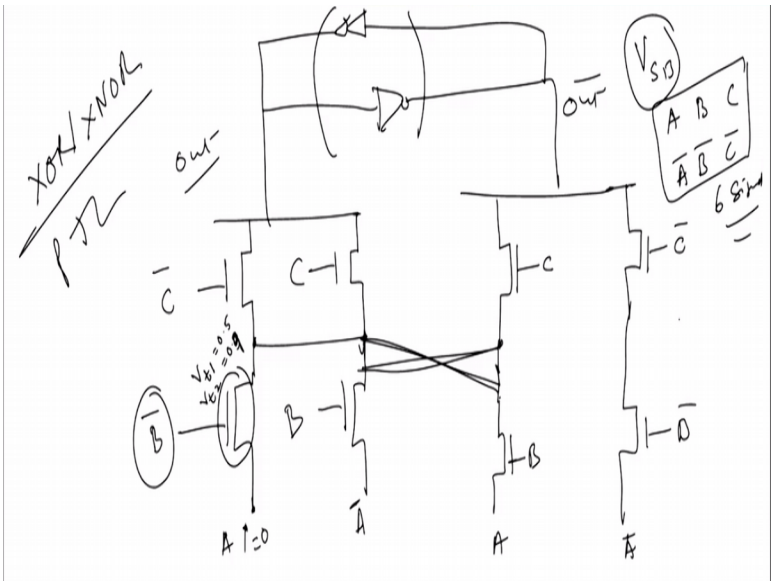

XNOR R is basically a 3 input logic gate and it is basically a past transistor logic. So let me draw for right and I will explain to you what these terminologies are so this is C bar this is B bar this is A right A we have then C and then from here we do B this is B again I have A here but this is A bar here and I connect this to this and if you go this side I have got C here and then I have sorry. So let me show to you that i have got here C right this is C and then you have got C bar here this goes to B bar this is A bar and similarly this comes to this will come to B and this is A.

So this is A this is B bar A bar let us see how does it work out in terms of this actually going to this direction right and this actually going to the. So you see this will be going where this will be coming this this will be coming like this and then this will be going like this. So this is your out bar and this is your out so whenever you are A and you see very well this is basically your XNOR XOR XNOR PTL logic.

So this is basically your swing is to (()) (10:41) PTL logic why this (()) (10:42) because these two latches here which is basically here tries to restore the swing VDD and ground any past transistor logic lowering the swing this pull up devices pull up two inverter payer will actually pull it up to a much higher value and try to latch it to the higher value of available to you.

The problem which people place in past transistor logic as I discussed with you earlier was the you always have a VSB right because please remember in conventional CMOS architectures my source as grounded or connected to the most negative terminal this ensure to me that threshold

voltage change was 0 but in this case you see carefully that you are applying a potential at source end. So in VSB is not equals to 0 at any point of time because source and bulk now relatively at very different voltages.

As a result the threshold voltage will change right and that is quite critical I will give you an example to show to just give you an example let us suppose this is A right and this transistor is there so let us suppose this shows a one here A = 1 voltage here rises VSB becomes larger there is a change in threshold voltage here which is let us suppose it is initially VT1 was equals to 0.5 volts now let us suppose it becomes 0.3 volts right VD2 after the change.

So you require a less amount of voltage to do it fine or reverse if let us look at the reverse first suppose it becomes 9 but your B bar which you got from some place it is value of voltages is just 0.6 because he knows for sure that 0.6 will switch on the value of the we will switch on this transistor but by virtue of VSB the threshold at shifted to higher value let us suppose and there B bar has to be at least 0.9 to switch it on then the whole functionality of this swing restorer PTL actually fails right and it would not work properly for you.

This is 1 important point which is always keep in mind the second important point here is that A, B, C I am assuming that A, B, C and A bar B bar C bar is all available to me. So all this 6 signals are available to me. For availability of the complementary signal if you remember we require a static transistor and therefore just to have 3 signals and 3 complementary signals we require 3 CMOS inverters which primarily requires and we require 6 transistor extra.

So that extra count you should keep in mind while discussing past restorer logic right and that is I was trying to discuss with you in this case. We came to the last type of logic we used swing restorer we use swing restorer one of them we use the second case in which we had the pull up and we had we had CMOS inverters which connected back to back which was able to pull the whole voltages up to VDD and push it to ground right.

The third one which is being seldom used in digital logic design is what is known as transmission gate logic. I will explain to you what is transmission gate is then we can see 1 by 1 how it works out. We have already discussed that NMOS is a good strong passage of 0 and PMOS is a strong passage of 1 right if I replace NMOS PMOS by single unit transmission gate I

will show you how I can actually have my voltage being not almost constant independent of everything else. So there will be say it will good it will be a strong passage of 1 it will also be strong passage of 0. So both will be passed very strongly by transmission gate logic and how.

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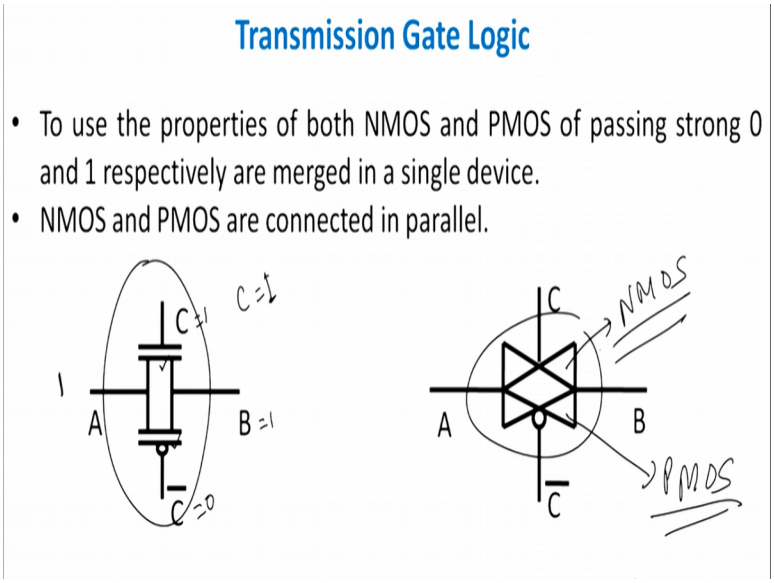

What is the transmission gate logic I will just show it you by this diagram which you see in front of you which is here right. So let us suppose A is 1 right A is 1 if let us suppose C is to 0 or 1 then C = 1 since C bar will equals to 0 this PMOS and NMOS and PMOS will be both on and AB will be equals to B will be = 1. I will explain to you what otherwise this looks very complicated but let us been threshold to you.

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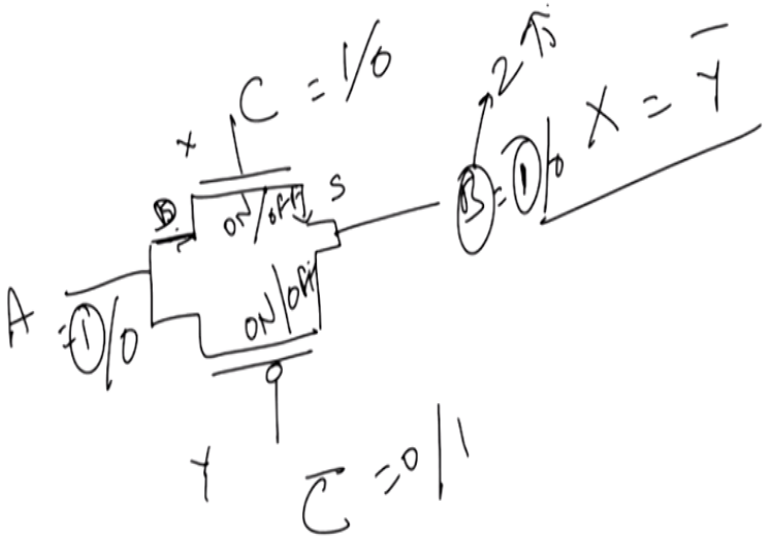

So I have something like this I have got an NMOS here right I have an NMOS this is a drain this is your this is a source and then connect to it PMOS right which is something like this and you connect this with A let us suppose this is B right and then this is (()) (15:20) C and C bar so apply complementary signals here and here. So X = Y complement sort of signal you apply so whenever C = say 1 A = 1 C bar will be equals to 0 this NMOS will become on and this PMOS will become on and as a result 1 will be transmitted to this B and B will be read as 1 or if it is 0 it will be read as 0.

If either C is 0 and C bar = 1 this will be also this will be also and therefore this will be high bit on states this will be in ZI having bit of state right. So the transmission gate helps you to transmit a signal without any degradation of signal what is the logic behind it very simple. Since I have got a NMOS and PMOS in series to each other right sorry in parallel to each other we will that the compound device which you see the effects real effects of passing one and zeros will be actually removed in this case.

So just to give you an idea and this is the schematic which we generally use in our locality that this is basically looks like this. So this is basically your NMOS right and this is effectively your PMOS right. So I have NMOS here I have a PMOS here for a practical purposes right. So let me come to therefore explain to that how does how does therefore may so this is what we get from this side now I will just show you how it works out in a detailed manner that.

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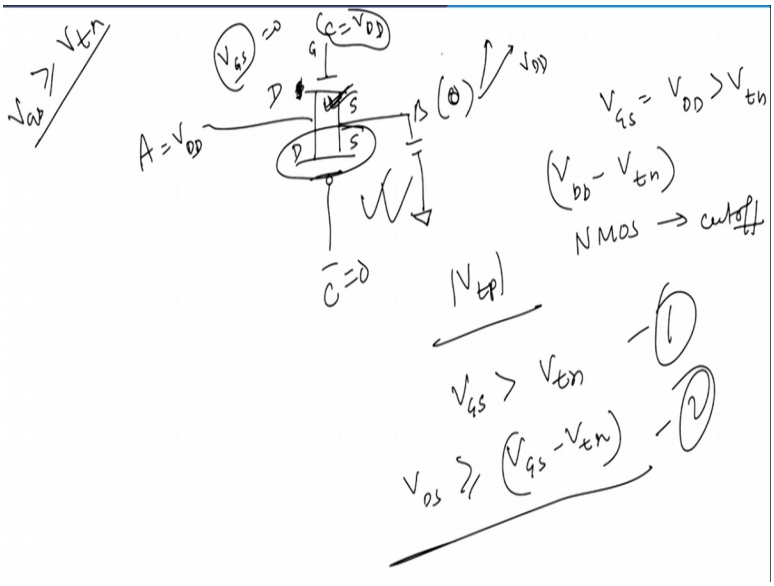

Say I have a NMOS and PMOS payer something like this right and this is C bar = 0 and I get C = VDD right I have got A = VDD and therefore B will be initially 0 suppose I have CL and this is grounded right. So initially let us suppose it was 0 initially and this is all half now what you do you give C = 1 and therefore C bar = 0 and therefore this will rise to a value = VDD but now obviously rise to its value = VDD.

The idea is that this is an NMOS this one is basically an NMOS it is a very strong puller of 0 right so if this is VDD right let us suppose this is gate obviously and this is source may be this is a source let us suppose or if you want to put it drain also does not matter but this source then VDGS gate to source voltage will be 0 if it is 0 it implies I cannot switch on the device because VGS should be actually greater than equal to threshold voltage of the device Vtn look it in an sense.

If i connect this to the drain this to the source and similarly this is drain this is the source then at such a stage when initially it was 0 then VGS was equals to VDD which is basically larger than Vtn of NMOS this switches on the device and therefore current starts to flow and charging it to near VDD as it starts moving towards VDD till VDD – Vtn right till the voltages rises to VDD – Vtn after this the NMOS goes to goes to from saturation and comes to region and therefore after this it will come to cut off below this.

But then please mind by that time the drain to source voltage of PMOS is such that but it has actually crossed mode of Vtp and therefore this has turned on and it is into this saturation region and therefore there will be current flow because of this. So the idea here is that by simply manipulating the values of the charge carrier or the current by virtue of the fact that for a device to be in ON state in saturation VGS should be greater than a Vtn for ON state I should also VGS – Vtn VD SAT VDS should be greater than equals to VGS – Vtn for it to work in a saturation region.

With these two conditions 1 the condition 2 I can safely say that I can have ac current flow between point A and point B of this network right assuming that you had initially 0 value available in this case.

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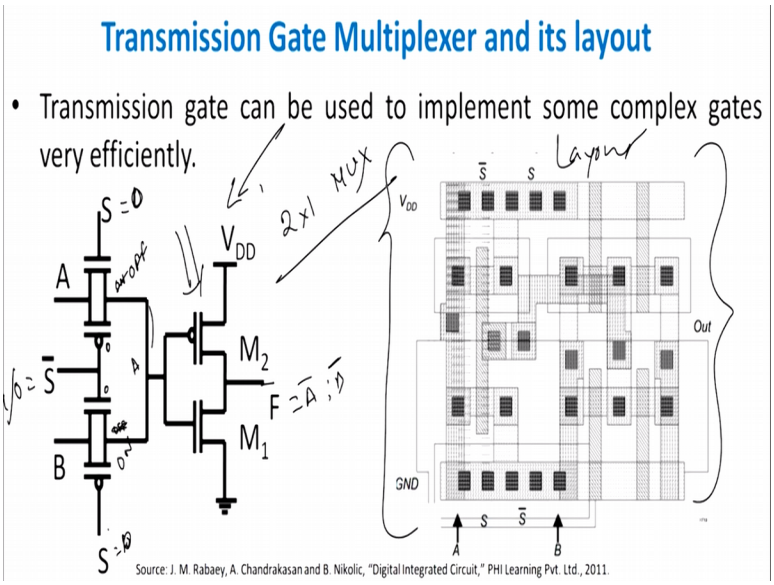

With this basic understanding of transmission gate logic let me show to you how a multiplexer can be designed using a transmitter gate I suppose multiplexer is clear to you. Multiplexer means that using a control signal I can actually allow certain signals to cross through and then disallow certain signals so if you have got three input signals available to you then by using certain pair of select lines I can allow only one of the signals through pass through and all others to block.

So this is basically a multiplexer design if you look closely to the left hand side of the this one do not worry about this one this is basically lay out which you use I am not discussing it at this stage this lay out this is basically layout of a tg logic also they are known as transmission gate if you very closely look here it is basically if S = 1 right S bar will be equals to 0 and therefore A will come here right if S = 1 this will be S S bar this is S also.

So if this is 1 right then this is 0 agreed this will be and this will be 1 and therefore this will be off and this will be on when this is on A will be transmitted to this point and A bar will appear so F will be = A bar. Now if S = 0 right so I get 0 here I get 1 here if it is 1 then this becomes ON and this becomes off so this becomes ON this becomes off right and B gets transmitted to the bar output side B bar sorry B bar gets because i have a static inverter also available with me.

So therefore by having 1, 2, 3, 4, 5, 6 basic transistors NMOS and PMOS I am able to design 2 is to 1 mugs. So this is basically design of 2 is to 1 mugs for all practical purposes and this was very fine for transmission gate logic right. The only thing which we should be careful and that is

very important as for as designing with tg is that you should ensure that SN S bar or C or C bar which are basically the clock right.

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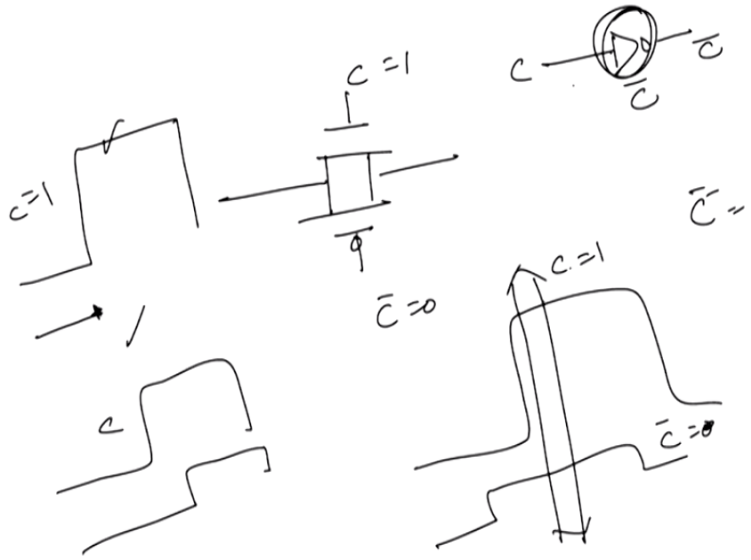

So what I am trying to tell you is something like this that if you have a transmission gate logic and the transmission gate logic has got something like this right so this is C = 1 and C bar = 0 then you have ensure that C = 1 and C bar = 0 happens exactly the same instant of time. So C = 1 means like this C = 1 and then it C goes to 1 then C = 0 is something. Let us suppose this it goes like this it stays 0 here right.

So they should be complementary in nature and there should be no overlap so let us suppose I have C here and I also have C1 something like this right or something like C1 here suppose C = 1 here right. I want C bar = 0 right I want C bar = 0 but what is happening is the let us suppose C bar is not equals to 0 it is something like this. This is C bar let us suppose by some reason or another.

Then i do have a corresponding where C1 and C bar are both = 1 and that means that if both are 1 then either of the device will be on not both of them will be on you getting my point. So if you allow only one of the device sort of PMOS and NMOS to get on then you have to also ensure then you will automatically see that the NMOS switches off at VDD = VDD – VGS = VDD – Vtn and the same thing happens mode of VTP when you are using PMOS.

So it would not work and give you a linear profiling for the whole range of voltages so you have to ensure that they are just mutual overlapping signals and the both further the problem is further actuated that the fact that since C bar is only come from C if you put an static inverter. So this will C bar so they will they will always be delay associated here right and this delay will actually then change the value of the output voltage logic level to a larger extent. So this is my just wanted to give you an idea about how a transmission gate logic works and how does it transmission gate help you achieve the factors which you want to do it right.

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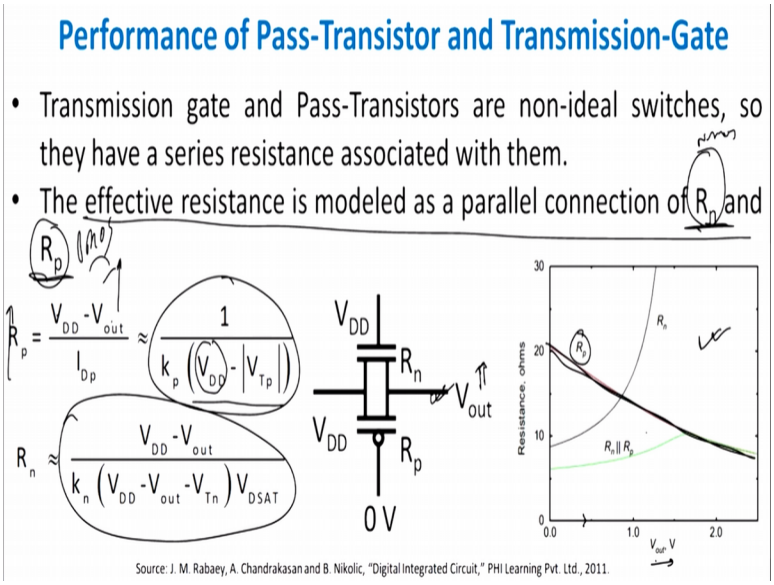

Out of this let me therefore give you an idea about how the transmission gate actually why does transmission gate almost profile of output voltages is almost fixed. If you look at this slide let me look at the slide in front you so as I discussed and the very starting of this module that any transistor when it is ON state will always behave as a resistor now the problem is the resistor will be resistor which you get will be a function of the input voltages because it is one time it is saturation another is non-linear another is linear another is cut off.

So all these three states will have three significant values of resistances and they will vary with respect to input voltage. So what we do here is the effective resistance which you see is modeled as a parallel connection of Rn and Rp which is basically the NMOS and PMOS resistance. So Rn is basically the NMOS resistance right and Rp is basically the PMOS resistance which you see in front of you.

Now if you see Rp is given by this formula do not worry from where it is coming at this stage and Rn is given by this formula which you see in front of you right. As you can see here when my VDD – so if you if you look at this point if you look at Rp as VDD – mode of Vtp becomes low and low right Rp goes on increasing. So you look at this graph which you see in front of you this one on the right hand side as Z out increases right as Z out increases this VDD – VDD term so becomes larger and larger right.

As it becomes larger and larger sorry when let us suppose V out increases then V out increases then what you see is that V out means this is V out this voltage increases this is increasing then your Rp will go on falling because why because v out is increasing right and as a result VDD – V out will be smaller and smaller and the Rp will be almost linear available to you so red curve which you see in front of you is basically the variation of Rp which respect to the external voltage which is V out in this case.

Just the reverse happens for Vn in Vn Rn, Rn is the resistance offered by the NMOS transistors so if you look at this Rn as the voltage increases output voltages increases Rn actually starts to increase because I think I can make it clear. See when VDD increases the output voltages VDS starts to increase.

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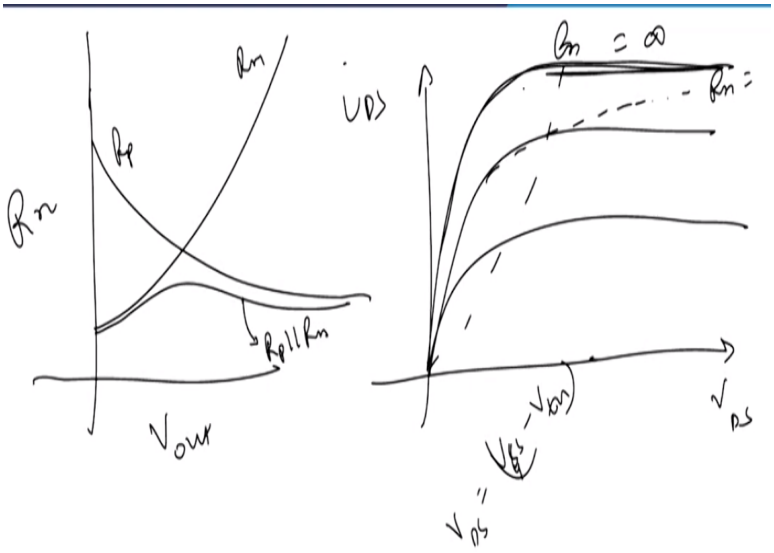

If you go back to your very basic IDVD characteristics of an NMOSFET it is something like this it was something as you are plotted remember that if you plot VDS versus IDS right drain to

source then initially is my resistance small and then it becomes infinitely large at this point at this point is almost infinitely large. For ideal case infinitely large if you have channel length modulation effect you will have at value of Rn which is finite value but will be always less than the infinite value.

So therefore as you increase the value of VDS beyond the point which is given by beyond the point VDS= VGS – Vtn you went into saturation and the resistance suddenly become very large. So if you therefore plot a V the value of Rn with respect to V out you can see that it will be sort of increasing value. Let us Rp will be actually almost like a decreasing value so this is Rp and this Rn right. So if you take this to together I can get us I can get a profile so this is will be nothing but Rp parallel to Rn and that is was I was showing you here. If you look at the green curve here I can read this whole thing it is all these things.

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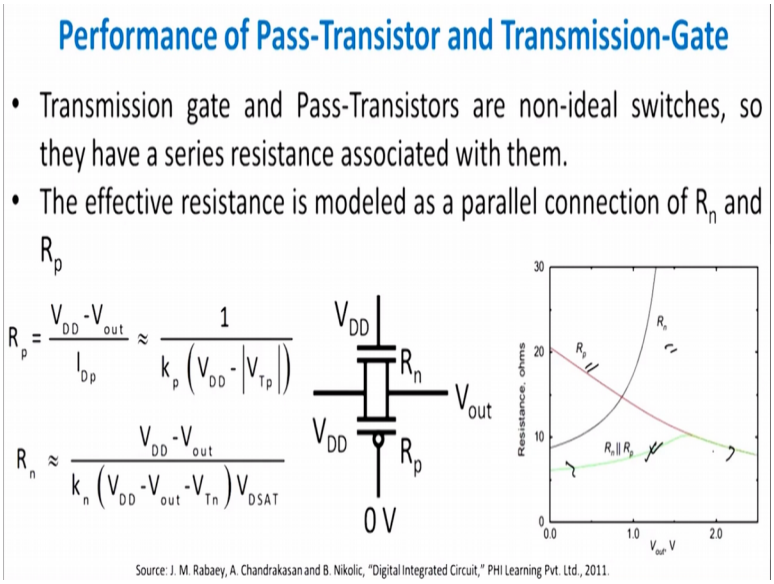

Then if you look at the point is green curve is basically the parallel combination of Rp and Rn. As you can see this is almost flat almost flat which means that the resistance is constants independent of the value of V out see if the resistance is constant the value of voltage available to you in the external part will be also constant and it will be lower than both Rn and Rp. If you look very carefully Rn parallel to Rp will be than the least as you know to resistance character will always be in parallel to less than the least.

When it is so automatically get a resistance which is much smaller as compared to the previous two cases and therefore there will be a good transmission of either 1 or 0 from one point to another right. So this takes care of the value of the past transistor logic.

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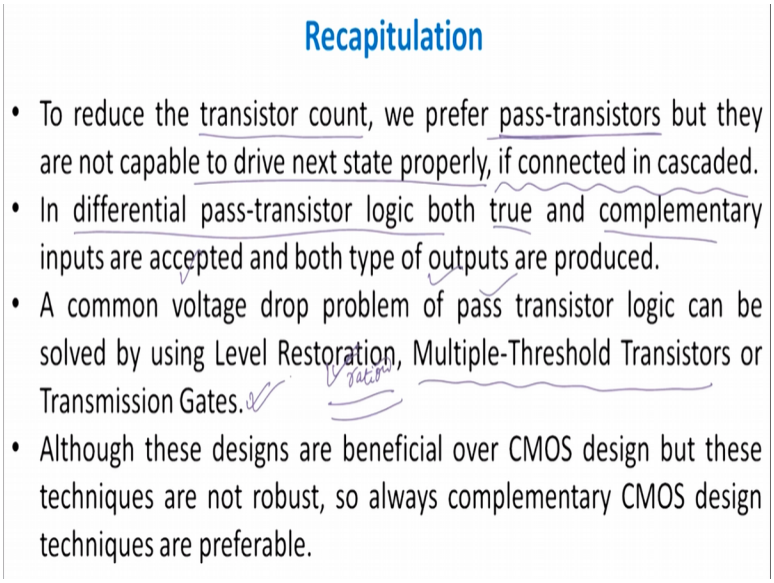

To recapitulate let us see what we did to reduce the transistor count what we did was we did so if we reduce the transistor count here and we had preferred what is known as the past transistor logic right but the but then past transistor logic has got difficultly to the next stage properly the reason being there will be a drop in the voltage available to it and it might be even then the switching threshold of the subsequent block and as we see that if it is cascade we do have a problem of transmission.

Now if we have a differential past transistor logic also known as swing past transistor logic then both true and complementary forms are accepted and both around out bars are also produced. We can remove the problems of past transistor logic by using level restorer by using a PMOS in the pull up case but as I sort I discuss with you changing it's a ratioed logic for sure. So this will be a reatioed logic right and therefore MR/ MR ratioed W/L of MR will be playing an important role in determining the functionality of the of the level PTL level restorer.

We also use a multiple threshold transistors in the path and we also use finally we ended up with transmission gates concepts. So what is basically a transmission gate and how they are how they are but the final idea here is that it might look to you that PTL or for that matter DCVSL are

much robust as compared to CMOS less transistor count but until and unless we have very strong reasons to go or all these types of networks still complementary CMOS technology which we have used till now is the nest technology and complementary CMOS design is a most preferred design.

So rather than using past transistor logic or even gate transistor logic so it is better to use a previous case which we developed right the cost we are paying for it is is a lower transistor count but the cost we are paying for it is that we need to have signal complementary bars it is become a ratioed logic which was not earlier and you also have a problem of reduced noise margins. So with this we finish of the concepts of past transistor logic and how to restore the levels of past transistor logic right. We will do in the next module what is known as dynamic logic so we have finished this static logic right and we will do dynamic logic after this one thank you very much.