CMOS Digital VLSI Design
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Module No # 04
Lecture No # 17
Combinational Logic Design – VI

Hello everybody and welcome again to the NPTEL online certification course on CMOS digital VLSI design we will start the fourth module of our block which is basically combinational logical block. Before I go forward let me recapitulate what we did earlier to give you an idea where we are moving in this module. In the previous module we had looked into the concept of basic logic how a logic works we also looked into DCVSL logic which his basically switch logic we also so it is relative advantages and disadvantages and we saw it is working principals. So just to recapitulate the whole thing let me discuss with you simple and simple AND – NAND this thing.

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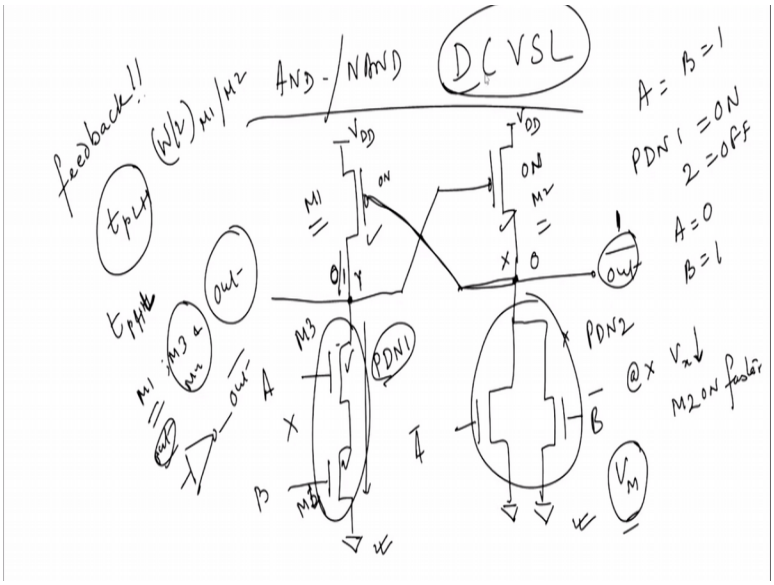

So this is basically AND and NAND this is DCVSL right as I discuss with you the pull down transistors will always be complementary in nature and the pull up transistors will be consisting of a single PMOS transistor right and you will have this NMOS here and you have this input A and this is input B. So this is behaving as NAND gate as you can see this will be 1 out here this

will be out right and then we will go from this side we have two parallel conditions here and here we do like this and let me put it like this and name it as A bar and name it has B bar right.

And let name this as your out bar and then we will do our feedback connection here which means that this will go like this and like this and this and then this will go like this and then this and then like this. So this is your VDD this is VDD and this is your NAND logic and this is your AND logic this is give your NAND logic in the output side. As you consider therefore this is basically a feedback mechanism.

Feedback mechanism which we have discussed in the previous term now if you look very carefully if A and B are both equals to 1 let us suppose this AND gate will be ON right so this is suppose we refer to this as PDN1 and this as PDN2 right then PDN1 will be ON N will be ON 1 will be ON and PDN2 will be in the OFF state. If this is ON this voltage will be pull down to ground and therefore this will lash out to 0.

Now this becomes 0 this is ON state and when this is ON this goes to high state and therefore this is approximately equals to 1. Now if the reverse is true that either A or B say A = 0., B = 1 then you can very well see that this pull down network will not work this will work and therefore this will be 0 if this is 0 this will become ON and then this will becoming to 1 right.

So this is basically a switch logic but please understand one basic fundamental principle here that the PMOS basically either feedback loop with the output of the previous block which means that the voltage swing say let us suppose this is X this is Y then if the voltage swing at says X VX is swinging very fast from 1 to 0 it implies that let us suppose this is M1 and M2 this implies that M2 will be switching on at a much faster phase right.

So therefore this is also known as a feedback logic right and it is basically a cascoded feedback logic and it is always a differential signal which means that PDN1 and PDN2 cannot be switched ON at the same instant of time either the two networks will be OFF and I will get a perfectly differential signal at out and out bar with this knowledge let me give you a basic idea about tpHL and tpLH.

If you look very carefully in this case of DCVSL the value of tpLH which is low to high will depend upon W/L of M1 and M2 right M1 and M2 here why because this is basically your transistor which is a PMOS transistor which is responsible for charging this node to higher value which is VDD. Which implies that depending upon the W/L ratio of the pull up device in this case only pull up device which is PMOS my tpLH will vary or my tpLH will have varies values available there.

Whereas tpLH right low to high sorry tpHL which is high to low will depend upon the type of configuration you have in the pull down network. So if you are using for example network which is PDN1 which is NAND gate in which both the transistor are in the series to each other than the resistance will get added up and your tpHL will high as compared to it similar minimum size inverter.

So therefore tpLH in this case is only depending upon the value of your PMOS W/L ratio aspect ratio whereas the pull down case it depends upon the aspect ratio of the NMOS transistor. Another important term which you should know about this is how do you design your switching threshold right switching threshold. Switching threshold primarily will depend upon the relative strength of M1 and these two transistors in the pull down case.

So this is suppose M3 and M4 right M3 and M4 then the relative strengths between M1, M2, M3 and M4 together this and this will determine the value of VM. So if you are pull up transistor which is M1 is stronger means larger W / L ratio is compared to the effective pull down ratio then the VM the threshold voltage will be switching threshold will be switching to the right implying that you're your noise high noise margins will be high.

Whereas if you pull down is higher it will imply that your VM will be shifting to the left and there will be very fast switching taking place in that case. So with this knowledge or which this idea we have we can formulate a policy here advantage again is that as I discussed with you there will be very small power dissipation in this case and functionality will be there we are achieving our functionality approximately 2N + 2 where 2 is basically these two MOS inverter is available to me.

Therefore the transistor ground is relatively less as compared to other one and the third thing is that I am able to get both out and out bar from the same circuit right. So I am able to get out here as I am able to get out bar here from the same circuitry otherwise I would have to actually use a static inverter in order to achieve out bar from out right and that we are not doing it here right and therefore the that is an added advantage which means that you have a gain of two transistor in this case in terms of lay out area.

With this we have finished the concepts of DCVSL or we have understood why is it very important as compared to other case though you can see therefore that DCVSL or for that matter any logic digital logic looks very interested as compared to CMOS invertor but the robustness of the CMOS invertor cannot be compromised for any of the logic is discussed on. Robustness in the sense it is basically an non-ratioed logic and therefore it is always give you an output independent of the type of W/L ratio choose right.

Same thing applies for DCVSL also right so this basic concept you should be aware or you should be able to handle. Let us now come to the module which is available in our hand at this point of time and that module is on the combinational logic design. So we move forward and explain to you what is the outlet of the talk. Till now please understand that we were all giving input to the gate of the MOS device with we were discussing in digital VLSI design right and we were trying to find out the current between source and drain right. Can we do some small changes in the way we integrate the input signal with the chip or with the device itself.

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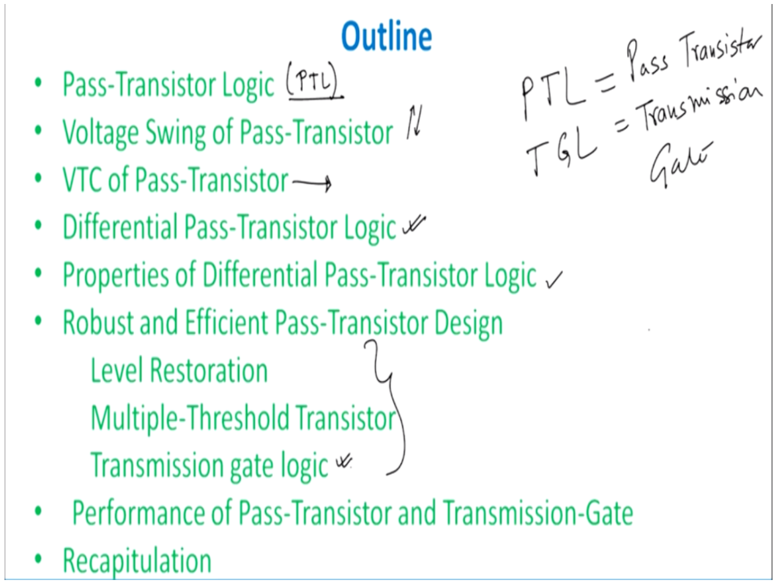

And that is where we first encounter with what is known as a pass transistor logic also referred to as I am sorry also referred to as PTL or pass transistor logic also refers to as PTL this is pass transistor logic. We will also look into the fact that if this logic is applicable for any digital design what is the available voltage swing does it go to VDD and to ground a the same instant of time.

We will look at the VTC of the past transistor how close it is to how far is it to the CMOS inverter of as you know of it then we will be using what is known as the differential pass transistor logic. So this will be a differential pass transistor logic the same concept the only difference is that we were using the previous case differential logic where the input or the input bar was available here we will see that how using input and input bar I am able to achieve out and out bar available to me using a pass transistor logic. We will look into the properties of it and then therefore we will understand what is the advantages of past transistor logic and therefore methodologies available to us which help you to basically remove the problem of past transistor logic.

Finally we end up with finally we end up with transmission gate so you will be looking this module to be pass transistor logic is the first module which we will be looking into. Then we will be looking at a voltage swing of the pass transistor logic VTC of the pass transistor we will look at the differential past transistor and then methodologies of pass transistor logic which is level restoration and multi VT transistors and finally we end up with transmission gate logic right.

So two logics we are looking currently VTL and TG right transmission gate so two logics we will be looking in this TGL. So this is known as the past transistors logic right transistor and we are looking at transmission gate logic. So both have their own advantages and disadvantages and they are working fine for most of the cases.

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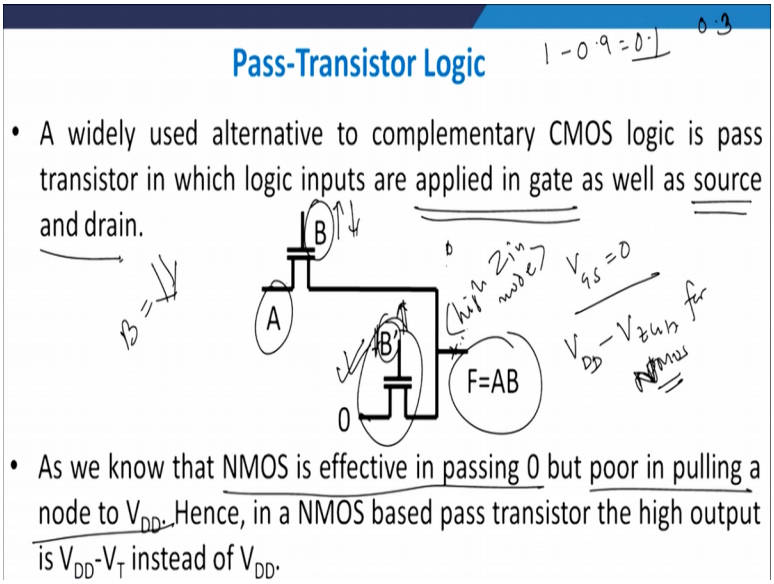

Let me explain to you what is pass transistor logic looks like or how is it different from the logic we have to find till now. As I discussed with you the starting of the combinational block was a module was that in most of the cases till now you are actually giving the voltage or the gates side of the MOS device right and as the gate voltage was exceeding the threshold voltage of the device you say that the device is switched on and therefore there is a current flowing between source and drain that gate voltage at which the reversion layer is formed near the silicon-silicon dioxide of an enhancement mode MOSFET in case of N channel we define that to be as threshold voltage right.

So this basic 3 or 4 definition should be clear to you as we move along this is the first time you will see where the signals are actually applied to either the source or the drain of the of the of the pass transistor logic. So the signal which is variable block the signal is basically a variable block is applicable or is applied to the source or drain of the block right. Now let us see what the problem areas where the advantage of.

So what we are doing is we are applying to the source right and in some cases we are applying to gate. So we are applied to the signal to both source and gate as well as drain. Drain is generally do not apply but apply the source and gate right and for most practical purposes source and gate as I go and applying the voltages if they are same then gate to source voltage VGS will be always equals to 0 right and therefore you will never be equal to switch on the device.

And there as to be at least difference of one threshold voltage in order to switch on your transistor in a condition where you are working with the pass transistor logic right. As I discussed with you in the previous turn that NMOS is the very good transmitter of 0 but a very transmitter of 1 right

So if a NMOS is effective in passing 1, 0 but a poor in pulling a node to VDD and we have already referred why was the voltage output becomes VDD – Vthl right this becomes VDD – Vthl for PMOS case for NMOS case of for NMOS right for NMOS case see if higher if you are using a high VT device or high threshold voltage device you might end up having the value of your node voltages to be even lesser than the switching threshold of subsequent block right.

Suppose VDD is 1 volt and your switching threshold is a 0.2 volts or 0.3 volts and you have used up a VT of 0.9. So 1 – 0.9 is 0.1 so 0.1 volts might not be able to drive the next transistors so that is the one major area but in past transistor logic we ensure that we get signal both source and as well as to the drain end so we giving signal A to source end and the drain end here right. I will explain to you what do you the signals do but moving ahead let us see at this point if B is high let us suppose if B is high then A will suppose I will give you an idea.

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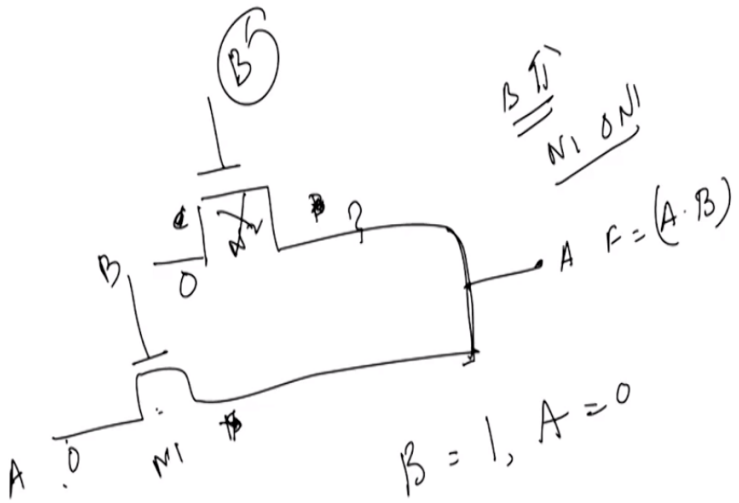

So I have a transistor here we have also have a transistor here right and this is this and what is happening is that in this case your this is A and let us suppose this is B fine this C and this D obviously this will be also B because both are having same potential. So from electrical point of you this two will be B fine and they will be a signal A here and this will be signal B here. So this will be a signal here A and B suppose B is high so let me just give you an idea here that you have got this and you have got this and this is signal let us say 0 and this is V prime right signal 0 and this is B prime right this is become.

So let us suppose B = 1 and A = 1 then you will safely say or I can safely say since B = 1 transistor N1 and this is N2. N1 is switched ON right and this A this is 0 let us suppose transmit to this source point right fine. So since it is a 0 and it is an NMOS it can easily transmits from this point to this point so I have got A bar here coming into picture because it is low. Similarly if B is high B bar is low this will be cut off and therefore this will behave as a open impedance state right.

So going back to the previous diagram here which you see in front of you I get the output to be equals to F to be equals to A fine. So this is what is known as the pass transistor logic what is pass transistor logic? That this logic allows you to insert signal not only to its gate side but also to it is source and drain side now while doing so what happens is that that when you are actually putting it in the source or drain side so on the source side using 1 then you actually lose 1

threshold voltage moving from the source to the drain of the MOS device and that losses quite critical and we should not do it at a latest stage.

But at this stage for your understanding purposes let us suppose that has happened and therefore I get what I get F = A dot B which is nothing but the threshold the AND gate Boolean expression available to you. You can have well asked me why are you using this B prime transistor which is this one because if even I do not use it I will still get F = A dot B right agreed.

But let us see what the problem will be when B is low when B is low and if this is not present then this node will be connected to a high impedance node clear. So as a result there will also some sort of issue corresponding to noises. So therefore in order to remove this problem that my voltage terminates at a value which is basically non zero implies that they will be a you will have some problem here in terms of impedances.

The impedances will be typically low in this case in order to remove it we have this transistors which is in front of you right. So when B is high and this is B bar is low and automatically A dot 0 will be giving you 0 and so on and hence so forth. Similarly if A = say B is low then this will be high right sorry when B is B bar will be high and then the 0 will be transmitted to be here. But please mind that 1 will be transmitted as VDD – VTN and 0 will be transmitted as mode of VTP.

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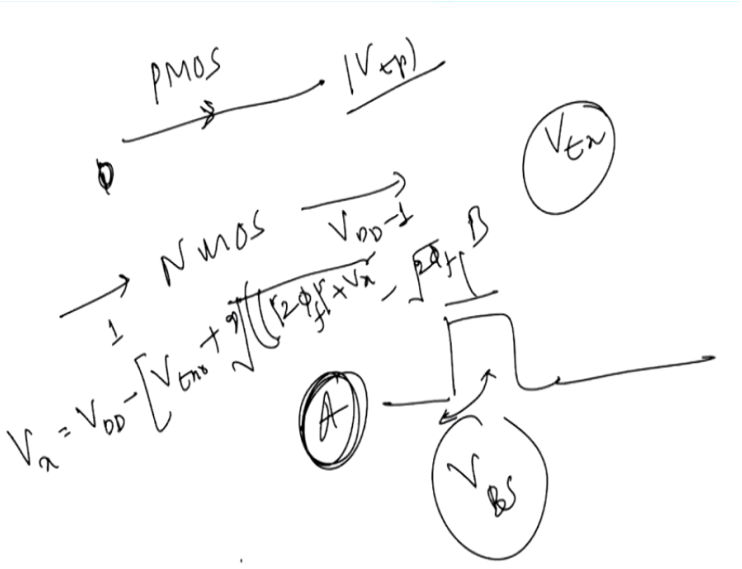

So let us begin very clear for pass transistor logic the overall impression is that when you pass at PMOS or you have a NNMOS right and If you pass through it in NMOS 1 we will get VDD – 1 volt right in if you are using a PMOS I get if you if you pass 1 through it and you have not paid this thing if it is 1 is moving from this direction this will actually look as or a suppose 0 is coming from here then there will be mode of VTP available here.

So there will be a change in signal with this knowledge we come to the point that you have this pass transistor logic. The second problem with pass transistor logic the problem is that if you change A B as I discussed with you just now that I have got A and I have for B right A and B and this going like this this is source. So what is happening is but if you go on changing A right and VBS value bulk to substrate or bulk to source this potential goes on changing and then VBS changes threshold voltage of the device changes.

And therefore it is written as I will tell you as how it is written Vx Vthl is VDD – VTN0 + gamma times right twice Phi f –Vx twice Phi x + Vx – twice Phi F root over. So if you look at the expression here again as I discussed with you in the previous turn that this holds good why because as you vary A this is substrate to source bias which is VBS varies till now it was varying it is applying gate voltage and there was no connection direct between source and the drain or the gate.

Now the reverse is happened this is direct connection between the source and the substrate and therefore when you vary the source value voltage the substrate value voltage also as to shift so that your body bias effects as 0 and that is a why you have shift the value of body bias voltage right and this is this is the reason why I have to shift it to a drastically to a low value. With this basic concept let me come to voltage swing in a pass transistor logic. Let us suppose I have got two transistors in series to each other which means that I have two transistors here.

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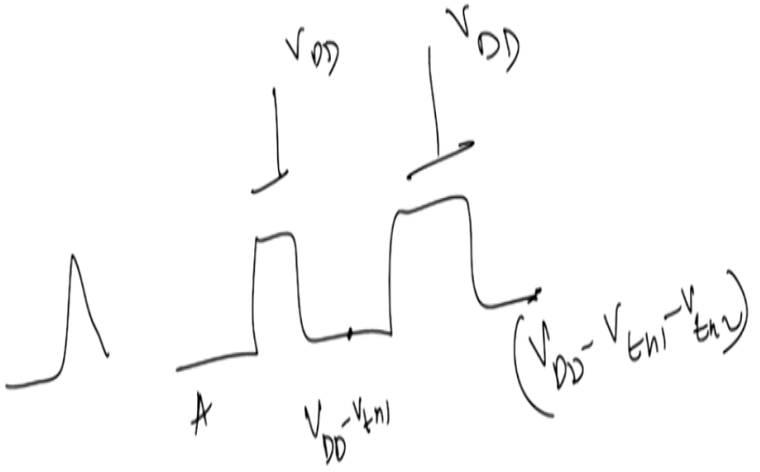

Which is let us suppose this A so I have got A here this is VDD then the value of voltage here will be VDD – Vtn1 and the value of voltage will be VDD – Vtn1 – Vtn2 right. So as you start cascading from source to drain there will be one potential drop as you move from left to right. And if this change is typically very long you also might have a problem that all the voltages are actually dropped within this period of time.

And you have only left with all the voltages are actually dropped within the period and you are only left with the few voltages by which you cannot even it means formulate the next fan out that is the major problem of a pass transistor logic. Now if you if you therefore understand or therefore get the principles correct let us look at the response of NMOS charging capacitor.

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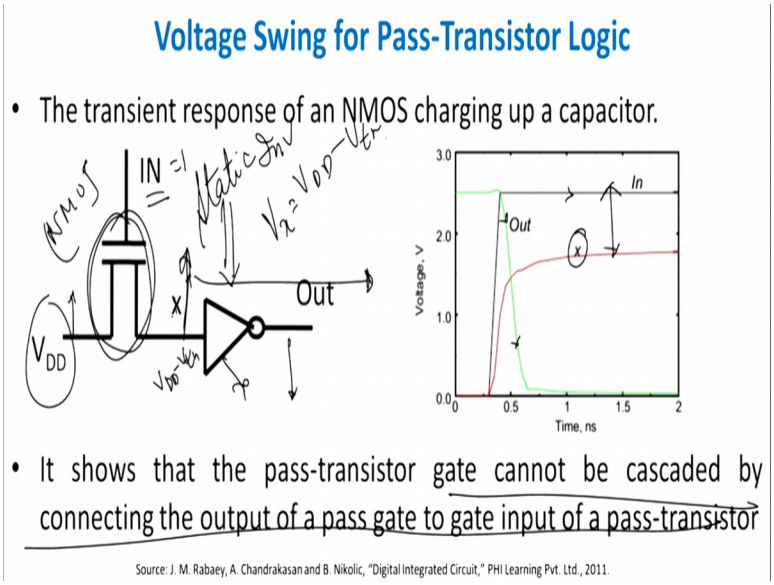

So I have got NMOS here right and I have a static inverter here so this is static inverter static inverter and I have got a an NMOS here which is acting as a source here. Now if NMOS is high this goes high and remains at VDD – Vtn when IN = 1 fine when IN = 1 it means a gate voltage is almost = to the threshold voltage of the device then x Vx will be always = VDD – Vtn of a Vtn right where Vtn is the threshold voltage of this PMOS fine.

And then you apply a then you apply at CMOS inverter and this CMOS inverter will either bias it to 1 or 0 depending upon the value of the threshold voltage which you are chosen. As you can see therefore that when input goes this is my input so when input goes high from 0 to 1 the output will start to fall down because when this goes 0 to 1 so this increases this increases primarily means this decreases so the signal actually the output decreases output decreases here right.

Now what happens is that initially when your VDD which is this one was say very small value and it is increasing slowly and slowly and the value of x also increased as per the rate of the value of x will also increase as per the rate of the VDD. So VDD is improving slowly and slowly Vx will also improves slowly if it is moving very fast it will move very fast and so on and hence so forth.

So it shows that the transmission gate cannot be cascaded by connecting the output of the pass transistor to the gate of the pass transistor. As we just now discussed therefore directly feeding

the output of a task gate to the gate input of the pass transistor is not a very good idea and the reason is that you will always a voltage fall at intermediate nodes right. So therefore if you allow this to happen at least 3 to 4 more slides, 3 to 4 more cascaded blocks this difference will be so large and we would be able to handle or get a clearer picture of the signal of the signal processing which has done right.

So this is one of the major voltage swing limitations of sort of pass transistors logic is all about. Now let us look at the VTC, VTC is the name suggest is basically voltage transfer characteristics.

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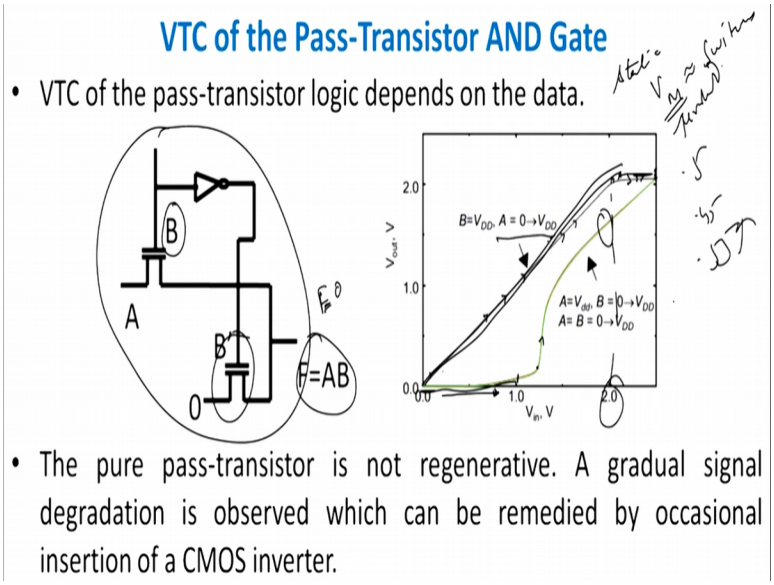

And you apply a voltage here A you have a B pass transistor here you have B prime is pass transistor and you have 0 here right F = A into B is the logic which you want to find out. Now let us suppose B was equals to VDD and A goes from 0 to VDD so what happens to the output? Output starts to rise as per the value of the VDD let this VDD is to 2, 0 2.0 volt 2 VDD right. After this what has happened is all your transistor switched on and enter into saturation region there is no one to play with and therefore the current is actually be getting constant independent of the applied voltage.

This black line in front of you which you see here is the line which shows you that when VDD = V out then how does the output voltages varies with the input voltage. Now obviously as you can understand they will be exactly equal as you move across. So you giving an input of two volts

and you get the output of two volts giving an input of 1 volt you get a output of 1 volt please understand the pure this thing I need not explain very straight forward as simple.

So if B is known to me the complement of that is fed into this NMOS and the output of this is taken here F = so A dot B. So you see you can have various differential logics available to you in order to look into the pass transistor logic of a pass of ratioed logic gate.

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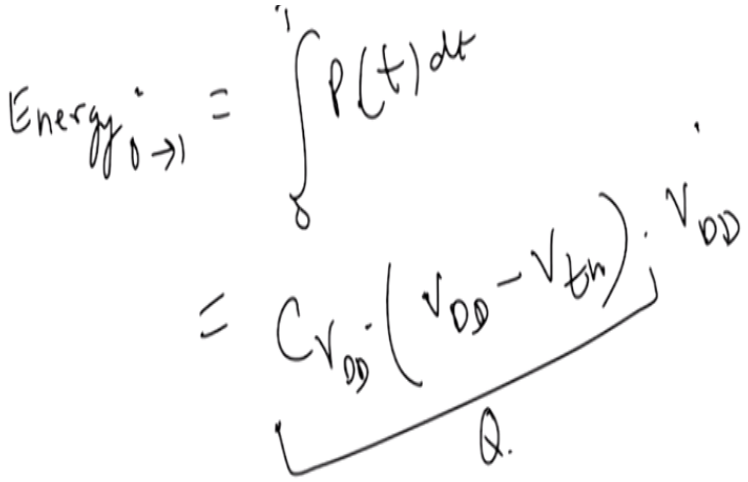

If you have energy say you have got an energy right energy what you define energy? The energy is defined as 0 to 1 why because that is the cycle when you are charging the output path and then therefore that is absorption of energy integral 0 to TP T Ptdt. So if you solve it and get the value I get C times VDD divided multiplied by VDD – Vth right. So the energy = Q so Q = C into V Q = C into V and so this will be VV square this multiplied by VDD square.

So this is Q into Q = C into V right and so this will be the total charge and that multiplied by VD will give you the charge per area will give you sort of current flow to the device itself from 0 to T time frame. So this is one thing which one should be pretty careful while choosing the type of gate. Let us look at the VTC as I discussed with you this is the first VTC after a particular point it remains constant reaches the maximum value of approximately equal to VDD the current flowing through VDD is first suppose 1 milli Amp right.

So let the current raise to 1 milli amp and after you have done that then you start doing the manipulation or next stage of manipulation. With this knowledge you have gained till now we see that as the input goes from 0 to VDD everything else remaining constant the value of the output voltage also varies linearly as the input voltage till particular point this point after this it is almost independent of the linear voltage sorry it is not having a any gate voltage variation.

What happens quite interesting when A is fixed to 1 right and B varies from 0 to VDD so B varies from A is fixed to 1 B varies from 0 to VDD when it is 0 this is basically 1 so this is cut off and this is 0. 0 means this is okay and therefore I will get some higher value at this point this is pretty interesting and pretty remember it was so therefore as the V in put value goes on increasing here right at this point till 1 volt which is possible switching the threshold voltage of the NMOS since it does not switch ON.

Therefore this is almost 0 and therefore F is almost = 0 and therefore this green lines shows the that value it is almost 0 right. Because you do not have anything to pull or push at V in = some value there is sudden switching on this transistor and as a result the voltage across its starts to becomes higher and higher and then it finally reaches value because of neutrality right. Because of electrical neutrality you will always have this value equal to the value of VDD which you choose at the initial start of the of this program.

Please understand this is not regenerative which means that there is no feedback loop available to me once the voltage has been developed charge as been dumped either it goes to ground or it is of no use typically to the electronic industry. What another important point is that see for the for this case when A was equal to 1 and when B was going from 0 to 1 or when A and B both where going from 0 to VDD in both the cases I see that the voltage level output voltage level is very less restored or very low value as compared to the input voltage.

Unlike the case of the first one unlike the case of the first one so we try to find out the reason why such a phenomena has got a value of voltage which is slightly different from the initial value of voltage which we have given at least the feedback voltage. So in order to make it again a latch on to its value of VDD let us suppose we just have to insert a CMOS inverter static CMOS inverter.

Whose VM is almost equal to the switching of the device switching threshold of the device if your VM is much larger as compared to switching threshold it has got no meaning if it is almost equal to almost less than that primarily means that I can still have a one issue or one case in which we will have some variation taking place in the output side this is what we get. So switching threshold it is 0.5 volt and you are able to achieve 0.45 it is of now use.

But if you put 0.5 there will be sudden suddenly switching on the device so I need to therefore so you see the signal is degraded here and I need to improve the signal levels right. So that is what it is there? let us look at the another type of pass transistor logic and that is known as the differential pass transistor logic.

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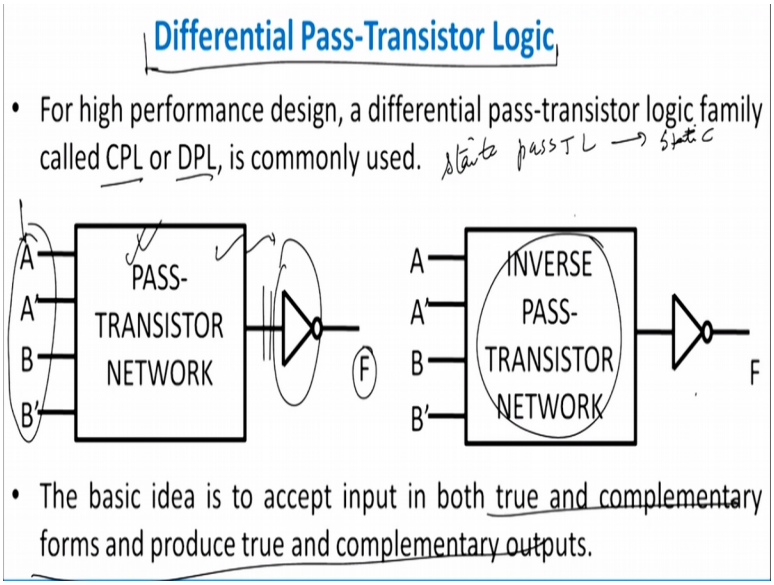

This is known as a differential pass transistor logic also known as a complimentary pass transistor logic or dual pass transistor logic and how do I do it get the inputs I also get it complement available to me. So A and A bar both are available this is my past transistor logic I get an output I put an inverter here and there is specific reason why want to do that after I put an inverter I have F logic available to me.

So the output logic F will be direct negation of the total input logic depending on the past transistor logic which you are using. Now what we are except is that to except the input in its primary as well as it is complementary form and produce true and complementary output. So the

job is to except data and its complement and release output ends complement right. So this what is basically a differential pass transistor logic this differential pass transistor logic we can have two types if it is static pass transistor logics then there is a reduce noise margin.

So if I got a static pass transistor logic PTL transistor logic then we define the transistor family to be what is known as the static family right and the second thing is that differential pass transistor logic you will have one important property that it is design pretty simple the is a modular design. Modular design primarily means as I discussed with you in the previous turn or may be in the today's previous lecture that if you look very carefully here it is a modular design.

So you have got this and this already built if you want to shift it to a triple gate simply add another gate you will get a triple gate. You want to add another gate here please do that add another gate here for all practical purposes right. So since it is modular it is more of a plug and play phenomena of VLSI design which is available to us let me come to the therefore I can have pass transistor logic as I discussed with you right and I can also have a inverse pass transistor logic.

Inverse pass transistor primarily means that just the reverse will be coming out you need to repeatedly change it is value to achieve the right value out of it right. This is one of the what we got from our this thing the idea let us look at this phenomena here let us look at this basic idea but since true or since the original signal and its complementary signals are inputs are available so and extra few circuits are available why?

Because till now you are static got only okay only I have got a signal and I can manage with them. You do not have signal agreed but you also had the complementary of the signal. This complementary of the signal adds the signal count to 2 if there are two input gates available to me or any number of independent of the number of gates depends upon the variable of the Boolean expression.

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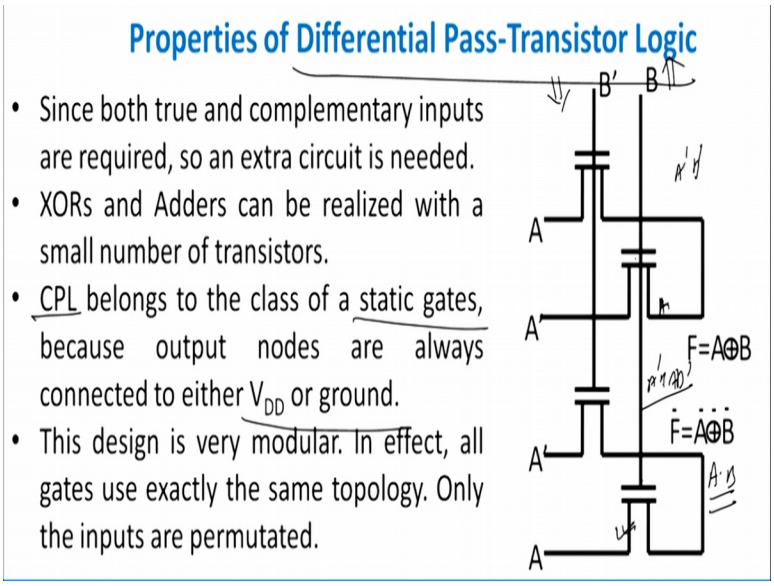

So the Boolean expression as got 3 inputs then it will also have a 3 complementary inputs fed into the system right XOR's and Adder's are generally utilized using differential pass transistor logic principals so this is also known as differential pass transistor logic complementary pass transistor logic which is this one belongs to class of static gates right.

And why because this either connected to VDD or ground and this very important when we discussing either of the dynamic logic or for that (()) (34:58) static logic that you have to two conditions when output is connected directly to ground or to VDD in that case impedance is typically high and if it is directly connected to one of in the intermediate nodes incidence impedance actually reduces drastically right and this a.

So basically that is what we are trying to say that it depends upon this point so if you look this is B and this is A. So when this is B high let us suppose and B bar is low. When B is high what does it imply that this becomes ON and therefore I get A dot B available to me. So when B is ON I get this also to be ON and therefore again A as output and when this A comes back to this point or to this point I get A bar B bar I also get A bar, B, A, B bar all sets of combinations of A and B bar right.

But important things is that I can realize this pass transistor logic using XOR logics or using Adders also right and these are very important or very important issues which one needs to know. So we see therefore that a pass transistor logics suffers from primarily two to 3 important

points the first point is that it is basically high activity factor activity and therefore alpha is relatively larger and therefore you would not be able to have the activity factor reduced in this case.

The second if you remember was that the voltages levels was not restored to its original value which is VDD it is falling much below this. So I do require a sort of circuitry which will help me to enhance the value of the voltages at intermediate positions.

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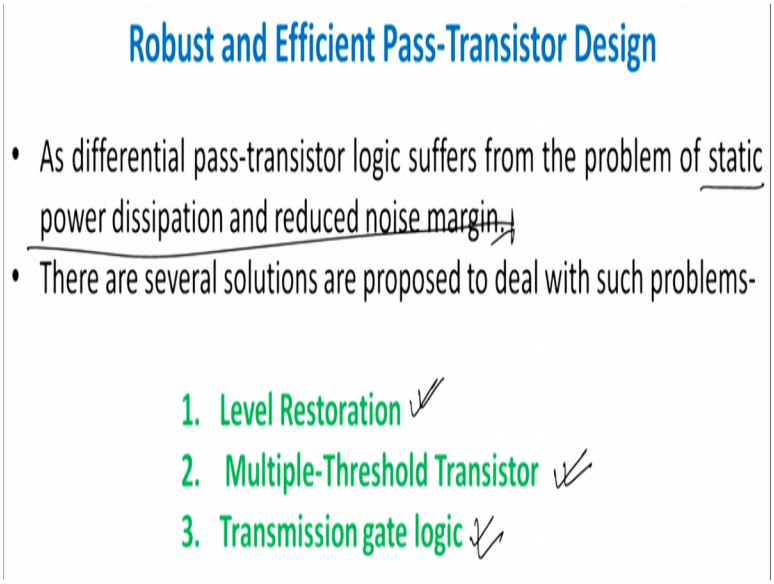

So let us look at it is suffers from basically static power dissipation and reduce noise margin right so let us see how it works out. So there are three techniques which we can improve our past transistor logics one is known as level restoration another is multiple threshold voltages third is the transmission gate itself right. We will look into each one of them individually so that you understand the working principle of each of them right.

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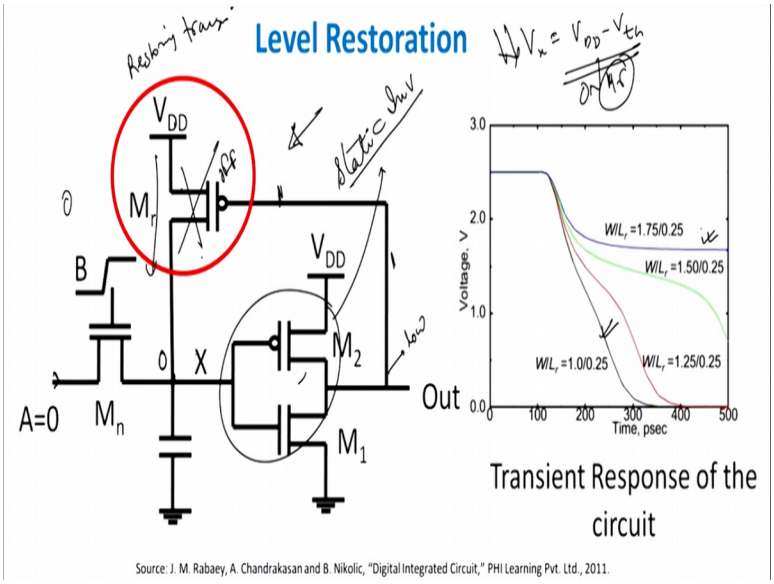

Let us look at the level restoration first technique to restore the value of voltages or currents in a typical pass transistors logic right this is typical pass transistor logic.

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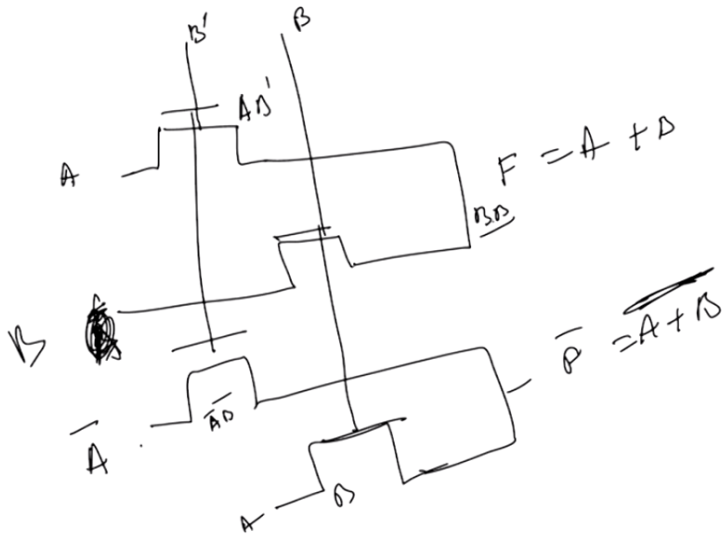

If you can see one more definition here I can give you for example if I am trying to buy a XOR gate so I get A so I get B bar right and this goes like this this this and then this and then you have got this in consideration say this is B bar right this is B and then this is B. So let us have this into consideration and then I am sorry once I will just make it again to give you a proper feeling of what I am trying to say.

So what I can get from here is that I have this this and then this is B and let us suppose this is A bar A bar and this is B bar here right and B here then I get F equals to and if I do like this right and if this is A so this is A and B right and this will give you F = A or B and this will give you F bar A bar + A + B whole bar right A + b whole bar and from here this is again drop here I can drop this one here this is A so this is A bar B bar A bar B bar this is nothing but BA so this is AB.

Similarly this is A bar AB bar and this BB right I have a OR NAND operations of a past transistors logic right and you can always manipulate this logic to achieve a much better to filing as far as this logic is concerned. Now so let us look at level restorer level restorer primarily means I will have a transistor which will restore the output level to because if you remember there is one threshold drop so at least one threshold enhancement should be there in order to make the fact that it should be nearer to VDD in that sense.

So look at the circuitry which is present in front of you and this circuitry on this this circuitry this in front of you we define so this is we have a static inverter here. So this is your static inverter right and which basically inverter M1, M2 is transistor we define MR as the restoring transistor right and MM is some load I am feeding the signal from here with A = 0 B going from 0 to 1. So when B was equals to 0 the output is neither is not connected to this this side and therefore assuming that nothing is connected I will have this to be equals to 0.

0 implies that this is an inverter this is 1 which again comes here as 1 and which is means that this is OFF state. But when A becomes = 1 right this point X VX will be VDD – Vtn this will become low provided this is lower than the switching threshold of M1 M2 and as a result when it becomes low switches ON the MR value and MR value this it become switches this VDD appears across this point.

So what has happened therefore is that whatever the small voltage drop was happening by virtue of a by virtue of a threshold voltages of a NMOS device you have been able to restore the voltage level by simply changing value of MI or by simply adding a extra transistor MR and trying to have this MR in series to the output node X right and trying to make this output node go beyond a particular point. Which particular point switching threshold of M1 and M2.

So the problem the whole issue was that if past transistor logic reduces the voltage to such a low level which is even below the switching threshold of the device of this this device then you are in a big problem right and you would not be able to switch the whole cells but if it is slightly will allow will make it switch OFF or ON and depending on that we have color you will have voltage at various points index.

With this knowledge let us see what happens if your restorer which is this is MR is basically your restorer transistor has got higher and higher widths. So the width is larger so this violet is the width higher width and this is the smallest width of 1 if it is got a higher width obviously the currents will be typically very large which is available to the currents flowing through this PMOS will be typically large in this direction and I will be able to restore the voltage sort of to an extent to a large extent.

So as the time increase from this side to this side as the W /L ratio becomes larger and larger as you can the voltage it is trying to restore also getting larger and larger right. So it was initially let us suppose somewhere near two volts now it is going down and down because as the time proceeds as a time proceeding in the output side this switches ON trying to pull this node to VDD higher the size of this width faster will it be able to pull right.

So VDD is 2.5 it will trying to pull so it was 2.5 initially now it falls down it tries to achieve the value = VDD right. So this is some of the reasons which is very important that as you make aspect ratio larger and larger you end up having restorer transistor relatively weak and though it is able to pull to higher value voltages but it is relatively week to understand and explain right. With this we will stop here today just now and then we will start with the next which is multi threshold devices for our practical purposes thank you very much.