CMOS Digital VLSI Design
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Module No # 04
Lecture No # 16
Combinational Logic Design – V

Hello welcome back to the combinational logic design module 5 for the NPTEL online course and CMOS VLSI digital design. In our previous module we had looked into the fact that how can we reduce the dynamic glichting what is the meaning of static glitching? How can you reduce the value of alpha and therefore the power dissipation? We start a new topic which is basically a ratioed logic we will start with ratioed logic now and the ratioed logic is something like this that means as I discussed with you in the earlier cases that CMOS inverter from your earlier if you look back at earlier days that when we are discussing CMOS inverter.

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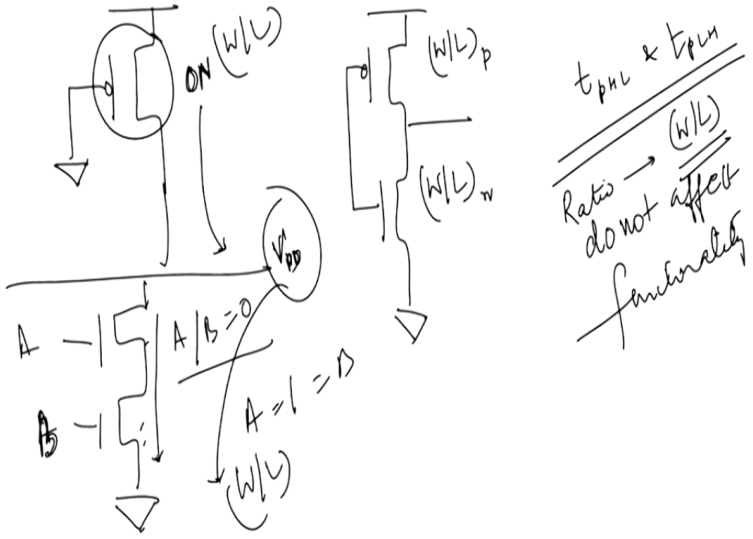

In that case your you had a PMOS and an NMOS and a the values of these aspect ratios W /L of P and W / L of N where primarily responsible for giving you the value of tpHL and tpLH right low to high and low to high transitions right and it depend upon the pull down and pull up capabilities of these devices and we also saw that if it is if the widths of PMOS is made width of NMOS is made twice as that of PMOS.

I would be able achieve almost the same value of tpHL and tpLH the reason being in mobility of electrons is approximately 2 to 3 times higher that of electrons of that of holes therefore you have to make a PMOS more widen to make it resistance smaller and therefore pull up will be equals to pull down. Now ratioed logic primarily means that all those logics in which the aspect ratio values W/L values do not affect the functionality at least. We define that to be as the ratioed logic do not affect the functionality right so it does not affect the functionality of the logic design we define that to be as ratioed logic.

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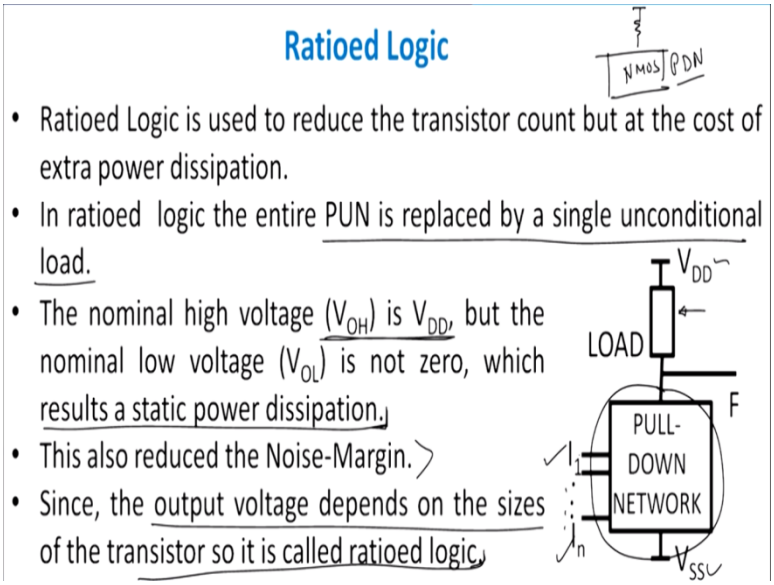

So as you can see the ratioed logic is one of the methodologies which people have used sort of Pseudo NMOS technology is that I will have a pull down network here as you can see this is pull down network then right and the pull up network rather than I having a perfectly complementary block as earlier will be replaced by a simple PMOS block right. A PMOS in always ON state now I will just show you what do I mean by that.

For example if the pull up logic is something like this it will be PMOS is always connected to ground and whatever will that the value of NMOS will let us suppose something like this that I can safely say that this is actually behaving like NAND gate now why because this PMOS this is basically width its gate always grounded this PMOS will always be behaving as an ON state right and therefore depend.

So if it is ON state it will be VDD for what either A or B equals to 0 output will be always latch to VDD right it is just like a NAND gate. Depending on the values of A and B therefore depending on the values of A and B so A and B are both equal to 1 right this VDD will try to pull down here but then there will be relative fight between the pull up case this W/L of this one and the total W /L of this one so that will so this VDD here will be pumped by this resistance and this VDD here will be discharge by some of these resistances.

So now what I mean to say is that if the pull down network is stronger I would expect to see that my output will go to 0 and if my pull up network is stronger which means the W / L ratio is larger I would expect to see that it will latch to the value of VDD whatever will the value of A and B. Which means that typically in such a scenario you should try to make your pull down stronger as compared to pull up when you want that output go from high to low right.

So this was the basic concept of a ratioed logic in which my pull up network as you can see is replaced by a single unconditional load. So PMOS in the ON state is basically behaving as a load so I have a resistive loading so I have a resistive load here followed by the NMOS block here right this is NMOS block which is the pull down network it is available here. So I have a I1, I2, I3 N input available and this VDD and VSS are the two higher and lowest value.

Now the idea here is quite interesting idea is that the output or VOH the nominal high voltage which is available to me is VDD obviously VDD because you are using a load here right so there is no multiple load as well as single load is there assuming that the drop across the load is very small all the VDD will appear at F and therefore your VOH output high nominal output high will be always latch to VDD.

But the nominal low ideally should be equals to 0 but it will not be a 0 because there will be a relative fighting between the pull up network and the pull down network and therefore it will depend upon the relative strengths of pull up and pull down network right this results in a larger value of results in a static power dissipation so your static power dissipations is higher in this case. Further your noise margins also lower the noise margins which you see are also lower if you look at this very carefully.

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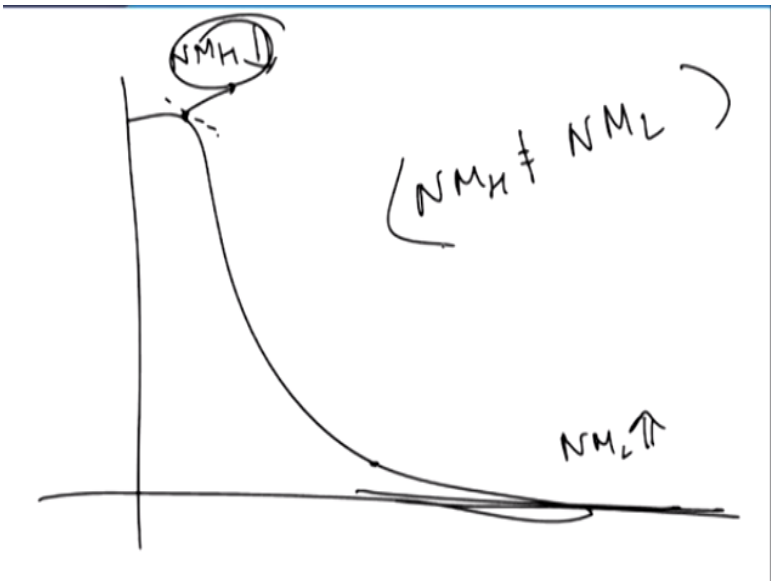

The reason being when you try to plot the voltage transfer characteristics for a network let us suppose your pull up is not very strong then what will happen it will (()) (06:09) like this and then it will go like this and then it will coming like this right. If you pull down is stronger it is looks something like this so what happens to your NMH? NMH is actually low why because this value is at this point is VOL, VIL and therefore so this is VOH approximately and VIL so NMH is low means high level margin is typically low.

Whereas low noise margin is typically high right and NMH is high but you cannot make NMH equals to is not equals to NML but since the probabilities of getting zeros and once in network is always 50% assuming there uncorrelated signals you always see that NMH should be as equal to NML but they are not at this case. So your noise margin gets reduced and becomes more noisy at least and not only reduce the asymmetric in nature and therefore they help you to reduce the values of and therefore you see output voltage in this case therefore depends upon the ratioed logic and therefore they are known as ratioed logic.

So what is unratioed logic a CMOS inverter for example is an unratioed logic depending whatever we are pull up W/L pull down W/L in most of the cases you will actually see the output either switching VDD or going to be out right and independent to W/L ratios where as in this case if W/L ratios are not properly fixed you might end up having asymmetric output characteristics right and as a result these are known as ratioed logics so this is basically the basic concept of ratioed logic.

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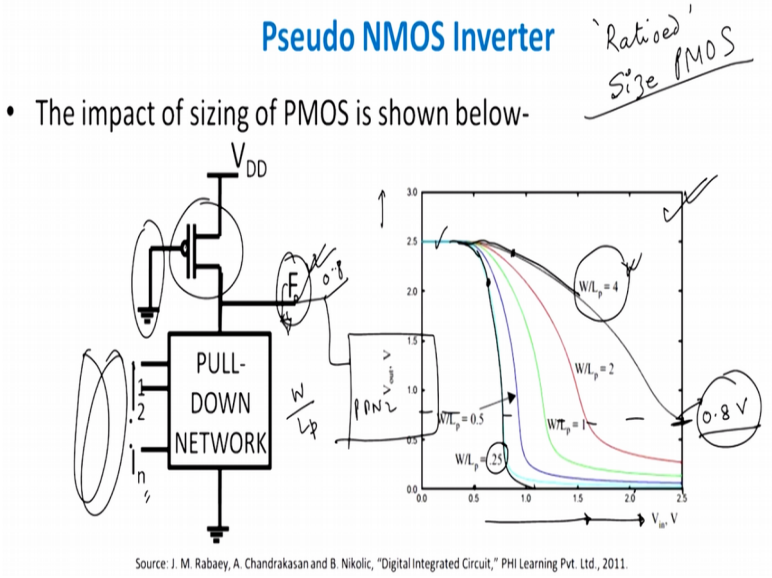

Let us look at the impact of sizing of PMOS inverter that is the reason we define this to be as a ratioed logic that it is basically depending upon the size of one of PMOS size of PMOS inverter the PMOS load this is the PMOS load this the ground the gate has been grounded so the gate has been grounded here and I have a pull down network with 1, 2, n inputs input at this stage. If you plug the VTC which you see in front of you the voltage transfer characteristics curve you see this is V out on the Y axis and this is V in on the X axis.

So V in what V in is basically your voltage at this point at V out is voltage at this point so you added the voltage at this point and you vary the and you try to get the value of voltage at this point at the output side. So you get C here it will obviously look like a CMOS inverter because when the input is low output is high when the input is high output is generally low. But see what happens when the W/L ratios of the PMOS starts to become higher and higher so where did you say 0.5 or 0.25 0.25 primarily means that it is strength is not very large it is got a smaller strength then what it does is that it does not allow the output to it allows the output to fall very fast.

If you look at the line blue colored line here with W/L ratio of 0.25 this is basically meaning that width by length of PMOS right similarly this is width by length of PMOS which is 4 times. So if it is 0.25 it means that my pull up is strong but effectively my pull down has become strong and therefore the voltage falls down very fast here right and it does not allow you to remain at VDD goes to 2.5 volt for longer duration of time.

So whereas when my W/L ratio is 4 you see this black line here it tries to remain at 2.5 for a longer duration of time primarily meaning my pull up network is getting stronger and stronger understood also why because W/L ratio is larger which means of the bits are become larger which means the resistance of actually reduced current is larger and it tries to latch to VDD for a longer V in period of time and it does not allow you to (()) (09:56).

Not only that if you increase your V in to allow larger value you will see that it does not go to 0 right it goes up to back to value of 0.7 to 0.8 Volts his is where the problem is when you have a ratioed logic that means though you pull up device is allowing to stay at higher values of VDD but then it not allowing you to go to the lowest value of your VSS the reason being that since W / L ratio are larger more current is flowing the output F is never latch to ground.

And therefore you will always have a residual value available to you right even when your V in is 2.5. So ideally when V in = 2.5 V out should actually go to 0 but no you getting approximately 0.8 to 0.9 voltage in the output side right and this becomes a difficulty or becomes a important issue when you actually start to cascade such type of networks. So let us suppose this F was supposed to drive another pull down network somewhere else right suppose it was PDN 2 it was trying to pull up.

Now ideally should go to 0 now it is 0.8 right now let us suppose it drives a PMOS whose threshold voltage is 0.5 so if would have been 0 it would have switched off NMOS of the next PDN pull down network. Now since it is 0.8 it actually switches on the network are you getting my point? At least that gate is switched on it should be switched off it is switching on so you see your output changes and it is by virtue of the W/L ratios that output changes not only that if you cascade it and try to find out a cascaded logic then you might end up having wrong interpretation of the values at intermediate positions.

So that is the basic problem of Pseudo NMOS inverter what is the basic problem is that you have a problem of this basic problem of reatioed logic that W/L dependencies is there. I will just plot for you the basic idea here and I will just show to you what do I mean by that.

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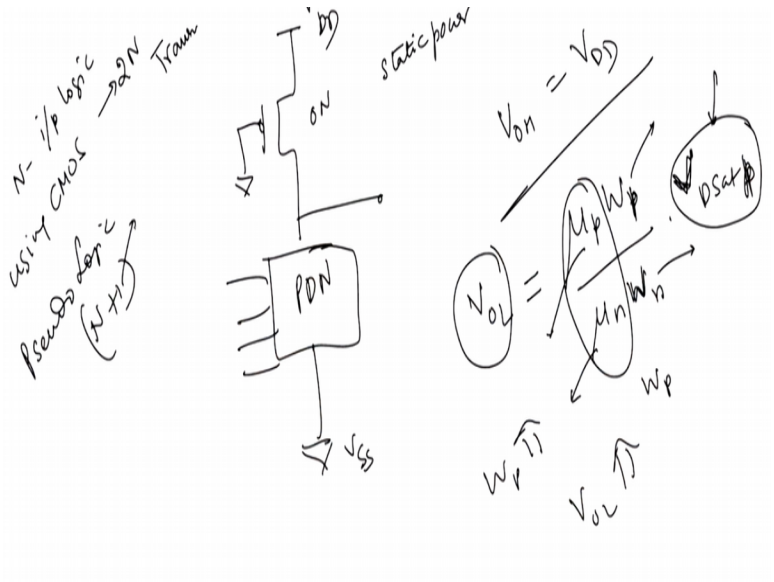

Now let us suppose I have got a PMOS inverter here and I have got PDN pull down network with multiple inputs and this is my PMOS which is basically grounded and therefore this is normally and therefore this is ON state and output will be whatever VDD this is VSS and this is VDD now we define VOH as I discussed with you will be always equals to VDD approximately = VDD because PMOS is very good puller of high voltage and therefore they all go to VDD.

But let us I will not calculate here but let us see what is the value of VOL? VOL will be given as MU p times Wp divided by Mu n times Wn into VDsatp where Mu n is the probability of holes Mu n is the probability of electrons Wp is the width of the PMOS Wn is the width of NMOS assuming that the lens are same of that the lens are same technology dependent and VDstap is that value of voltage at which the saturated you get a saturated output.

So it is basically velocity saturation is taking place and you get a velocity saturated output here available to me. I define that voltage to be as VD sat which is the constant value for the PMOS this thing assuming C here if you go on increasing Wp you are actually increasing value of VOL right and as a result as I was discussing with you in the previous term that increasing the value of VOL means this shifting this to the right and therefore noise margins are basically becoming higher and higher right.

And therefore you see it depends upon Mu p and Mu n constraints because they depend upon this thing Wp and Wn are the values which is given to you so therefore WP increase your VOL and

therefore your NMH Wn increase will reduce your VOL and thereby making your pull down stranger as compared to pull up and therefore your higher noise margins low noise margins will be better as compared to high noise margins right.

So what we can say okay let us keep our eyes closed and making Wp high and higher assuming Wp higher and higher and higher VOL and therefore I will get a very high noise margin much better high noise margin agreed yes you can make W/L higher but at the same instant of time please understand you will always have a larger static power dissipation available now right.

Why because when you make your W larger you the device remaining in the linear region or remaining in the saturated region both the devices PDN and PO and the 1 will have a larger probability will remain therefore longer time. So static power dissipation will be higher and you will get a larger steady power dissipations available in this case we will get steady power dissipations. This was what was your basic idea of Pseudo NMOS inverter and as I just discuss with you is therefore dependent upon the values of W/L ratio available to us.

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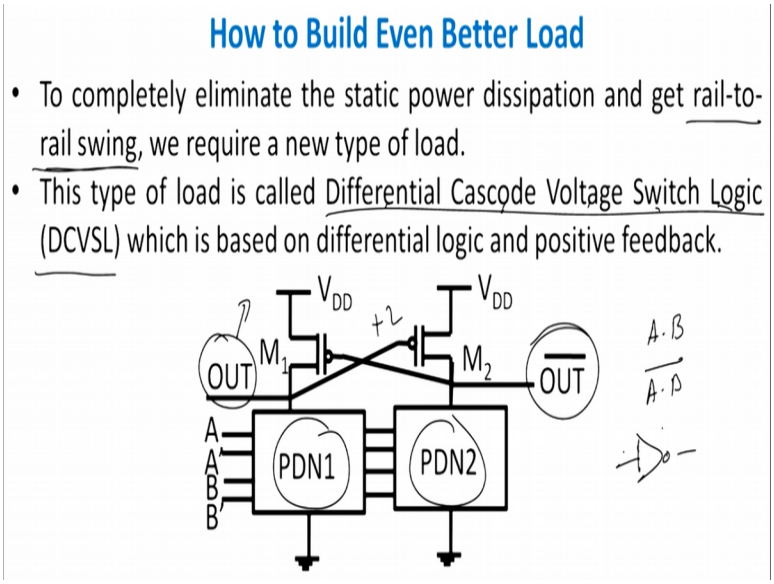

A very interesting picture came and that was known as the differential Cascode voltage swing logic also known as DCVSL so it is differential cascade voltage switch logic which you which is DCVSL right and it is based on a concept of differential logic and positive feedback. So basically I am looking at differential logic. Differential logic means that you will have perfectly

differential logic available which means that you will have the you will have out as well as out bar.

So you will have the Boolean expression if suppose you want A.B you will also have A.B bar available to you. So you will have always output available to you, you will always have out bar available to you in all the cases to completely see there is problem in the previous cases that you did not have problem at the ratioed logic was that to so just to give you inside to implement a N input CMOS logic you require two N transistors right I have discussed this point earlier also so if I want to implement N input logic using CMOS right using CMOS fully CMOS I required 2N transistors right I required 2N transistors.

If I do a Pseudo NMOS logic then I get N + 1 why N + 1 N is the number of transistors in the pull down capability an done is because of PMOS which is acting as a load right but what we get here now is that here we are trying to implement but the price I paid there was that the static power dissipation were higher and in my previous discussion earlier also had to told you that study power dissipation is rising and that reason is rising is that you are allowing since your want your noise margin to be high W/L is high you are allowing larger amount of current to flow through in a static case as a result your power dissipations are very high.

This was a method which was developed at certain cost will come to the cost later on but it was developed with the fact that there is all most 0 study power dissipation so there will be no static power dissipation here and we also get a rail to rail swing so full VDD to ground swing is available to us here right full VDD to ground is available. So what we do here is very simple and straight forward we make here so if you look back here this is your this one how it looks like that plot for you here again and again I will show to you.

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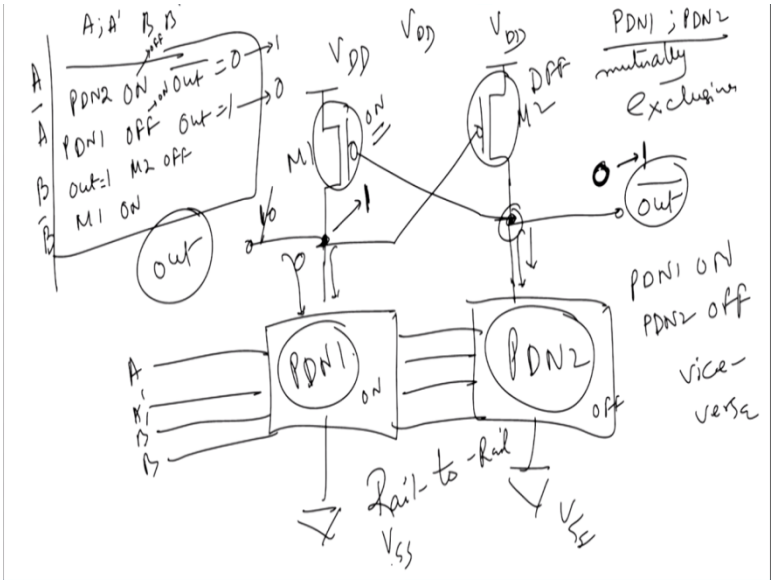

So I have got something like this that i have got a PMOS here right again I got a PMOS here right I have PMOS I have here let us suppose PDN1 and I have got here PDN2 I have got inputs available so let me show to you so we have inputs available here so this is your out let us suppose out bar right and this is let us suppose your out. So A, A bar say B say B bar right. Similarly this all the same network is going here also four lines are going here and then what you do you try to then inculcate this two you do a cross connection between the two right.

How do you do transmission used to simply like this so this is M1 this is M2 and this is VDD and this is your VSS of course VSS is connected here. So what do I mean to say that I have not only the inputs available but the compliment of inputs are also available. So if I would have worked with two inputs actually require my four inputs two basic inputs and two complimented inputs right.

So I have A, A bar, B, B bar as input my PDN, PDN1 and PDN2 were the two pull down networks are also defined as mutually exclusive they are defined as mutually exclusive. Exclusive means basically that if PDN1 is ON right ON PDN2 will be OFF and vice versa right. So we define that if PDN1 is ON and PDN2 is OFF or vice versa we define that to be as mutually exclusive network which means that out and out bar will always to opposite to each other as you can understand very well by now itself.

Which means that I will always get the logic and the inverse of logic visible to me in a DCVSL so as you can say therefore see an important point which was missing in the previous case was that at no point of time out or out bar will left floating it will be either connected to VDD or it will be either connected to the ground. So it is basically connected to a low impedance node at all instance of time for any of the values of A, A bar, B, B bar.

Let us see how it works out let us suppose initially let me assume that out was high right and out bar was low right out bar was high and out bar was low. So it was 0 here now out bar is so out bar out bar is 0 which means that it is connected so it obviously means that PDN2 was ON PDN1 was OFF at that stage and therefore this was 1 why 1 because this was 0 so M1 was ON now M1 was OFF this was OFF since this was OFF this PDN2 as ON as this was dragging this to 0 and I get 0 here available to me and therefore the logic seems to be okay right.

And now out bar changes to 1 let us suppose out bar changes to 1 shift towards 1 because of some changes in the value of A and A bar as 0 changes to 1 right. So there is now a relative so now you see this was ON right as it changes to one it means that PDN2 will go to OFF state now which means that this will go to ON state which therefore means there will be a relative relative sort of fight between PDN1 and M1 to bring this state out of 1 to 0.

So if we obviously it has to go to 0 means PDN1 has to go high and therefore 1 will come down and becomes 0 here right. But there will be so but when so this will only happen when PDN2 goes to OFF state right. So PDN2 so let me just graph once again the whole full feedback network this is based on positive feedback that let me give you an idea about what I am trying to say that let us suppose I have got A, A bar, B, B bar as the inputs available to me PDN2 is let us suppose ON then my out bar is equals to 0 right therefore PDN1 by dissipation will be OFF.

And therefore my out will be equals to 1 which effectively means that if out equals to 1 it implies that out = 1 will simply that my M2 will be OFF state right and M1 will be in ON state M1 will be in ON state because this was 0. So this is initial condition which is available to me now what has happened by some change in values of A and A bar and B bar this out goes to 1 right out goes to 1 but out bar goes to 1 as out bar goes to 1 PDN2 as to go to OFF state right it has to go to OFF state right.

As I goes to OFF state as I goes to OFF state PDN1 has to go to ON state as it goes to ON state this voltage will start to fall down and therefore out which was initially = 1 will not starts to go to 0. So which means that it is perfectly a sort of a feedback logic which why is that good? It helps you to speed up because the voltage here at voltage at out bar going down will actually help M2 to go on so you do want to wait for a quiet a long time and therefore this voltage will be from 0 to 1 very fast irrespective of the value of PDN right.

So this is known as the dynamic and DCVSL logic which is quite useful and this will also give you rail to rail swing as I discussed with you it will give you a rail to rail swing what is rail to rail VDD here and VSS here So I will get VSS to VDD swing between output and input directly right. So with this knowledge with this idea let me draw for you a simple NAND logic and NAND logic is DCVSL so it looks something like this that if for a NAND logic.

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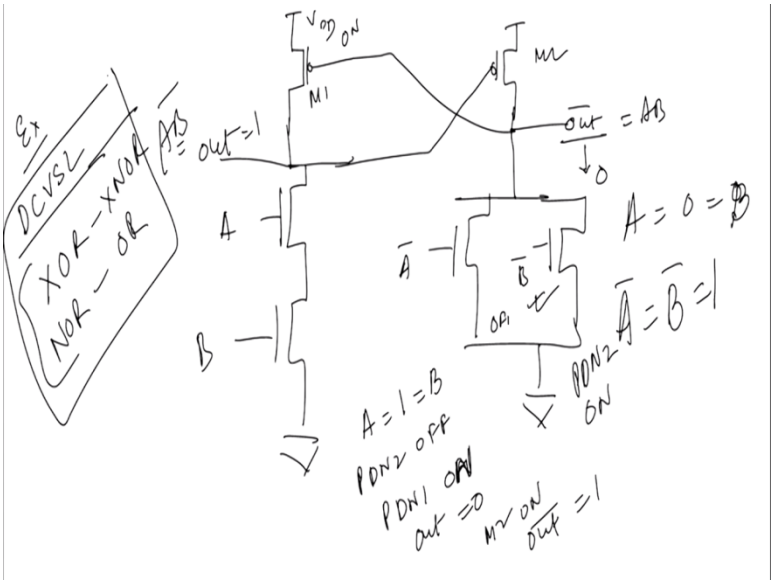

This is what I get right I have this this into consideration right and then it goes like this and so this is A right this is B this is your AND gate and then you have got a here B right AB and this is A bar and this is B bar from both are there of grounded here what I do is that output which I see this is out bar and this goes like this and this is connected to this value this value right and this is directly connected here and this is directly connected here fine this is okay. So I get output here and this is your out and this is your VDD fine.

Now so this will be AB and this will be AB bar and therefore whenever A and B are both A and B are both zeros when you are known that this network will get switched ON right both are sorry A and B are both equals to 0 implying that A bar = B bar = 1 therefore PDN2 switches ON right this is PDN2 it switches ON therefore out bar goes to 0 and it is goes to 0 this switched ON and this goes to 1.

Now and A and B was geos to 1 no need of suppose A and B then this switches OFF PDN2 goes to OFF state and PDN1 goes to ON state as it goes to ON state goes to 0 as out goes to 0 suppose this is M1 M2 then M2 switches ON right because this goes lower and out bar goes to 1 which was initially 0.So I can use this type of logic to calculate give you the values of both out and out bar at a much easier in a much better manner right. So both out and out bar can be evaluated at a very fast phase.

I leave an exercise to you please find exercise to you is that if you can use a DCVSL to get the value of XOR, X NOR, XNOR gate or even an NOR NAND and then may be NOR and may be NOR and OR right something like this. So try to find out for this one and (()) (26:35) is basically a to an extent non issued logic right. So we understood what this basic concept is all about DCVSL and how do you how does DCVSL what is the advantages is that you get both out and output bar in this case but the disadvantage is that the area requirement is very high right.

So for N input you require here large data are almost here + 2 you require at the top right but advantage here is 2 outputs here out and out bar right. If you do not have the case and if only out was available to you should have you could have used 1 inverter at the output side right and you could have gone the static inverter very easily in this case. As you can see here this is basically a XOR XNOR for your using just the problem which I gave you using DCVSL and gives you an idea about how this DCVSL works actually.

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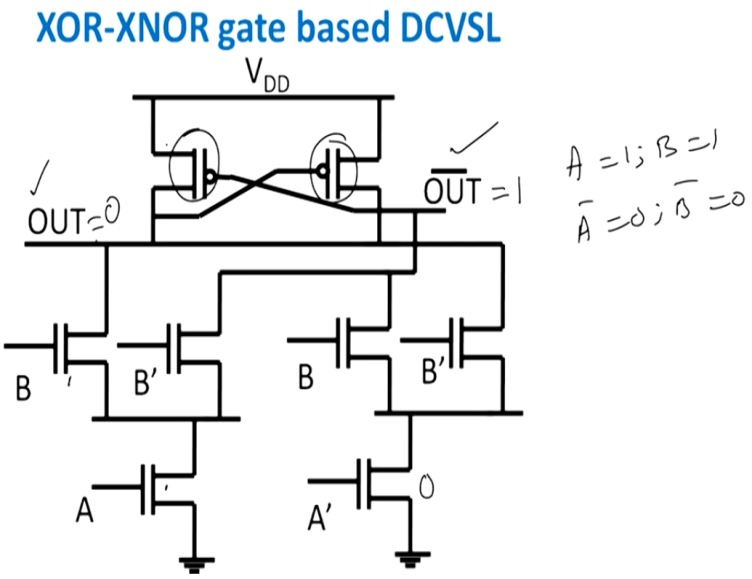

As you can see here this A and B are both equals to 1 say A = 1 and B = 1 let us suppose then A bar = 0 and B bar = 0 in that case if B A = 1 primarily means this is 1 this is ON so I have got out goes to 0 right and in this case if you look very carefully A is this is 0 this out bar will go only one right quire interesting case that was any logic you do it is but obvious this out and out bar will always be sort of will always be a inverted of each other right and that is and therefore out and out bar will be either connected again to VSS or VDD depending upon the values of A and B which you are choosing.

What does this PMOS do they act not only as load but also help you to swing between one step to other at a very fast phase because this is a positive feedback network available to you right. So you have to be very careful when designing this logic that you should be you should know effective values of voltages of out and out bar and how does the A and A bar which you have putting here A bar A values how the how the you are changing right.

You should also ensure that I have discussed with you earlier that try to keep those signals which are moving very faster whose which are basically a signals which are basically the which are critical signals as closed to the output as possible that definition understanding still remains the same for you explanation purposes.

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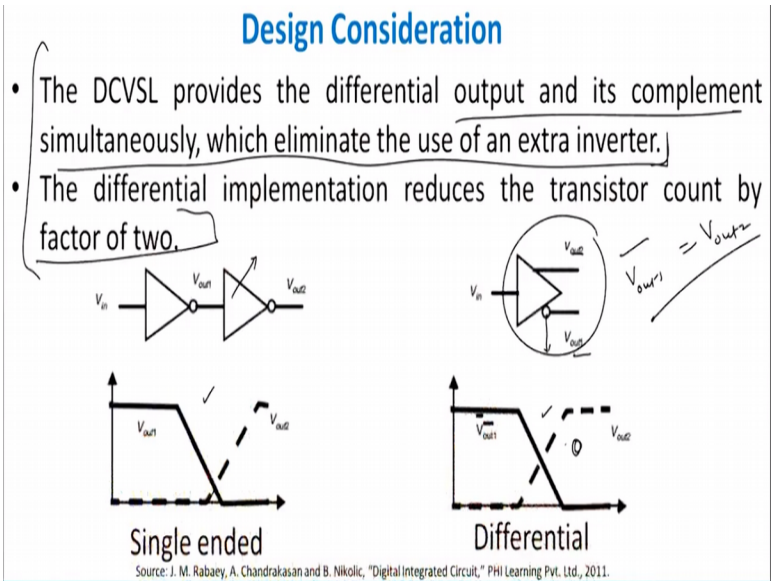

As I discussed with you therefore DCVSL provides a differential output and it is compliment simultaneously and therefore it eliminates the use of an extra inverter. As I discussed with you extra factor which you see in front of you is getting there and the transistor count is reduced by factor of true. So that is two important properties of DCVSL and the way we show in this manner that output 1 and output 2 as you can see there is a small circle here implying that out 1 is basically inverted at out 2 right.

So that is the meaning by circle input at this stage right as you can see that if you have single ended output your if you have a differential output I have single ended output why is this a delay because of the increase in delay of the inverter right and therefore you see that in already fall it to so low value and then it starts to rise. So the delay is very high whereas in the differential logic delay is very low right almost 0 delay will be there if it is perfectly differential in nature.

And the reason being is your extra 50% peak to 50% fall is approximately equal to both the cases now let me therefore recapitulate what we did in this basic module of module number 3 and 4 we understood what is the basically a power amplifier how is a power consumption of a CMOS logic gate and we saw that to be strong function of activity factor but activity factor is again depending on two fact one is the circuit topology which is also known as static and this is also dynamic.

So I should be able to reduce both of them static cannot do too much but dynamic you can do it glitching as well as introducing of something high threshold devices in the middle. Now there is dynamic (()) (30:54) which is I define to you glitching because of finite delay of individual gates what how there are three major issues by which you can do that or reduce the alpha probability of 0 to 1 transactions and these are logic restructuring try to make it as symmetric as possible.

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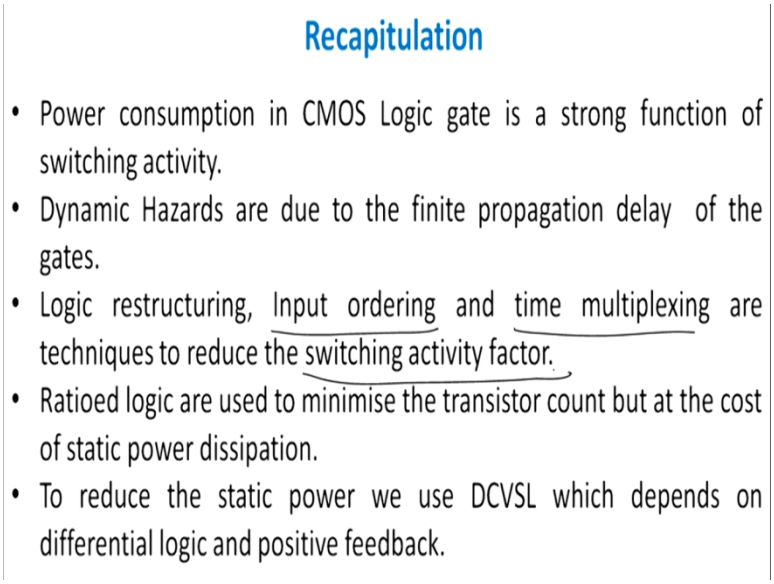

Input reordering try to make the highest reordering 1 closest to the output or delay it in (()) (31:18) to the logic as you can do that you can actually reduce the power and do a time multiplexing job this will reduce your switching activity factor to the larger extent. Then we went for ratioed logic and saw that ratioed logic and implemented by having a normally on PMOS or the pull up stage which is basically PMOS whose gate has been connected to ground and therefore it is ON.

But then in this case as discussed with you W/L ratios are quite critically understanding functionality of the chip because since it is always ON if you make WP larger thus compared to WN the overall WN then you might end up having always stuck to VDD even if vary WN pull down network is ON right. So it should be very cautious the price you pay for it is that lower transistor count the price you pay for in this case is that the power dissipations are high static power dissipations are very high in this case.

Lastly we went to do DCVSL which is basically differential Cascoded voltage showing logic and then we saw that using same logic I can get out and out bar very easily and this out and out bar can easily manipulated or adjusted to get the values of the output characteristics static power dissipation are relatively low in this case and the static power dissipations are low like basically based on differential logic.

So I have a positive feedback does differential logic speeds are relatively higher right and you have almost 0 static power dissipation in this case with this we have finished with the basic idea of DCVSL and CMOS which is complimentary MOS in the module we will looking into pass transistor logic and also at transmission gate logic. So that we will be doing as we move ahead in the next module thank you very much