CMOS Digital VLSI Design
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Module No # 03
Lecture No # 13
Combinational Logic Design –II

Welcome to the NPTEL online certification course on CMOS digital VLSI design and we will continue on combinational logic design part 2 which is where we have left you know previous case this one. We have seen in our previous discussion that for any logic realization we require two important points and that important point is that you require.

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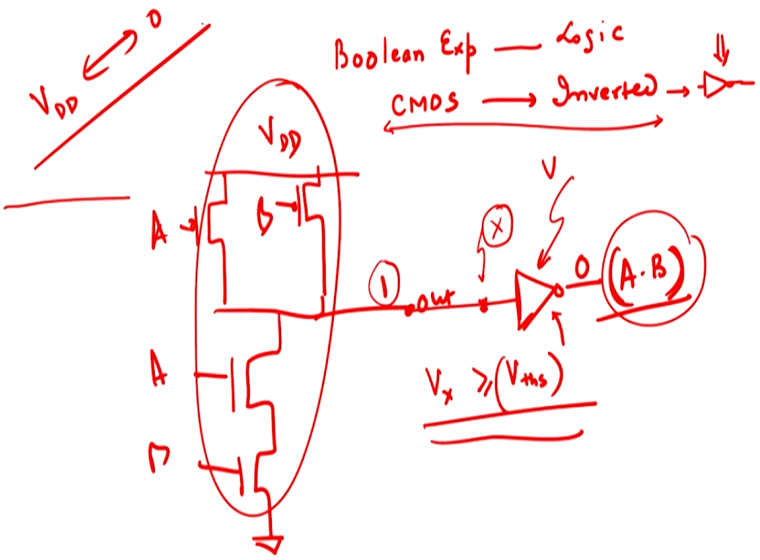

We have seen that you require a Boolean expression right so you require a Boolean expression using this Boolean expression you can realize the logic right now when you use PMOS inverter to do that the logic will always be inverter logic right. So in order to achieve the actual logic you required to put a static inverter in series to the output in order to achieve it right.

Now most of the time it is very important to see or must be seen that if you do not if this logic inverter which we have discussed yesterday does not allow the output signal to swing to value larger than the switching threshold of this inverter then this inverter would not be able to see it on 1 on 0 right I will give an example. For example yesterday's to input NAND gate or whatever

you want to do so if I have got a two input NAND gate right like this and this was my design right AB and I have got A and I have got a B here right.

So this was AB and this is my output right so this will be to your input NAND gate now if you want to convert into a AND you have to pass it through a static inverter and your get A dot B right. This is what we have discussed yesterday but mind you if the voltage at this particular points so this is connected to VDD right and this is grounded. If you connect if there if this the voltage at this point let us suppose we name it as X the voltage at X if is greater than = the switching threshold switching threshold of this inverter then only greater than or less than then only we are able to deduct A dot B right.

For example I have to get 1 here and there is should get 0 here a 1 primarily means that the voltage here should be larger than switching threshold of the inverter it might happen in some cases if this case it would not happen but in some cases is also might happen that this 1 will be read as by this as 0 by this inverter because the voltage available at point X might not exceed the switching threshold of the CMOS inverter.

So you should be very careful while designing two things when you want to design simple inverter by applying a static inverter in cascading with the with the CMOS logic inverter you have to be very careful that the static inverter threshold voltage switching threshold are lying somewhere around VDD / 2 for most practical cases do not try to switch it too much towards VDD or too much towards ground then the reason being that this CMOS inverter characteristics which you see here NAND gate NAND 2 gate we will have almost rail to rail swing.

So I will actually gate a VDD to a 0 swing available to me right so this we have learnt in a previous turn we will also one important point before i move forward is that.

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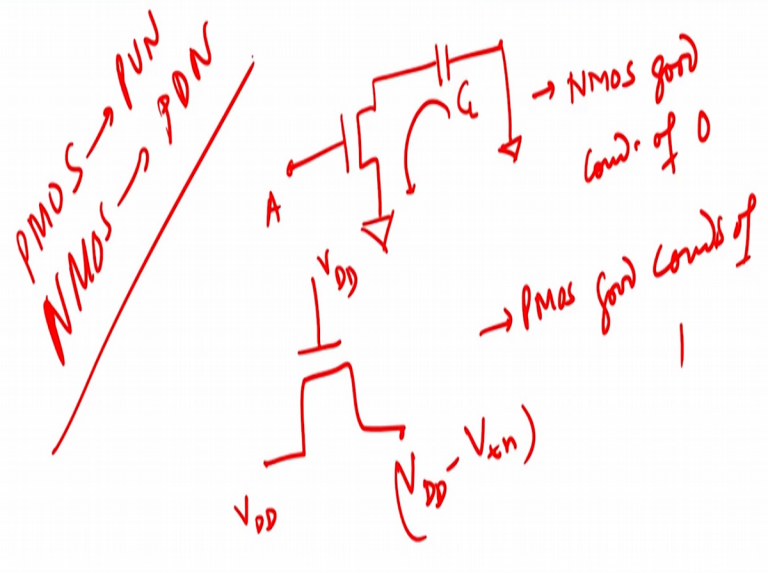

If an NMOS is a very good string passage of 0 right so you got NMOS inverter in the serial is charged to some value then this CL will discharging here and the voltage here will be starting to fall down at the particular point now NMOS inverters are good conductor of 0 right. And PMOS are good conductors of 1 which means that whenever through an NMOS and 1 is past between input and output of NMOS.

So if I pass VDD here and I apply a VDD here then the voltage at this point is VDD – Vtn right and that is the reason why you always have NMOS transistors as a part of a pull down network. So when it is a part of pull down network it easily it able to pull the output voltage to 0 and my PMOS is generally my part of the pull up network it is easily able to pull the voltage at 1 right. So that is the reason PMOS is always a part of part of pull up network right and NMOS is a part of pull down network right and that is the reason why we do like this right. So coming back to the topic which we were discussing in the previous turn.

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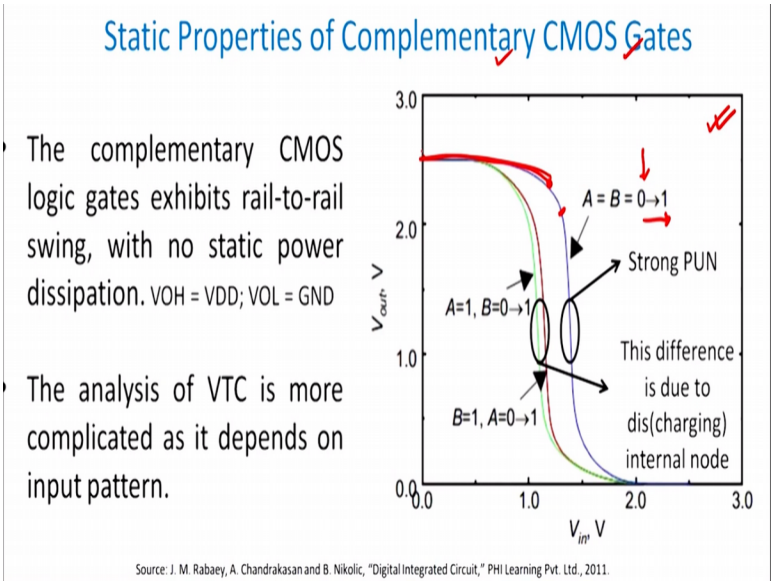

Let me come to therefore the static properties of the complementary CMOS gate right static properties means what? I will take a 2 into so is this example is taking input NAND gate right. So input NAND gate I just not draw here and I will draw it for you again.

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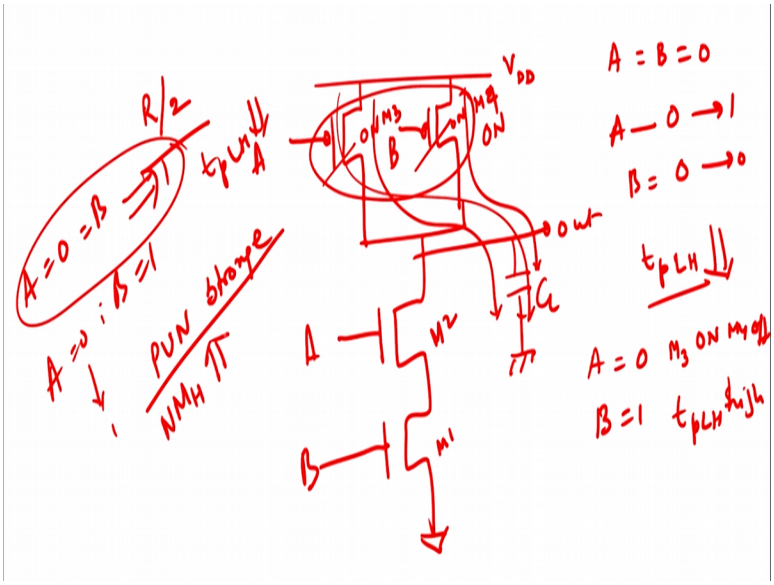

That I have got a VDD supply here right and then I have got this and I have got this then I have got 2 NMOS's in series to each this is A this is B and I have got PMOS's in parallel to each other this is A this is B and output is taking somewhere from here right. So what I wanted to show to you is that when you have a CMOS inverter right CMOS complementary CMOS inverter.

It is VTC which is shown here is data dependent right but type of data available to you in the input side of the logic CMOS inverter will actually determine to you the tpHL as well as the values of your noise margins and therefore the VTC is dependent on the values of your input voltages. Now I will explain to you one by one what do you I mean to say by that so the first idea here is that let us suppose A and B where both equals to 0 and both now go actually to 1.

So A goes to from 0 to 1 right and B also goes from 0 to 1 so both are initially reserve and both 1 now when both are initially 0 please understand the pull up network was on so this was both on so A was also on right and B was also on when both are on this charge CL was getting charged to this part as well as from this path.

So the charging is very quick and therefore your tp on output side low to high will be very low I hope your getting my point because you had two paths of charging the effective resistance therefore equals to R / 2 and therefore since the resistance is fallen down the current will increase as a result you will be able to discharge this CL and I am not faster phase right and therefore the time taken for the output to go from low to high will be very small.

What is the other scenario? The other scenario is that let us suppose A = 0 but B was equals to 1 when A was equals to 0 since this M let us say this is M1, M2 I have M3, M4 so M4 so when A was equal to 0 M3 was in on state right but when my M4 was off there was no charging current thus charging current only from this path this path right and therefore your tpLH in this case tpLH will be slightly higher as compared to the previous case.

So if you take 0, 0 = 0 = 0 and then going to 1 another example equals to 0 but B = 1 and this going from 0 to 1 in the first case your tpLH will be much smaller as compared to the second case right and that is the reason which means that the propagation delay which you see in front of you is primarily (()) (08:47) dependent which means that it depends on the data type of data which you feeding it in resistance.

So with this knowledge with this idea let me see how this works out so let us look at the first graph which is the blue one which is in front of you which basically tells you a if A and B are both initially and both are going from 0 to 1 right. So both A and B where initially goes to 0 and both are shifting from 0 to 1 this is the criteria this is the idea I am putting here so when both

where 0 my pull up network was very strong and therefore you see your voltage high voltage because when pull up was strong output will be strongly connected to VDD and therefore for a larger range of V in input voltage you will have a large value of VDD.

So therefore you see the VDD is extending up to almost this point this much point almost this much point right. So therefore when your pull up network is strong when you PU1 is strong right strong then you allow the output voltage to latch to VDD for a longer period of time and therefore your NMH which is the high noise margin is also very high in this case. So therefore noise margin will be high and your tpLH low to high will also very low in this case right so this two things you should be very careful about at least this stage to understand the whole issue here.

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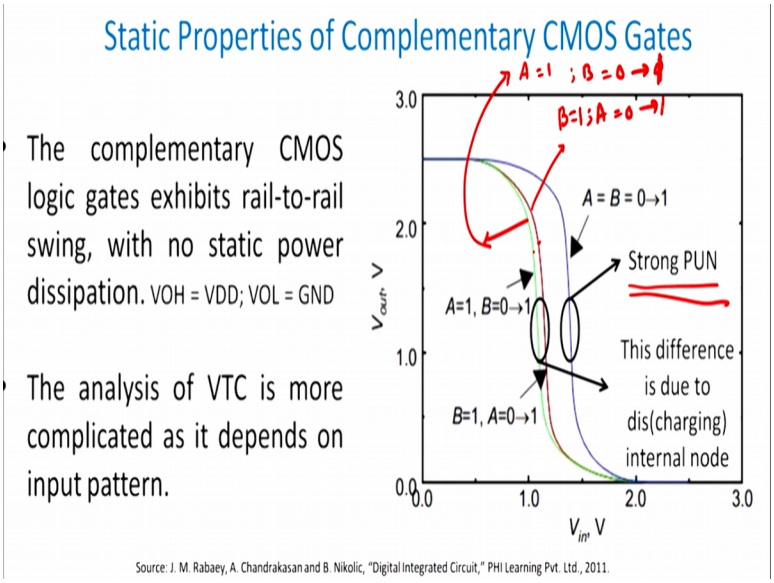

So what your learnt therefore and therefore I have strong PUN network here because A and B where switched on. Now let us come to an issue here on the second case when A was equals to 1 and B goes from 0 to 1 right which is the green one green curve which you see in front of you because of this, this is the criteria which I am using that for A goes to 1 B goes to 0 to 1 0 to 1 sorry it goes from 0 to 1.

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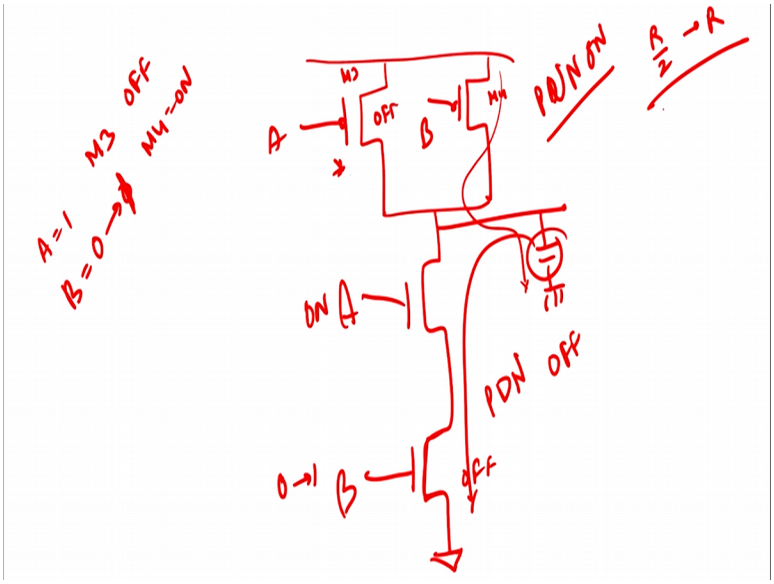

Now coming back to the again the same diagram if I have A here sorry I will just make it once again so I have got this NAND gate available here and I am using that A = 1 and B goes from 0 to 0 to 1 right it goes from 0 to 1 I have got A here I have got B here and I have got A here and I have got B here right.SO A was equals to 1 primarily meaning wise this is cut off so this was off so what happens is that M3, M4 M3 will be off but M4 will be on and therefore there will charging of CL but this charging of CL will be much as compared to the first case because there is only on part available to you and the resistance which is initially R / 2 as now become effectively = R.

So therefore what is happened is that by applying an initial value of voltage of 0 and then going from 0 to 1 we have ensured that this is that M3 initially off which is this one is off M4 is so that charging path is basically this one right when A = 1 this was on this was on but this was off but as I told you in previous term that your pull down path pull down network is basically off state and pull down pull up network is basically on state now when B goes from 0 to 1 right this node or this B switches on and they switched on the voltage output falls to 0 right.

And therefore this goes to 0 to 1 and therefore any voltage are available here will have a root from here and the output go from 1 to 0 right. So tpHL will be now available to you right. So I understand one basic criteria one basic issue which you need to correlate that this is very finite difference between this and this. This green one was equals to 1 and B goes to 0 to 1 and the violet one this this violet one is you the fan B = 1 and A goes from 0 to 1 there is sudden change

is there and a certain change is something why is it like that I will explain to you within few word as you move forward.

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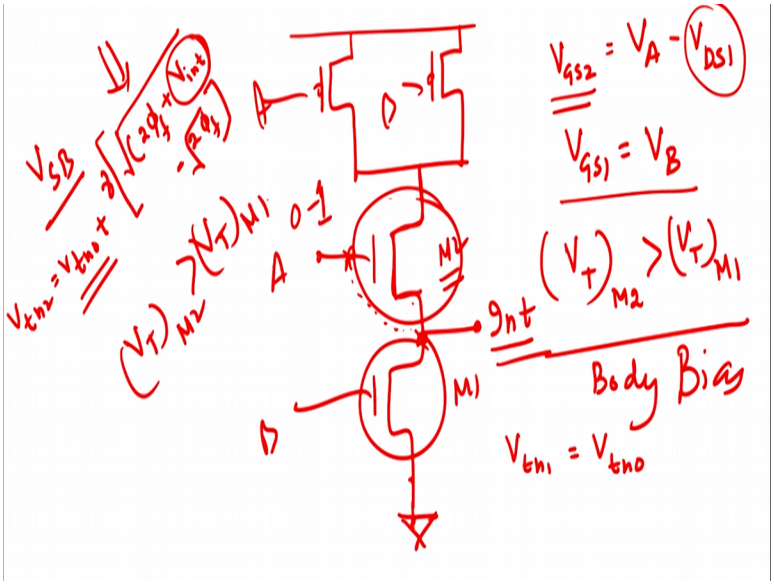

Let me explain to you in that sense that I have again simple inverter appear here right and this is grounded so this is A right this is M2 let us suppose and I have an internal load here INT let me name it I have M1 here and this this is B and of course this is A and of course this is B right. So I can write down VGS2 gate to source gate to source of 2 M transistors nothing but equals to VA is this one – VDS1.

VDS1 is VD voltage this voltage because this is grounded because this sentence is grounded drain to source of drain to source of M2 will be nothing equals to voltage available at this point. So this minus this this voltage minus this voltage will be the effective VGS is available to you clear. Now VGS1 will be always equals to VD why? Because source of this is always connected to ground therefore this will be goes to 0 therefore VGS1 will be always equals to VB.

So you see even with application of same voltage VI = voltages ZB goes to 0 the effective gate to source voltage of the second transistor is lowered by the VDS2 value as a result as a result you can appreciate therefore so the threshold voltage of M2 will be larger as compared to the threshold voltage of M1 by virtue of the body bias. Minimum of body bias first VSB source to bulk so if you source voltage is varying your source to bulk will also vary fine.

So when you source voltage is varying your source to bulk will vary and therefore VTN1 can be written as VTN0 right but for the case of VTN2 I can write this as VTN0 + right gamma which is the body coefficient factor multiplied by root of 25f + VINT right internal load this I close it here – 25F root over my basic question this is a VSB remember this is your VSB and therefore VNT if you find out here which is nothing but VGST = VA – VDS thereof this quantity gets added to VTN0 and therefore VNT2 is larger than VTN1.

Which implies that therefore my final application I want to say is that when the factor is that you do have V = 1 and A goes from 0 to 1 A goes to from 0 to 1 right you introduce a larger threshold voltage MOSFET above all lower threshold voltage MOSFET here. So VT of M2 is always larger as compared to VT of M1 under this particular criteria when this is true or when if this is true one let us see what does how does it influence your overall characteristics of the device of this circuit.

As you can see here that difference between this point and this point is that as you move towards the left right you have a weaker and weaker pull up network right as you move to the right as you move to the right means your right looking at the graph as you move towards this side you have a stronger pull up network. As you move at therefore weaker pull down network and if you move to the left you are stronger TUP stronger PDN stronger PDL which means to say that this green one as got a much stronger period as compared to the this one right.

And therefore this remains to a lower value till a larger limit of Vin so you see thought this difference is very small but please understand this basic issue due to threshold voltage changes right you actually see a small shift why because of the threshold voltage of NMOS is lager right it takes a larger gate voltage to switch it on therefore the pull down network slightly weakened as it starts to weakened and moves to right that is the reason this is basically to the right to that of that first case. So we have understood at least get an idea how a basic VTC functionality of CMOS invertor works out.

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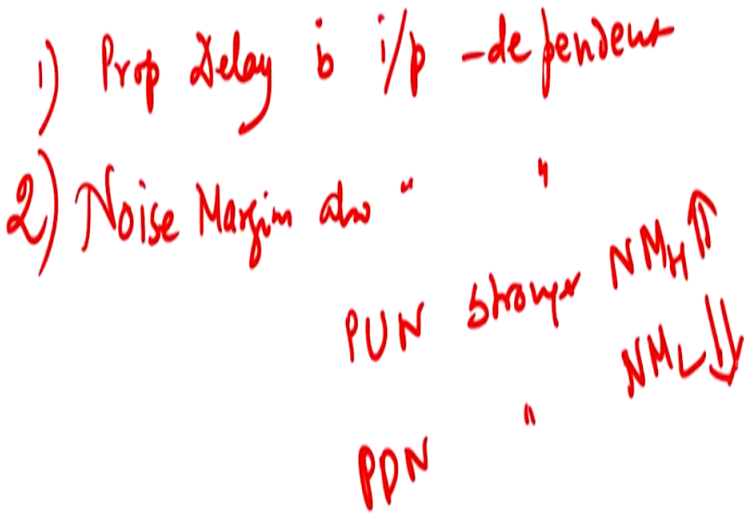

So let me therefore recapitulate this whole discussion the first is therefore that my propagation delay is input dependent right this is very important dependent and noise margins also input dependent. So if therefore if you pull up network are stronger right I will get a higher NMH high noise margin if your pull down network is stronger I will get a larger I will get a larger NML lower value.

Which means that higher PUN for a stronger PUN your NMH is higher why very simple and straight forward it therefore tells me that a 1 will be read very easily as 1 even if there is noise at till larger level right? Whereas when your PDL is stronger a 0 will read as a 0 even if your noise voltages are available to you in the below side right. So it can reject noise much better when your 1 and 0 swing available to you for the pull down and pull up network.

Now this takes care of approximately idea that it is always a noise margin's and propagation delay are input dependent right and that is quiet interesting to look into in general scenario. Let me come to therefore the propagation delay of the complementary right so what we do we have already started that I can replace individual gates right individual transistors by the equivalent resistance values right that is known as the switch model right we have already seen that it is a switch models if I place each transistor by its corresponding R and the switch I can do all the activities of the device using this switch model.

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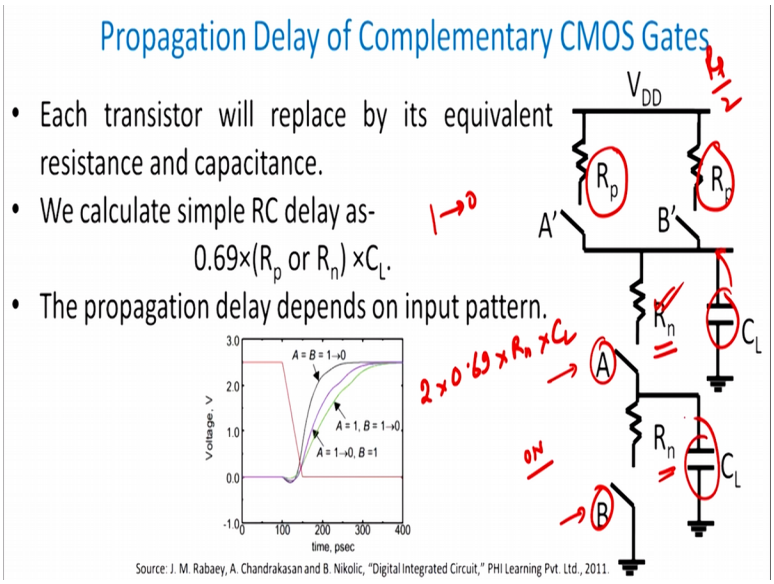

So let us look at switch model for our complementary MOS device here which is therefore I can see at the right hand side this is right hand side we have taken it from Rabaey A chandrakasan and Nikolic book is available this is digital integrated circuits by Rabaey chandrakasan and Nikolic in this case if you look each transistor we are replacing by its equivalent resistance and capacitance right.

So this CL which you see is basically the load capacitance by virtue of transistor at A and CL this CL is again due the second which is the lower one I am assuming that this low capacitance almost equal in both the cases with this knowledge with this basic idea we can simply say that to compute the RC delay it is nothing but block 2 0.69 into R into C that it what it had been talk to us that the delay is effectively 0.69 into R into R into 6 into C.

But quiet an interesting idea comes into picture therefore if you look at the pull down structure or the pull down architecture right if you look at the pull down architecture I require both these transistors A and B to be on in order to have a tpHL which means that for a output to fall from which means that which means that two resistance in series will add up and therefore the overall resistance will be twice the resistance of a single gate agreed.

So your tpHL high to low will be something like this that 2 times 0.69 into Rn into CL right CL assuming that they are almost equal and therefore they are in series so 1 / CL + 1 / CL be there and automatically will get CL / 2. So you get something like this as the overall capacitance values but when you have both A and B going to 0 then you please see that as I discussed with

you in the previous slide that RP will be RP / 2 because you have two resistances are parallel this CL is basically the load capacitance at the output node and this CL is intermediate capacitance.

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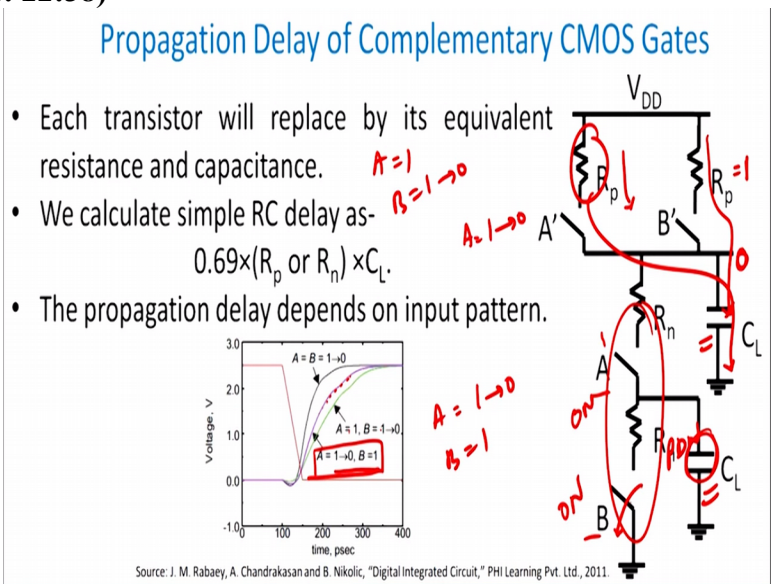

As I discussed as i am discussing with you that if you look at this graph here the propagation delay also depends upon the input pattern we have already seen this point I will be bit faster in this case I will explain to you. See the black one is the line which gives me the black one which is this one is when A and B are both equals to 1 both are going to 0 right both are going to 0 now when AB are both 1 right when A and B are both 1 your NMOS was both the NMOS's pull down was able to discharge the cell at the faster place and therefore a tpHL was much lower and therefore you see this gives you a very fast rise and you can understand why?

Because both these transistors are getting in the on state and therefore CL this CL is getting charged by the virtue of this as well as this so charging is faster therefore switching is also faster therefore you see this redline is increasing at a fast phase so this what we have understood I will explain now let me come to the case when A = 1 to 0 and be was equals to 1 right now when A was equals to when both A and B where equal to 1.

So A and B where 1 means both where on in this case and the output was equals to 0 now what is happening is that A = 1 right A is still 1 but now what as happen is B has come from sorry B has actually so A as gone from 1 to 0. So has got from 1 to 0 means this is this was initially = 1 only this as gone from A = 1 to 0 which means this is switched on which means that I have single path

available to me to so my lower path gets broken of and higher path upper path gets jam or gets charged through this RP value right.

And therefore you see A = 1 B = 1this is this notation the violet color back ground which you see in front of you gives your value. See then the last one is that A was equals to 1 A was equals to 1 right and B was going from 1 to 0 a very sudden change is there second change is this was so both were on right so both pull down was on this case this is the pull network was on now what was happened is that B is going from 1 to 0.

So this is open and your have a path of available to you from here it is getting noded but please understand in the previous case when A was going from 1 to 0 the intermediate capacitance here did not have a path to discharge an therefore you did not have to discharge the path and therefore the violet was moving faster whereas in this case you have to discharge both this CL as well as this CL.

As a result what you will get is the time taken will be larger right so let me again reframe the whole thing recapitulate the whole thing that if A and B are both equals to 1 going to 0 that is the fastest tp LH is there if A = 1 and B for if B = 1 and A going from 1 to 0 is the next fastest and the last one is 8 + 2 1 B going from 1 to 0 is the next fastest and the reason we have just now understood.

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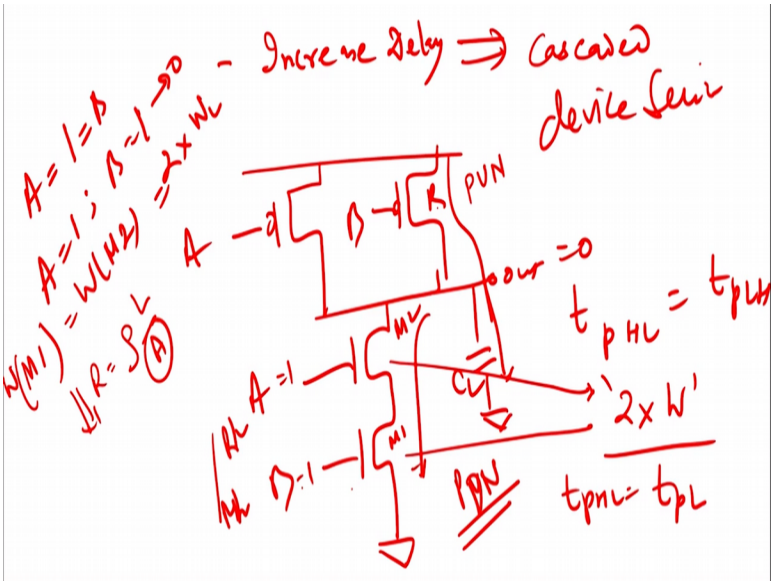

So if you want therefore let me recapitulate this whole thing that if you want to therefore increase the delay right increase the delay then what you do is you try to a cascade device in series cascade devices in series when you put in series the R value increases and therefore you will get a larger RC delay and similarly obviously the low value will be there.

Now from this basic concept can we therefore give you any logic or criteria for the sizing of this transistors? How to size this transistors right? Now you see when your this is output this A and B are both 1 right out is going to 0 right and so there will be some path of it available to you but when A and now if you want to make it tpHL = tpLH which means that you want to make hydrolo transition exactly = low to high transition.

Suppose that is A with which you are starting to do then this PMOS so when so initially A was = 1 = B now = 1 but B goes from 1 to 0. So this is the path which is available to for charging this CL value agreed now this if you want that the charging and discharging process times almost the same there have to ensure that since the capacitance is same you have to just ensure that that the resistance is also same in the pull up path pull up network exactly goes to pull down network the rest is the same right.

So therefore I should do simple thing that I should make the W of these devices double right if you make the W width of M1 and M2 right if you make the width of WM1 = WM2 equals to twice its initial value the low value then I will get tpHL = tpLH and increasing W by twice means basically you were trying to increase the area you are trying to increase the area R is more right and therefore what happens is that R = remember rho L / A.

So when A increase double R falls to half so this becomes R / 2 and this is R / 2 R / 2 + R / 2 = R and this is also R and as a result we will see that whenever you want to have equal values of tpHL and tpLH propagation delay you require to have the W / L ratio at least for the NAND gate exactly double that of PMOS right.

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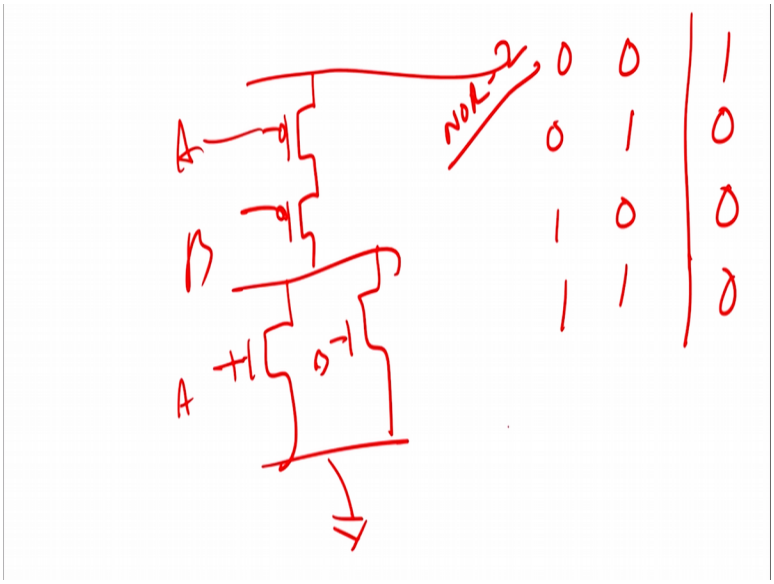

If this is true what you have learnt jus now I will just finish by this session by doing one more thing let me just do one thing that this is basically my two input NOR right by my previous discussion I have two input NOR this goes to ground let us suppose these are all V this is A right A and this is A and this is B right. So when both 0, 0 output will be equals to 1, 0, 1 will be 0, 1, 0 will be equals to 0 and 1, 1 will also be equals to 0 this is that therefore NOR to logic right.

So what we will do in next section of the clock we will be will be looking at NOR to logic and find out tp HL and tpLH and how we can size the transistor here in the as compared to the previous case. So we are just doing the transistor size here right thank you very much will meet next module.