CMOS Digital VLSI Design
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Module No # 03
Lecture No # 11
Spice Simulation –II

Welcome back we had started to look at various functionality of spice and we were actually doing a LT spice simulation,

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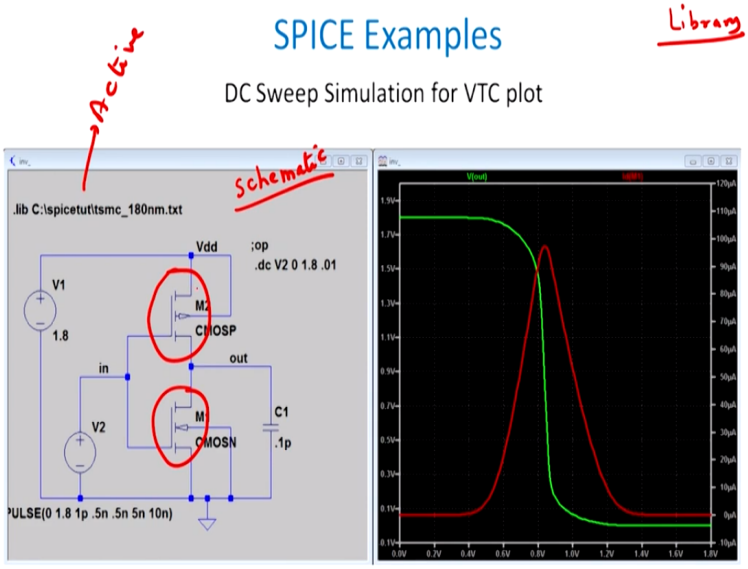

Now you see in front of you is basically the schematic so this part is known as schematic this which means that I am entering so these are the models PMOS and this is an NMOS models right. So and this has plugged and played from the library so I have a DC I have a library in the spice package from where I just to click using the left button of the mouse and then drag it from the library on to the schematic.

So this is known as the schematic in the active schematic therefore I have PMOS, NMOS if you look very carefully the PMOS NMOS body of my NMOS right has been connected to the most negative term most negative terminal as might discuss in the earlier stages which is primarily with the ground and the body of my PMOS is connected to the most positive part of the cell which is VDD right.

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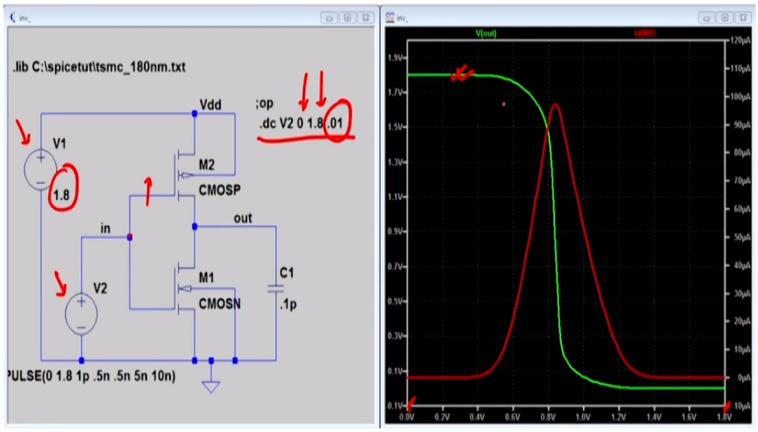
SPICE Examples

DC Sweep Simulation for VTC plot



So what I am trying to tell you here is that I have got two voltage source is here which is V1 here and V2 here right and V2 primarily a so V in is basically this V1 is basically a DC bias whose value is fixed to be 1.8 volts and V in V2 is the applied gate voltage at this particular point right. So this is the Vin which I have giving here now if you look at this point this is dot DC V2. So V2 is DC and it is varying from 0 to 1 .8 at a step of 1.01 so what I am trying to tell you is I am applying a DC bias such that it is varying from 0 to low value to high value from 0 to 1.8.

So if you look the figure here on the right hand side it is basically varying from 0 to 1.8 so you look at the green curve is the output and we will discuss the red curve later on but this is the output which you see in front of you. Remember from the basic voltage transfer characteristics which is basically that if you have V out I will explain to you.

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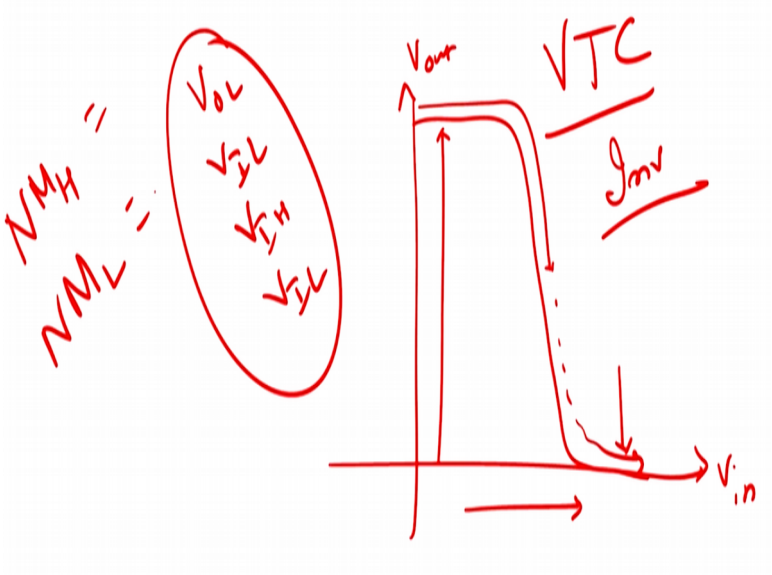

That we do have suppose a V out versus V in right and this is V out here then this something like this has been discussed earlier that has the V in value increases the V out value goes on becoming fixed at a particular point it starts to drop down and then it goes like this to a my well that means the V in is low V out is high and when V in is high V out is low right and this is how a static voltage transfer characteristics for a static inverter looks like.

Now we were from this we can do many extraction for example I can find the value of VOL, VIL, VIH, and VIL right and therefore and from these quantities I can find the value of NMH, NML which is high now its margin and low noise margin spice can get all these value for you in a very easy fashion. So if you look if you go back to your next slide here let us at this slide if you see.

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SPICE Examples

DC Sweep Simulation for VTC plot

We will see that my for low values of input my I have got output is high and as my input goes to high value which is 1.6, 1.8, 1.4 the output is actually almost = 0 it is almost equals to 0 which you see in front of you. This is the basic characteristics of CMOS that I am able to get the full swing available to me which is typically till 1.8 here approximately it is though sorry this is 1.8 which you see here this is the maximum value and this is the minimum value approximately = 0.

Therefore the full swing I am able to get therefore the noise margins are very high this red one which you see the red curve which you see in front of you which is this one is basically the short circuit current as I discussed with you that now we can see very easily that this is the point approximately 0.8 or 0.9 is the voltage at which you get the maximum short circuit current. Why because 0.9 voltage here implies that both these devices are in linear region and therefore there will be a heavy current flow between VDD and ground and suddenly you see a current flow.

So your current was initially very close to 0 micro ampere right but around VDD goes to 0.8 to 0.9 I suddenly saw a rise in the current to approximately 100 micro ampere if you look at the current is approximately 100 micro ampere. So it is 100 times increase in the current this is short circuit current so please understand when I give a DC bias 0 low DC bias to high DC bias I get 1 short circuit similarly If i go from high to low I get another short circuit.

So for every one transition from high to low and low to high I get two short circuit currents and that adds up to the overall power coming back to the spice simulations once again this DC. So

what does spice do is that though we have given a 0.1 difference here spice does very quiet interesting which is known as interpolation linear interpolation technique.

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Then what does spice do is that if I give a voltage value which is by here and I give at next parameter value here it tries to calculate this value here and within this point to this point does what is known as linear interpolation right. So it has a interpolation here and thus the linear interpolation which means that it takes this value and with the slope which is available at this point tries to interpolated at this point right.

So it does not calculate each and every value otherwise the simulation value is very high so it does internal points or internal DC biases which its sees its interpolates and for all other purposes let us tries to find out the value of voltages at individual point. So this is what it is there in the circuitry and gives me a relatively a good value to work on with. So I get a VTC available here this is my NMOS this is capacitance we have used of 0.1 Pico farad this is the capacitance which we have used here and this is the PMOS here and this is NMOS here.

An important line which you need to insert is something like this right which tells me that for 180 dynamiter TSMC. TSMC is basically a foundry it is basically known as Taiwan semiconductor manufacturing company right manufacturing company TSMC and it provides to you that various parameters required for current to be calculated for 180 dynamiter MOSFET.

For example it will give you the mobility it will give you the value of oxide thickness it really give you the value of that value of gate voltage that which or drain to source voltage at the onset of saturation is VDSAT right. All these values will be given by this text file so this text file is basically a file which is provided by the manufacturer right to these companies which is LT spice in order to integrate their model with this spice.

So that for the results which you get are in very close reality or the actual simulation rules which you see. So this is important file dot lift file and you have to insert this log lift file from the source. So you define the path from where are you taking it and then you dot leave you get the next slide.

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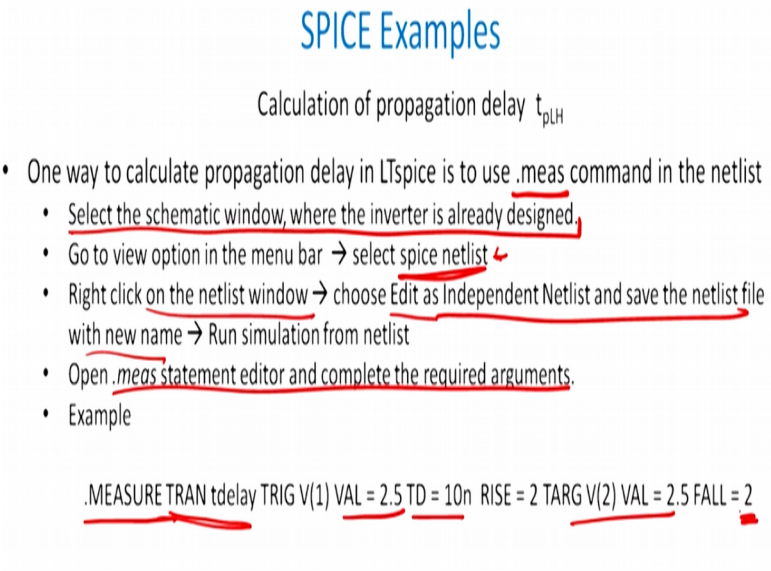

Let me give your idea how to for example measure the propagation delay from low to high which means that I have I want to do a low to high transition input output transition how do I do it the way to do it is to use that mes command in our profile right and I just show you the next slide and I will explain to you what this amount is.

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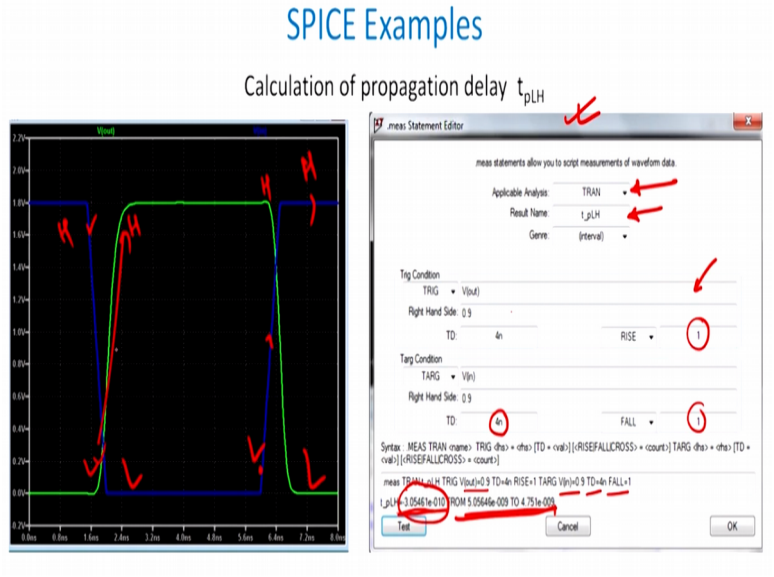

So you go to so what you do here is that you select the sematic window right where inverter is already designed. So the current schematic window of the inverter is there you just have to go to the venue bar and select spice net list right, right click and net list window and choose edit as independent net list say the net list with in new name.

So what you do your inverter save it as a new net list save it as a new profile and then you open the dot mes statement within the editor and complete the arguments what are the arguments which is available there for MEASURE transition delay Tdelay means basically transient delay and value I 2.5 lowest value and you give increment or decrement of 10 nano second and second value is 2.5 high to low with the fall of 2 nano second approximately right.

So what we do just look at the statement here I give a transition statement here right what I need to store it in name so I get tpHL LH right and there I say the interval means I will have to do a internal swapping between low to high what I do I try to find out the value of V out and I give 0.9 as the highest value where I try to reach is approximately with the delay of 4 nano second I defined and then fall I define as 1 and rise is 1 and then what we try to tell you is that my VDD is basically 0.9 voltage and then my fall time delay time and my input voltage is defined here.

From there I get the value of tpLH to be equals to this much value right tp LH low to high value and between what point and what point is given by this these two points. So between these two points this is the points of tpLH I get low to high value which I get right. So if you look very

closely this is my output right which is going from high to low and therefore my green one is going from low to high but when output is input is going from low to high right your output is coming from high to low right.

But we input is going from say high to low input is from high to low your output is going from low to high. So I have trying to find out this value of time taken in order to reach this value right ideally this should be 0 obviously as you are aware this will never be 0 because of residual capacitances resistances. So I recommend that please open up the spice package and try to do all these examples we will giving you right assignments for this one in due course of time for you to handle all these course.

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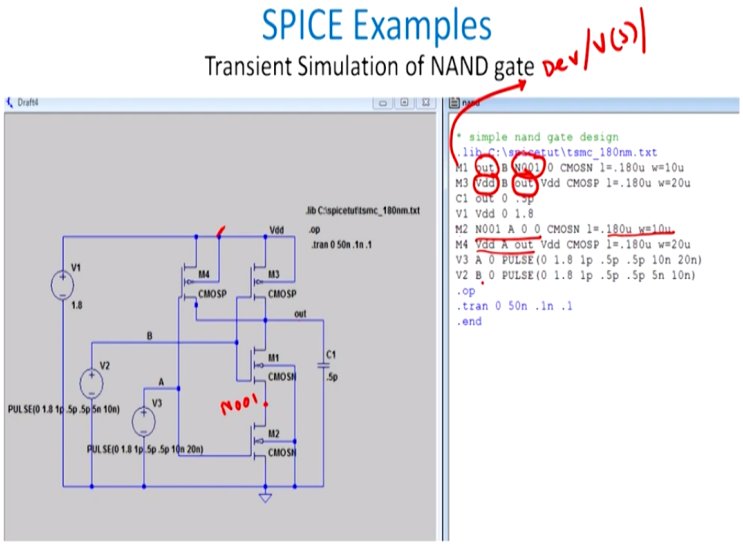

Let us look at simple to input NAND gate I think NAND gate to table all of you are aware. So if I got basically a three input system with a this basically a two NAN 2 right NAND 2 and we get 0, 1 here so for all these cases we very well find out what the value will be so if it is 1, 1 output and output will be 1 end of that will be 0, 1, 0 will give you what and will be equals to 0 output will be this will be again 1 this will be again 1.

So you have got 3 ones and one 0 with this you just write down the simple term this is the programming schematic entry this is the corresponding schematic entry which is see you in left hand side it is easier and this one is in a difficult you require a bit of practice to come to this point and if you look at this point M1 is what? M1 is let us say M1 is M1 right M1 between these

two points it is there between this V out which is v out node and it is also between the point which is given by N001 right which is somewhere here and whose values are length is 0.180 micron which is 180 nano meter and width is 10 micron.

So width of the 10 micron right and then width of this PMOS M3 is 20 micron right and then C1 is nothing between out and ground is 0.5 Pico farad V1 is the voltage source between VD and ground and this is ground this is VDD how much value 1.8 M2 is what? M2 is so let me wrap this point for all practical purposes what is M2? M2 is again an NMOS between which point between this N this is N001 and ground whose value is 1.8 nano meter and w = 10 micron.

Similarly M4 is between what between VDD and out so it is between VDD and out so what is do is I tried to find out the two nodes where source and drain are connected. So the first this one busily your the device or the voltage source or the current source so on and hence so forth the second point is that node or the originating node from where its originating and the third which is this one.

For example so what we define we define this node right and then we define the output node here which is there here similarly between the input node VDD and output node V out which you see in front of your right. So these are the few techniques which you should be careful about.

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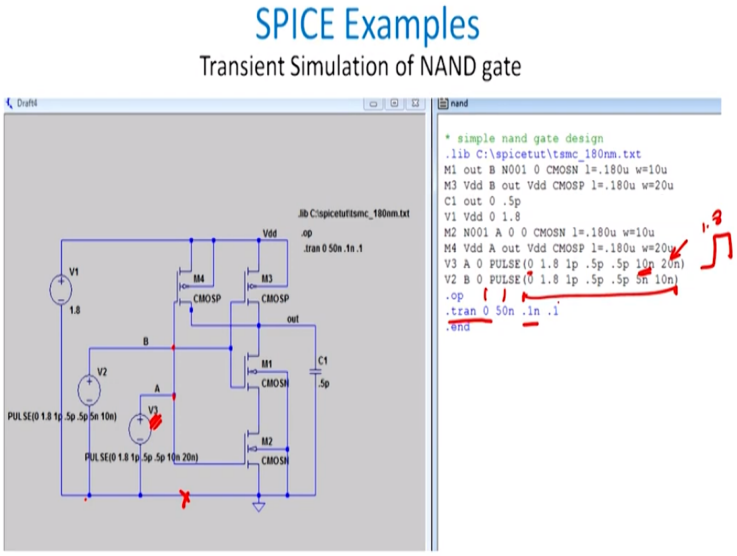

We come to the next stage which is V3 what is V3? V3 is basically the voltage source used here which is here and it is between node A which is this one and ground and v2 is between node B and ground but I have giving a pulse here right. So I am giving node giving a pulse right whose dimensions are given in this banner it goes from 0 to 1.8 volts right with 1 with 0.5 second 1 pico second rise time and 0.5 second incremental value and then we go from 20 Nano second still 20 nano second we go and the time of 10 nano second. So this schematic values it has to be fed by you and you can change it as per your requirement dot trans means you do a transit analysis from what to what 0 to 50 second and with the 0.1 nano second as the increment value which.

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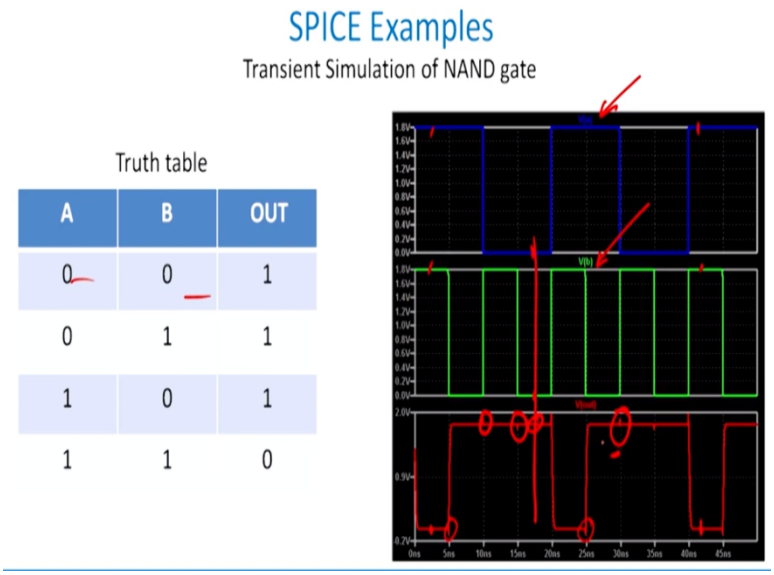

So this is the value we will like to do to with this if you go back to the results it did something like this this is VA is the input voltage and this is VB which is your which is so VI is 1 voltage which is the input voltage VB is another voltage and what you see here is another output voltage here right this is the V out as we discussed for 1, 1 you get 0 so if you get 1 here I get 0 here but if I have 00 which means this point and this point if you go here I have got 1 here right 00 give me 1 here right.

Similarly if I do a let us say let us say 1 here right and a 1 here I get a 0 here right so it is getting fulfilled. You see quiet interesting a small spikes here right you have small spikes here when the when either VA or VB or together means when you see a spikes together also right we will you can see spikes here also which means that when either VA or VB or just VB actually does a transition from 1 to 0, o to 1 you actually start to saying spikes at the output side right.

I will just give an excise to you these are basically miller spikes coming out because of miller capacitances a miller capacitances and discussed already this in the previous discussion and I have already told to you that why this capacitance come into picture these capacitance comes into picture primarily because of large amount of overlap between two points and as a results these spikes which you see in front of you add to the large amount of power dissipation is that digital logic design helps you to do that.

So primarily to reduce power one methodology is to reduce the overlap capacitances parasitic and so on and hence so forth. (()) (16:17) as I discussed with you but coming back to spice once again spice helps you to do what? Will help you to try to find out logically the values of current voltages and also give you the various values of voltages and currents in this network I will recommend that you please download the spice packages with you and try to have a good look at it.

Many solid examples are available at open source you use one of those solid example and you can learn any other ting spice since this course is primarily digital VLSI design and lot of simulation I cannot give you anything further than this you can look at any of the large amount of data large amount of methodologies by which you can do the spice simulation but rather than teaching this is more to do hands on. So it will be better if you are able to do hands on this one so take the simulation tool download after downloading it try to inculcate or use these platforms with these I think I will stop here and we will shift to in the next topic which is the combinational logical block part 1 thank you very much.