CMOS Digital VLSI Design
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Module No # 01
Lecture No # 01
MOS TRANSISTER BASICS – I

Hello everybody let me welcome you to this NPTEL online certification course on CMOS digital VLSI design. The first module which will be given is MOS transistor basics as you can see in the PPT. Now over the next about 20 hours of this module of these sections we will be actually looking into the basic architecture of a CMOS VLSI digital design. Primarily we will be focusing on digital design and it will be also based on complementary metal oxide semiconductor which is CMOS so CMOS stands for complementary metal oxide semi-conductor we will see what does it mean?

So the first about 4 to 5 hours of the lecture will be primarily devoted to the MOSFET which is the basic building block for CMOS. And after using that as the building block and let us see how it works out in terms of the electrical characteristics of the device in the circuit. We will then move on to the behavior of the CMOS in getting a arithmetic unit. For example can we design a adder using CMOS? Can we design basic multiplexer using CMOS technology right.

After doing that which will be basically looking into the arithmetical part in the logical part of the processor. We will be finally ending our structure or our module or our online NPTEL course on the basic fundamentals of the system design for example we will be looking at memory primarily at memory as one of the example of using this circuit design. We will be looking also its peripheral circuitry.

So with the next 20 hours of this lecture online lecture course we will be concentrating on these few facts which is stated just now. The first module as I discussed with you just now is on MOS transistor basics. And this is MOS transistor basics part 1 we have part 2 after this module itself.
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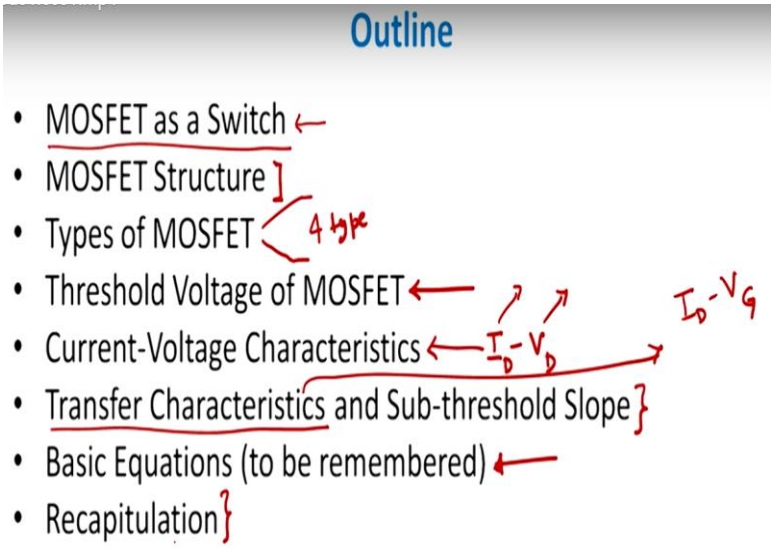

So let me come to the outline of the module is as follows we will first understand MOSFET as a switch. Now why is it important?

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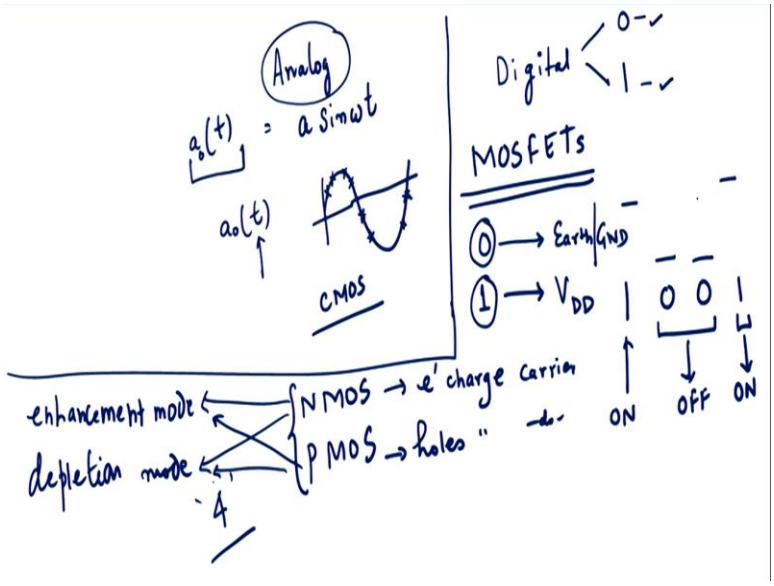

Please understand that when you are actually working in digital logic right in digital logic whenever you are working you always work with zero's and one's right. Unlike in analog wherein your signals are basically time dependent which I mean to say if it take an analog design right I will have a signal for example A sin omega T which primarily means that if I have let us suppose a0t then this a0t is basically a function of obviously the time which means that for each and every time I can tell you what will be the value of the signal available to you.

Whereas in digital logic which is seen in front of you we are only working with zero's and one's right. So therefore it is very important that I should have a device with me right which actually does the switching easily between 0 and 1. So that is the prime motivation that why MOSFET's which is we will see the structure of MOSFET why MOSFET came into the whole study of things?

Because this is one of the device which will see just now in the next slide which allows you to easily shift from a 0 voltage to a high voltage that means you will have something like this you will have one's and zero's may be 0,1. So this is basically 1, 0, 0, 1 which this means that this is in ON state this two will imply that will be in off state of MOSFET and we can have this one as the ON state of the MOSFET right.

So I can easily therefore change the state of this device which is MOSFET Metal oxides semiconductor field effect transistor without actually looking into large amount of delays or large amount of power dissipation. So if I can do all these mechanisms at very high speeds and relatively low power my job will be done to do the basic fundamental blocks of a digital VLSI design.

Whereas in analog design it is not like that in analog design you are actually working with something like this your sign wave and therefore it is suppose you would need to work at this point you also need to look at this point need to look at this point. So there might be multiple points at which the behavior needs to be known right we of course we use MOSFET for analog design as well but the things become a bit more complicated in analog design as compared to digital design.

Please understand in digital design 0 applies to the earth or ground right GND ground or 1 applies to VDD which is the applied voltage. So which means that I apply voltage if my systems goes to the applied voltage it is termed as 1 if my system geos to ground applies to 0. So I require therefore a switch with this basic knowledge or the motivation behind this first module we will first introduce to you therefore the next slide which is here that we will explain to you how MOSFET works as a switch right.

Then we will come to the MOSFET structure itself why is it important? Because you should know how a MOSFET structure looks like and therefore if you are able to appreciate the MOSFET structure in terms of its dimension and its placement of various modules within the MOSFET you will be able to appreciate its working principles in much better manner. So that is the reason why MOSFET structure we will be concentrating on as we move along.

What is the type of MOSPFET's? We will be looking into two types of MOSFET's primarily right we can have MOSFET's again two shows or in we can have MOSFET's again in two parts or in two ways. I can have MOSFET in terms of its charge carrier capacity so I can have NMOSFET, NMOS which is also and also PMOS right. So this NMOS is basically where electrons are the charge carriers right and here you will have holes as the charge carriers right.

So you will have this consideration that means based on its material properties I can have two types of devices which is NMOS and PMOS. Based on its electrical characteristics I can also have two types of devices and this is known as enhancement mode MOSFET enhancement mode device, enhancement mode MOSFET and I can have a depletion mode MOSFET right.

So therefore what does it primarily mean we will come to this discussion as we move along but let us therefore have technically I can have therefore four types of structures I can have NMOS enhancement, I can have NMOS depletion, I can have PMOS enhancement, I can have PMOS depletion right. So typically I can have four sets of structures available to me. So this four structures we will have very separate and unique behavior but the underline physics of its mechanisms of working still remain the same for all the four structures or the four configuration.

So this is the basic concept of the basic idea which we will be looking into as we move along in this module. Now if we come to the after we have finished with the types of MOSFET's which is we have just now seen there are four types here right. We define but it is a very very important property specially dealing with VLSI design is what is known as the threshold voltage of a MOSFET and we will discuss that as you move along which means that do we have a parameter available with us?

Which will actually let us know at what voltage this 0 to 1 switching can take place which means let me say give you an idea let me say I want to switch it at 1 volt. So if I apply a voltage of 1

volt onto a MOSFET and if I make it swing upwards to make it 1.1, 1.2 can I switch it on? Or if I load that voltage applied to the MOSFET below 1 volt say 0.9, 0.8 can I switch it off? Yes I can do that then we define 1 volt as the threshold voltage of the device right.

So we will see what is the definition and how can we understand the threshold voltage we will also look into the current voltage characteristics which is also referred to as IV characteristics of the device. I is the current and V is the voltage this current voltage please understand is basically the drain current versus drain voltage and that this is how it differentiates from the transfer characteristics right.

So we will be looking subsequently on transfer characteristics and this is this characteristics is basically between drain current but the gate voltage right and this is between drain current and drain voltage. So I will just show to you just now that MOSFET can have three terminal primarily three terminals but effectively four terminals and using this four terminals I can manipulate the current flowing through the device.

We will be looking at the sub-threshold slope which is primarily the switching characteristics of the device we will also look at the basic equation which we have developed. So I will be deriving certain basic equations and explaining to you how does it work out? And then we will recapitulate what we have learnt till now as far as this course is concerned.

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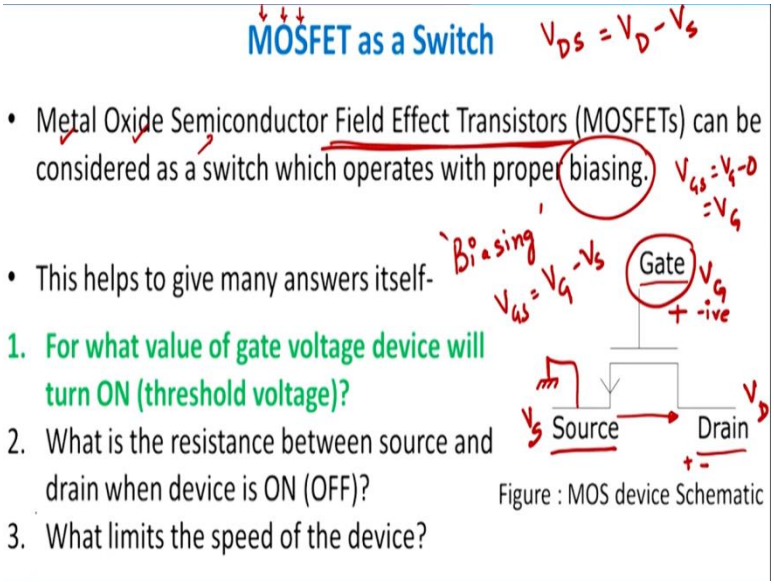

Let us look at the MOSFET is switch the first thing which you should be aware of. So if you look at the MOSFET its primarily a if you look at this stage at least it is basically a three terminal device out of which the first terminal is known as the source the second terminal is known as a drain and the third terminal is known as a gate right. So it is basically a three terminal device source, drain and gate right. Please come to the analogy here analogy of what analogy of water tap.

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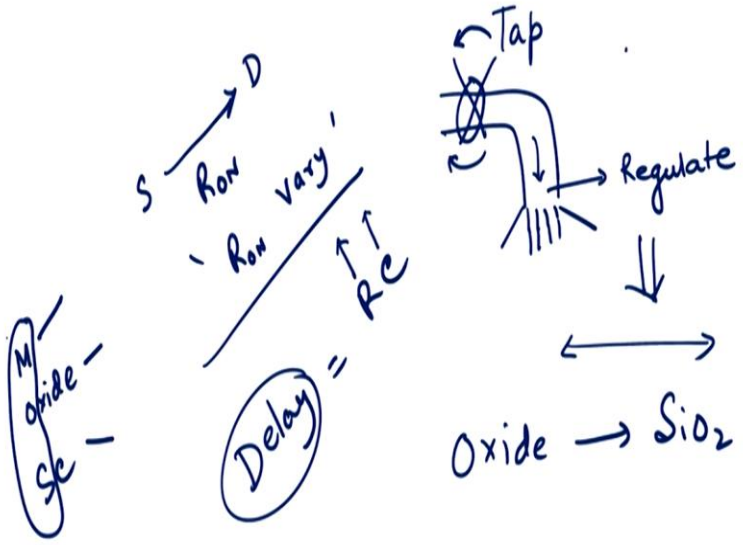

Let us suppose I have a water tap here right and water is flowing out of the tap right water is flowing out pardon me I am not a very good do not do very good drawing and I have a tap here right. So this is basically my water tap now by changing the by making it moving in the anti-clock wise direction I can load the flow of the water flowing through this pipe or by moving it in the clock wise direction I can actually increase the flow of the pipe right.

So by moving the clock either in the anti-clock wise direction or in the tap either in the anti-clock wise direction or the clock wise direction I can therefore regulate the flow here right which this is the only think which we should remember but means by applying a force in the transverse direction which is transverse means the water is flowing in this direction and you are applying a force sort of in this direction using a valve you are able to regulate the flow of water.

Similarly if you can actually therefore look into the fact that MOSFET's exactly behaves like a water tap that means by applying suitable potential on the gate side I can therefore manipulate

the amount of current flowing through source to drain right. So this is the only thing which we should remember it as a switch which means by applying a suitable gate voltage if I can manipulate the current flowing from source to drain such a structure is basically known as a MOSFET.

What is the full form of MOSFET it is metal right oxide right semiconductor which is this one and then field effect transistor right. So this is basically a field effect transistors right so this is basically why it is field effect? Because again as you must be knowing for a basic semiconductor courses or basic semiconductor device courses that in this case the flow of electron is guided by the amount of electric field present in the device right and that we will see how it works out.

So let me define one important term here which is very very important and we will be using it time and again and that is known as biasing right. So we define a term known as biasing what does biasing actually mean? Biasing means application of appropriate voltages at the three terminals of the MOSFET so that it can be moved from on to off state and vice versa right. So therefore the biasing therefore means the amount of voltage applied to gate, source and drain.

So amount of voltage applied here is as VG amount of source is VS amount of voltage applied is VD. When we say VDS we effectively mean it is VD- VS right when we say VGS we effectively mean to say VG – VS so please understand this notation and we will following this notation time and again throughout the modules. If we look very closely here for all practical purposes it is a convention and there has been a reason where is convention.

Source is always grounded right you apply a positive bias or a negative bias on the gate you apply a positive bias or negative bias on the drain but source for all practical purpose generally in most of the cases is grounded right you ground the source. So when you say VGS effectively mean to say VG – 0 which is therefore nothing but VG. So when you say VGS or VDS it is the absolute value of voltage which you are putting on the drain side or gate side which will give me an idea about the gate to source voltage or drain to source voltage right.

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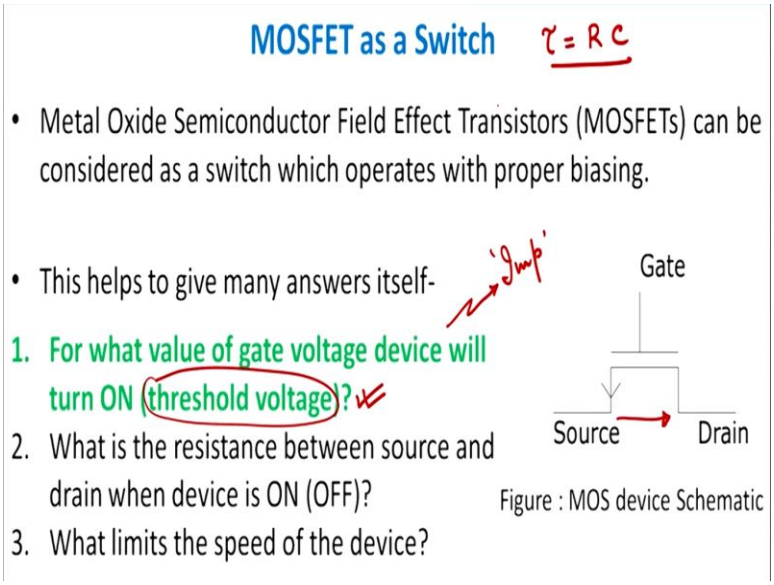

So what are the three very important questions one needs to understand? The first thing is for what value of gate voltage which is this question highlighted in green here. So we need to first understand for what value of gate voltage right you will be able to switch on the device and that is how we define as a threshold voltage of the device. So this is underlining green very important concept or understanding in digital VLSI design at least.

Once you switched on the device you have a current flow between a source and drain right you will obviously have the current flow right as I discussed with you just now. Now as per your very basic electrical engineering knowledge Ohm's law will tell you when you apply a voltage in a current flow I will always have a resistance of the device which is basically voltage by current.

So when your device is in the ON state can I calculate what is the value of the resistance offered by this device? And can I vary that resistance which is Ron? So I what I am trying to tell you is that let us suppose I have got by source and drain there is a current flowing through source and drain right if the current is flowing through source and drain I will obviously have an ON resistance available with it.

Now do I have a mechanisms by which I can vary this Ron right this is the bottom line we will see as far as this is concerned but means can we apply a proper bias to change the Ron value and why is it important it is very important because then if you change the Ron value you can change the amount of current flowing through the device and therefore let us suppose the user

comes to me and I want the 1 ampere current and I can give you a 1 ampere current a user comes to me say no I want 1.5 ampere current I still give you 1.5 ampere current by simply changing the value of Ron.

But changing the value of Ron imply that you need to change certain biases of the device in order to achieve such a structure. We will be therefore also looking at the speed of the device and very very importantly you must be also knowing this fact from your understanding earlier understanding the Tau is basically equal to R into C what is this Tau? Tau is the delay so basically if you go back we define delay to be equal to RC times constants or in a very basic language that RC times constant is defined as my sort of my delay which is available to you.

So higher the value of resistance offered by the device higher the capacitances and higher the resistance more will be the delay. So this methodology gives me an idea that if I am able to find out the resistance at least one part of my job will be done I can I need to find out capacitors which will come in module 3.

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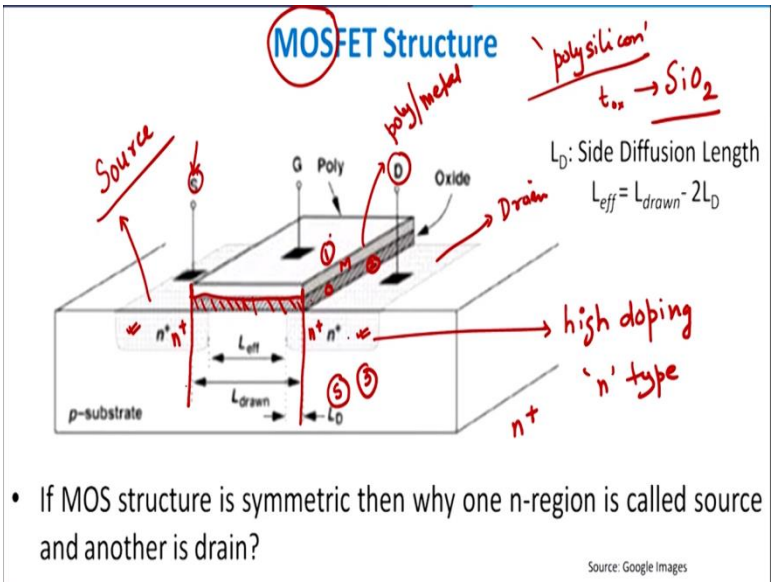

Now let us look at the structure of the MOSFET which you seen front of you. The structure of the MOSFET is something like this in front of you and this is a three dimensional structure and this three dimensional structure if you look very closely has got few important properties which you should be very carefully look into the fact. If you look at this this side and this side this is basically a P type substrate.

So this is basically a P type semiconductor the whole block here which you seen front of you is basically a P type semiconductor which you seen in front of you this all is P type right this all is P type here you also have two regions here which are the two regions this is one region which is n+ so you will have very large doping concentration of electrons here you will have very large concentration of the doping of electrons here.

So these two regions this will have high doping concentration of what type of n type high doping of n type and therefore we referred to this region to be as n +. So I have n+ here I have n+ here right this is known as the source referred to as source here referred to as S, and this will referred to as drain here right drain and this is the drain which you have seen in front of you this is the source which is seen in front of you.

Now you also need to grow the gate which is the third terminal which you seen in front of you. What is that gate? This gate is primarily so this is this if you look at this point this is source this is gain this is the oxide layer which is there right this is the oxide layer this dashed curve which you see in front of you is basically the oxide layer right and you have this known as poly layer or metal layer.

So this will be known as a poly or metal poly means what poly means basically poly silicon it is an amorphous form of silicon and which acts almost like a metal and it is surface properties are very good in order to make it a gate device you can also replace it by a metal proper metal of proper work function. This is a oxide layer which you seen in front of you this oxide layer is primarily for your understanding purposes at this stage is basically silicon dioxide.

So I have therefore a semiconductor here right this is my semiconductor this is my oxide and this is my metal right and that is the reason this is known as the metal oxide semi-conductor. I hope I have been able to explain to you the first three characters of the device here MOSFET's after this first three are metals which is this layer metal layer number 1 is metal layer number 2 is oxide and layer number 3 is basically your semiconductor.

So you have got MOS structure available with you which is metal oxide semiconductor. Now what is happened is we defined so this you have drawn up so you have drawn the metal gate

from this point up to this much point right so this is your point where you have drawn the gate this is defined as Ldrawn.

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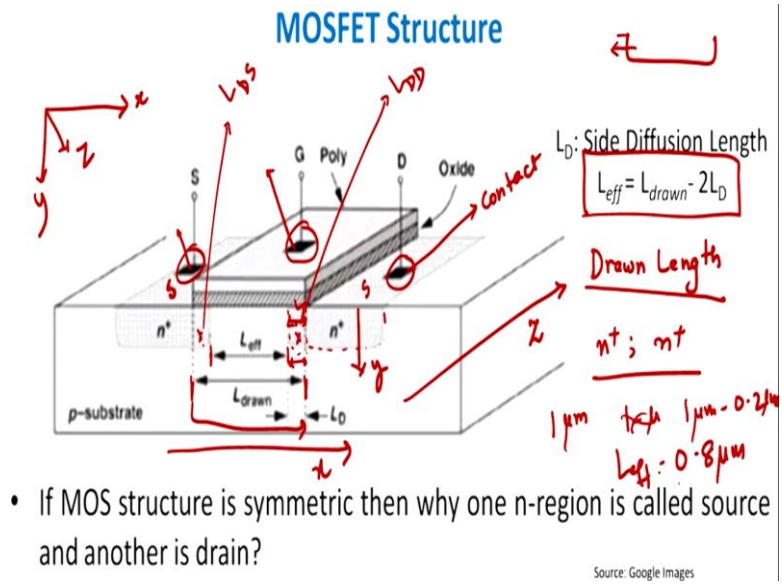

So we define this to be as this to be as this distance to be equals to drawn length we define this to be as the drawn length. Drawn length is also known as the basically the gate length right but this is the effective limit we will see why? So this is the length which I defined here primarily as the distance of the gate. So in this direction right so let me define the directions for you this is let me say x right and let me say this to be as y and let me define this to be as z.

So this is my x right this is my y right sorry this is my z and this is my y so I have got xyz 3D three dimensional structure available to me. Now we define this so now let me see what happens so this black color which you see here and here are known as contacts why because primarily if you look very closely this is a semi-conductor is not it right. So you require the final layer to be metal because you are all your final layer metal is all your current carrying capability the very good current carrying capability is of metal the lowest resistivity highest conductivity and therefore the least power dissipation will be there.

And therefore what I say is the final layer at which the signals will move the final layer top layer will always be a metal. So i somewhere or other require a contact or a junction between semi-conductor and metal that is what you see in front of you here. So this is one of the junction here

another junction here another junction here right. So this is a metal semi-conductor junction which you see in front of you or metal semiconductor contact.

So I have a drawn length as I discussed with you this is the drawn length which in front of you but what has happened is when you have actually making this n+ region here right this n+ regions these n+ regions are heavily doped right. When they are heavily doped because of annealing because of temperature variations and so on and so forth they will do side diffusion which means that they should remain stable at a particular point they should remain stable between these two points but what has happening over the time these are start moving in this directions right.

So which was initially you had actually meant to be drawn like this right you ended up having something like this. So this we define to be diffusion length So we define this to be as the LD or diffusion length. But we understand since source and drain are perfectly symmetrical to each other you will have two diffusion lengths one on the source sides this this can be referred to as L diffusion source and this can be referred to as LDD right.

So therefore the effect so this will be what? Since they are entering in the whole region the effective length available to me is not shortened and its defined as L effective – 2 times LD why two times? because one is this side one is other side fine. So if I have a 1 micron channel length right effective length sorry drawn length is 1 micron but your LD is say 0.1 micron then and therefore your L effective will be approximately equals to 0.8 micron.

So you had started your design with one micron device you ended up having 0.8 micron fine, so for all practical purposes at this stage please understand that we are using this oxide layer right oxide layer which were using here oxide layer basically silicon dioxide right. So what is the final structure available to me I have metal I will have oxide and I will have semi-conductor here. So I will have metal oxide and semi-conductor right so this is therefore known as the MOS transistor available to me.

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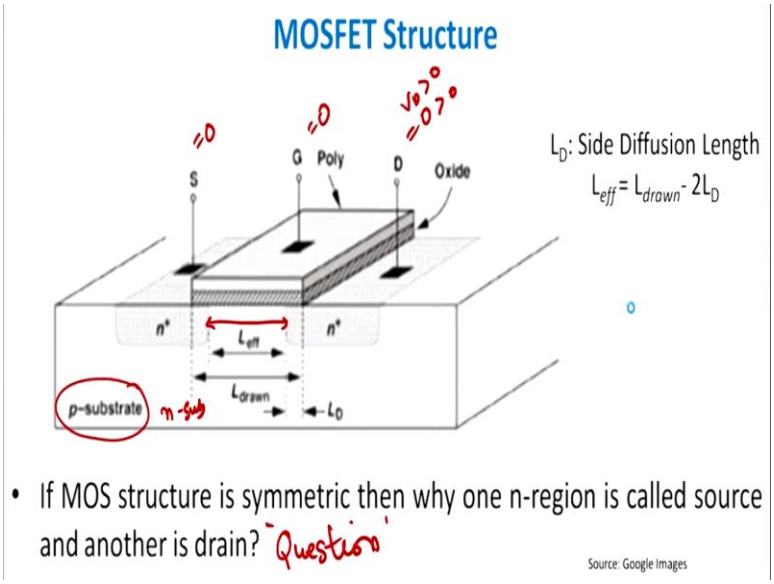

Now if you therefore see this structure and you see you will see very well but this is perfectly symmetrical structure right it is perfectly symmetrical structure that means you switch source and drain nothing will change right but there is a reason why we referred to the left side of the source and this to as drain. Please I am leaving as a question for you people please try to find it answer this also this questions internally or through your friends or through your colleagues or through your mentors anybody. But get this question done before you moved.

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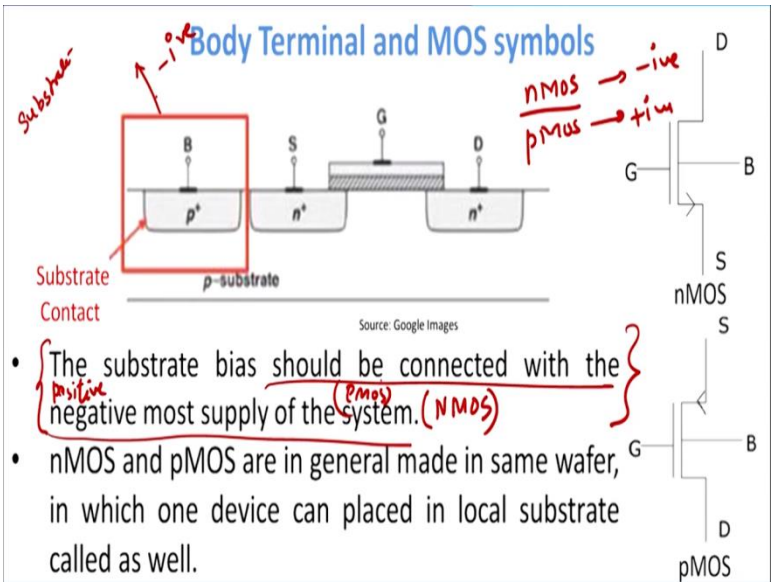

With this knowledge we therefore present to you with this slide which tells you is basically a so what we did? Please if you if you look pretty closely till now we were not referring to we were only referring to this part of the whole structure. So I have the source i have this drain, I have a

gate, I have an oxide layer, I have a metal layer and these are metal semi-conductor contact which is seen in front of you this is your substrate.

So this is basically P type agreed but you can also have a fourth terminal which is referred to as a substrate contact. So substrate is generally back of the chip so substrate also give a bias here right I can give a Bias here right I can give a bias in substrate and therefore that will be known as substrate bias or VS or VB we referred to as VB bulk we referred to this as either bulk right bulk device we referred to as this is bulk or substrate either of the two names we give and this is again with respect to source.

So if I if I get term like VSB right it is basically source to bulk right so it is VS – VB which you see. So I can therefore effectively give four potentials at four contacts of the MOS device and I can get variety of currents out of it or variety of electrical characteristics out of it right so that is the gain out of these 3 to 4 slides which we have discussed till now. For most practical purposes please understand this substrate contact is generally contacted or just added to the most negative terminal of the whole system.

We will see why? and later on but just keep that in mind that when you making an NMOS, NMOS means when your carriers are electrons that time you generally connect the substrate to the most negative terminal of the battery. If it is PMOS then you connect to the most positive so this is for the most negative and this is most positive right that is what is also written here right.

If we look at this part of the slide it is written here that the substrate bias should be connected with the negative most supply of the system this is only applicable for NMOS the sentence. When you have PMOS the substrate bias should be connected with the positive most positive most supply of the system this is for PMOS right. So now you know why we will do that we will see later on that is convention which we follow just as the convention as the source end you generally put a ground.

Similar convention is that if you do not want the substrate to make your life difficult try to make the NMOS substrate go to the most negative terminal or 0 terminal and for PMOS try to make it to the most positive terminal. With the convention, let me therefore with this knowledge we have

understood the basic concepts of this design let me give you the schematic how do you how various books gives you the schematic right.

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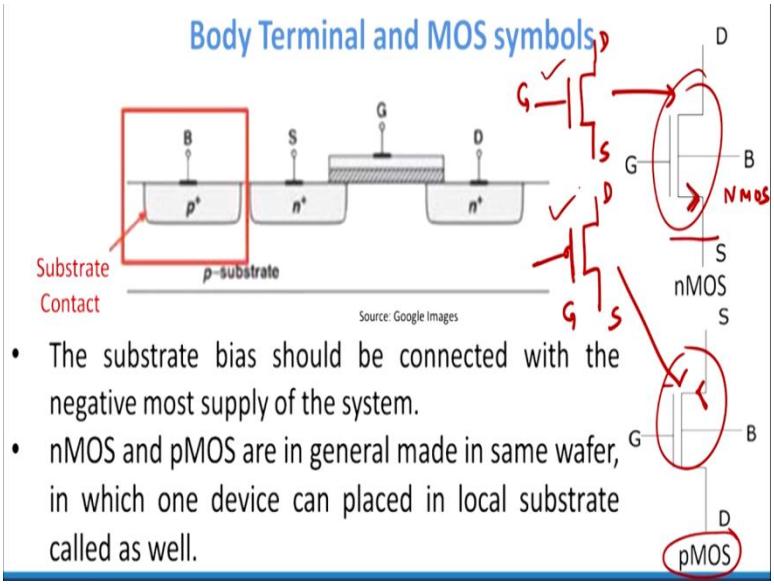

The first is basically this one right where you have got a source, gate and a drain and this is arrow which is going from gate to drain gate to source and this type of is known as NMOS right. Similarly you can have another device in which the arrow is from source to gate right then we define that to be as PMOS. Am I clear? That when you look at NMOS or N metal oxide semiconductor field transistor the arrow head will be going from gate to source and when PMOS it will go from source to gate right.

We will discuss this why is it like that in the subsequent slides but this is what we will the convention is. Another convention is people follow in most of the cases is for NMOS it is something like this they do not do anything but for PMOS they put a small circle in front of the gate so this is gate this is your drain let us suppose source, drain, source, gate this is for NMOS and this is for PMOS.

So in PMOS so some books we will find this structure in some books we will find this structure but do not get confused both of the same thing and both work in the same methodology. Let me come to the explain to you the a process which generally which you see in front of you.

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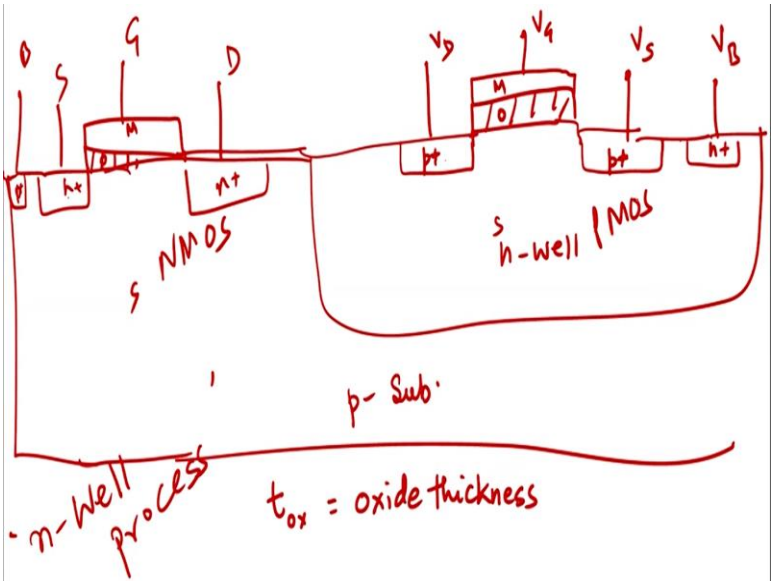

If you look at the process quite interesting that I will explain to you why and how it does you generally make this to be as so I have got this is known as n well right I have a P substrate here right I have an n well here so I make p+ p+, I make oxide here, I make gate this is your VS let us suppose this is your VD right and let me just make a small correction here and give you an idea now this is an n well.

So this is my drain source right this one here you will have n+ and this will be your bulk or your substrate. Similarly so this is a P substrate here I can directly draw n+ n+ here right and I will have gate so this is my oxide layer and this is my gate VG and this is my oxide layer so oxide thickness generally referred to tox. Tox is referred to as oxide thickness in VLSI design for more practical reasons right and this is the metal, this is oxide this is semiconductor here metal oxide semi-conductor.

Then you will also have a bulk here right this is p+ and there will be bulk here so I will have drain here I will have source here right. So this is the overall structure this is also known as n-well process. So what is a n-well process, it made an n-well out of which I made so don't you think this is PMOS because your source and drain is having very large amount of holes here and this is basically n+ n+ region and therefore this is basically and NMOS.

So I have the I have NMOS here right and I have PMOS here fine. This is known as n-well process for understanding purposes or for giving an idea about what this is all about. Let me

explain to you very two important issues before I move forward that let me therefore explain to you to how does a MOSFET work actually because that is the basic idea or a basic concept which we need to find out.

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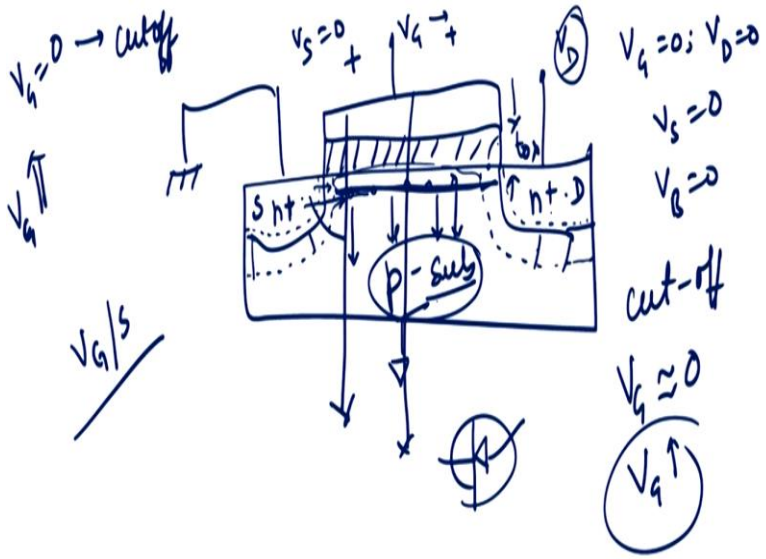

If you look back a MOSFET actually as I discussed with you if you let me again redraw the same figure right and assuming that there is no wall there is no side diffusion I have n+ n+ I have got here right VG and I apply here drain voltage here I have sources grounded so let me apply VS = 0 and this is my P types substrate I have not used this P substrate right I have oxide layer here and my tox here and so on and so forth.

Now let us see how it works out this is n+ n+p so if you do not apply any bias anywhere across the board you will start getting a depletion region which is equally spaced in the n types as well P type on the n+ region there will be depletion region very very thin depletion region will be there. And this depletion region will have equals spacing this distance this distance, all will be equal because this substrate is throughout the substrate but doping concentration is fixed throughout this region and this region the doping concentration is also fixed.

Therefore the depletion thickness between this point and this point is also same not only that if you do not apply any think else as it is basically depletion region it is devoid of any free charge carriers this will have large amount of holes available right because it is a p type substrate so

there will be large amount of holes there will be no electrons at this point. So there is no direct path between the source and the drain for the electrons to move from source to drain.

So this is the case when your tap has been closed and there is not water flowing from source to gate in this case I will assume that VG = 0, VD = 0 of course VS = 0 and assuming that the bias potential is kept at 0 voltage which means that VB is equal to 0. Under such a criteria we will see there will be no charge carrier flowing through the device right and this mode of operation is defined as the cut off mode of operations this is defined as the cut off mode of operation when my gate voltage is very close to 0 and I do not have any electrons available at this point here right and there is not channel formation can taking place here.

Let us do now let us do something else let me keep my VD fixed equal to 0 VS also equal to 0, I also do not touch my bulk voltage but now I start to increase my gate voltage right. So the first condition was when VG was equal to 0 I defined that to be a as cut off now what I do I start increasing the value of VG make it 0.1, 0.2, 0.3 so on and hence so forth. As I start making it higher and higher what do you think what will happen initially and will discuss this in detail we will think that assume there is a gate voltage here these holes which were near the silicon-silicon di oxide interface which holes these holes near the silicon-silicon di oxide interface right.

These holes will actually will do what start getting repelled on this side. Why because they will if I apply a positive gate voltage there will be electric field which will be directed from metal towards the bulk through the oxide layer agreed if there is a electric field this holes will be shifted down to the bottom towards the substrate. As they get shifted here you will be left with only a depletion charge here which means that what depletion charge you will have ND- which means that you will only have fixed ion available to you which fixed ion the negative type dopant species which are available here right.

As the result what will happen is you will have here is a depletion region available in these two points right. When there is a depletion here right there will be depletion here agreed. So still there will be no current flow which means that you increase the gate voltage no current flow till now but still we go on into the gate voltage. Please understand the gate is positive right and this is grounded.

So I am basically forward biasing my gate to source so if I replace this by sorry let me do one thing therefore that if you look at the source end so I can therefore replace it by a PN junction right this can be replaced by PN junction here till 0.7 nothing will happen beyond 0.7 there will be break down and there will be electrons coming from this end to this end and as it comes here though the drain voltage is at 0 volt but this electron coming out and reaching at this point sees a large potential even at this end right. So let me make it once again the clear whole thing cleare.

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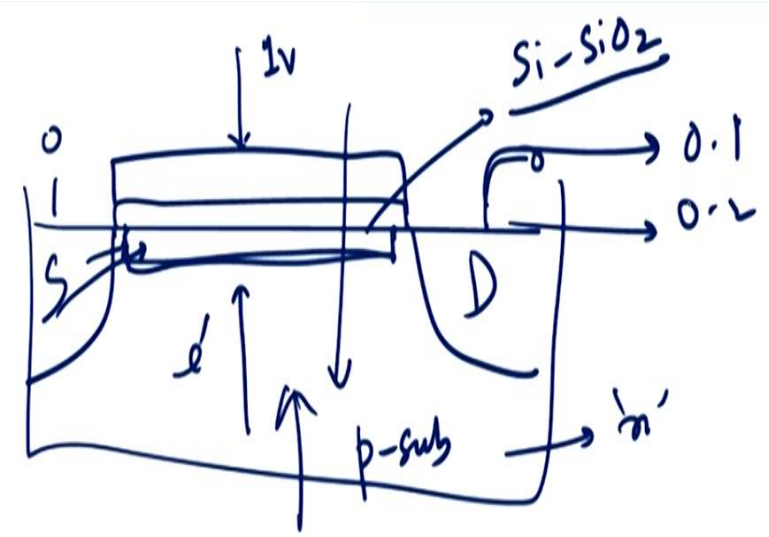

So what does it see as it comes out you have a source drain here as I just comes out from here it see some of the applied gate voltage of 1 volt here so this is 0 this is 0 right it is still see 1 volt here approximately 1 volt here. So there will be thin sheet of electron which will be lying between these two points who has supplied it partly supplied by the gate also please understand partly supplied by the bulk.

So though bulk is basically P type substrate there will be some minority current and carries known as electrons for which this electric field which is directed inwards electrons will be actually moving in this direction. So at certain gate voltage there will be large number of carriers available near the silicon-silicon di oxide interface right there will be large number of carriers and this large number of carriers will result in a small channel being formed between source and drain.

Now if you apply a drain bias say 0.1 or 0.2 there will be electric field which will drag the electron from source to drain resulting a current. So this is how functionally a MOSFET basically works a MOSFET gives you MOSFET works initially as such. So you should be aware so therefore what you have learnt all these discussions is that we have learnt that a MOSFET as I discussed with you can have therefore n type MOSFET and P type.

When you can have P type when this P type substrate is replaced by n substrate this n+ region is replaced by p+ this is p+ and you apply a gate voltage which is negative indirect in dimension. So in NMOS you apply gate voltage positive drain voltage positive in PMOS you apply gate voltage negative and P and drain voltage negative very important when we study CMOS in later stage.

So what we have done till now is we have understood therefore that I can have a NMOS I can have a PMOS so this is what the n+ structure is I can have NMOS and PMOS I can have NMOS replaced by a PMOS doing what simply having a P type substrate replaced by n type substrate right and this is enhancement mode device we will discuss just now and will show to you how it works out right.

So please to recapitulate the whole thing for n type enhancement mode MOSFET we will discuss what is enhancement mode or n type devices substrate should be P type your source and drain region should be n+ region and you have to apply a gate voltage which is positive drain voltage which is positive to get a current. Whereas for a P type MOSFET you require a negative gate voltage and negative drain voltage but you also require an n type substrate and P+ P+ as the source and drain region available with you fine. With this knowledge we will be come to the type of MOSFET available to us.

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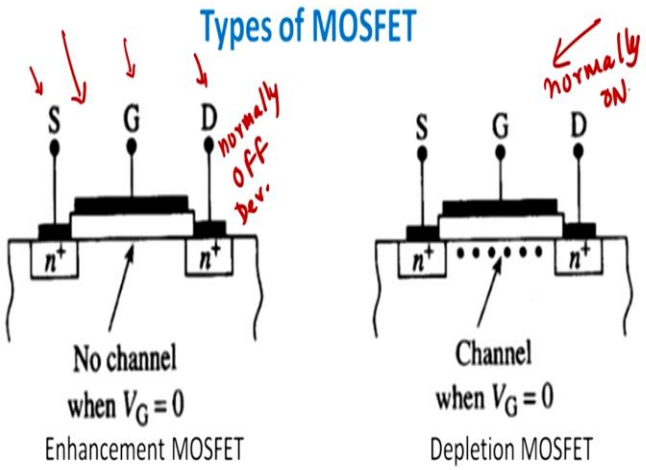

- Throughout the course we will discuss about Enhancement MOSFET.

As I discussed with you in first slide the two type of MOSFET's available to you are enhancement mode and depletion mode this one is basically enhancement this one is depletion let me look at this here enhancement mode MOSFET. Enhancement mode MOSFET is exactly what I discussed with you about few minutes back why enhancement please understand it is also known as I explain to you it is also known as normally off device.

It is also known as normally off device why it is known as normally off see if you apply a gate if you did not apply any biases on the source when did you when you did not apply any bias here or here you did not have any channel between n + and n+ region fine there is no channel no current which means that under no bias condition and no bias condition there will be no current flowing between source and drain.

This is the most fundamental element of enhancement mode MOSFET therefore for enhancement mode MOSFET I have to apply a gate voltage to get the channel being formed and a current being flown between source and drain right. Now let me therefore explain to you what is depletion mode MOSFET? Depletion mode MOSFET on the other hand is basically also referred to as the normally on device why it is on device?

Why I will tell you why? Very simple very basic fact if you replace this by let us suppose I have this device right if I replace this p type substrate by n type substrate when even with source = 0 gate = 0 at drain = 0 even have large electron available between these two arms and therefore

there will be large flow of electron between source and drain if you apply a drain voltage greater than 0 right.

So if your VD is greater than 0 you will have current flow this is known as depletion mode MOSFET which means that under application of no potential if there is a channel being formed we define that to be as depletion mode MOSFET right so we just now learnt two type of MOSFET one is known as enhancement mode MOSFET one is known as depletion mode MOSFET for all practical purpose throughout this course we will be concentrating on the enhancement mode MOSFET right.

So therefore we will define so that is what we have written here throughout this course we will be actually discussing only about enhancement mode MOSFET of all practical region for all practical purposes.

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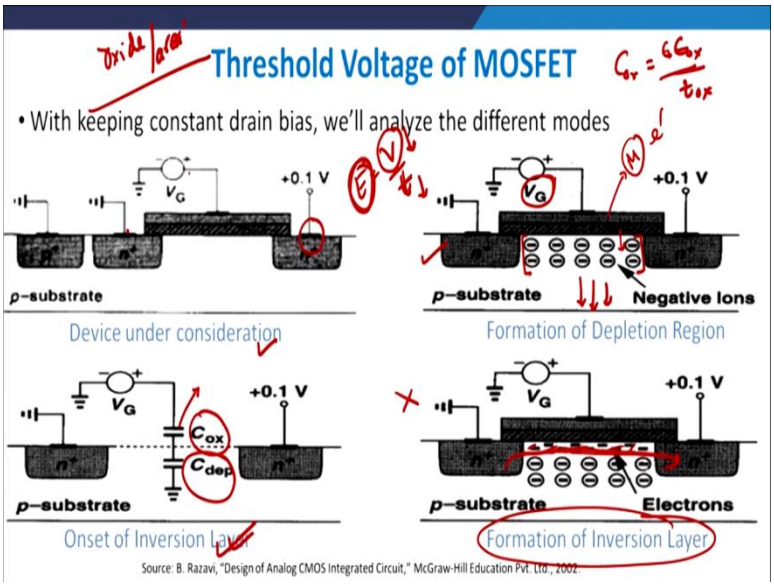

So we have just not discussed this phenomena as I discussed with you that if you apply a gate voltage here right if you apply a source is grounded you applied a positive gate bias right now you what you do what is a gate as I discussed with you in the previous term you increase the gate voltage as you increase the gate voltage the negative ions which you see in front of you gets accumulated here and all the free holes are pushed back into the substrate right.

So now what you have is basically two ox, two capacitor is in series why you will have one cox, cox is what cox is nothing but epsilon ox by tox right epsilon not into epsilon ox by tox. Tox is the oxide capacitance thickness which you see in front of you why because you know very well from your basic electro statics that if you apply and if you have two charge, if you have two chargers right separated by a dielectric or a or a separated by dielectric in this case it happens to be silicon di oxide then we referred to as a capacitor.

Look at the look at the oxide layer the oxide layer on one side as got it is a metal so large electrons are there on the other side it has got large number of negative ions agreed they are not mobile they are fixed but they are charged nonetheless therefore this oxide capacitance tox place a vital importance role and therefore that is referred to as cox.

Cox is referred to as for all practical purposes we will look at cox is oxide capacitance per unit area right we will discuss this later on we will come to it. But oxide capacitance per unit area which means that if you reduce your oxide thickness and the gate comes at a very close contact with the channel right. You actually start to increase the electric field as well as you also starttend to increase cox value.

Which means that I can have large amount of charges getting accumulated on the interface silicon-silicon oxide interface. So tox place a very vital role in determining at what point will the device switch from on to off state. As a brief inside let us suppose tox has been shortened or it been reduced then let us suppose at 2 mega volt per centimeter right 2 mega volt per centimeter in the transverse direction in the lateral direction you had the channel being formed.

You lower your toxide therefore now you required a lesser amount of gate voltage to form the same amount of electric field are you getting my point electric field is defined as voltage by distance t. So if electric field is constant right for the same amount of V to be available with you or the same amount of or if you if you for example if you reduce the tox right you can as well reduce the value of voltage in order to have the same value of electric field and therefore your threshold voltage will start to fall down right we will we will discuss this as and when but just keep I mind that tox place a very vital role in tox means the oxide thickness right place a very vital role in switching of the device.

So as I discussed with you, you will have one oxide capacitance thickness you will also have onedepletion layer capacitance thickness here right. You will have one depletion layer thickness here as well and there will be in series right. Now after we have done this we have done this we have done in onset so this is known as onset of inversion we define this last diagram which you seen for in front of you is basically the formation of inversion layer.

As I discussed with you earlier in this case now very near to the silicon-silicon dioxide interface this area we will have large number large carrier available which charge carriers electrons right and therefore there will be channel form between this and this into form the channel a gate voltage.

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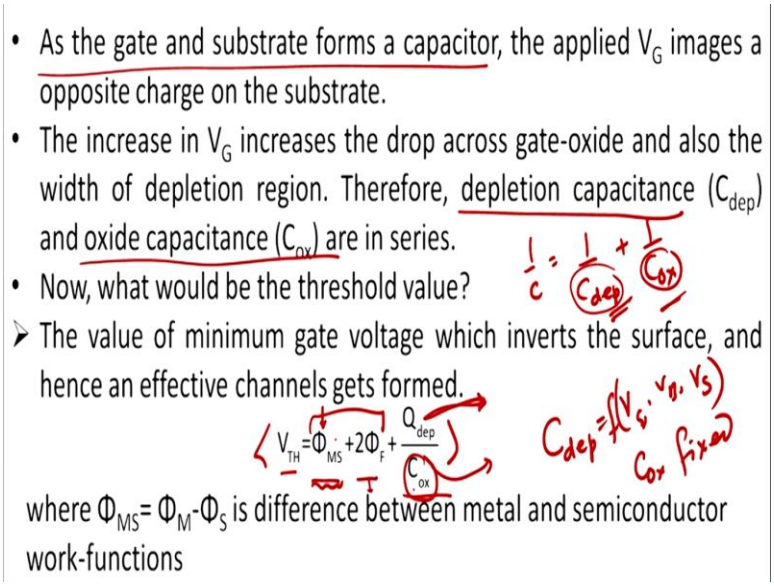

With this knowledge whatever written in this slide is basically the same thing as the gate in the substrate forms a capacitor the applied gate voltage gives a mirror charge on the substrate opposite mirror charge so negative. The depletion as I discussed with you depletion capacitance and the oxide capacitance are in series. So the overall capacitance which you see will be 1 / C depletion + 1 / cox and will be less than the least please understand.

Therefore the overall gate capacitance will be broken up into c depletion, depletion layer capacitance and oxide capacitance right. But the idea is this depletion capacitance will be vary with various mode of operation but the cox is almost fixed. Because depletion layer will become

high or low depending on the applied bias right therefore c depletion is strong function of bias. So c depletion is a very a strong function of applied bias VG, VB, VS whereas cox is fixed.

So our fixed capacitance which is this one and I have a voltage variable capacitance is c depletion now let be defined therefore the threshold voltage device. Threshold just understand this statement and will come to the mathematical of its later on threshold voltage of a device is therefore referred to as that gate voltage at which the channel is inverted this is the two line which I am speaking to you make it very clear for all practical purposes is that threshold voltage is defined as that gate voltage right at which the channel is formed or the channel gets inverted right.

What do I mean by that inverted means what if you look if you go back to a previous slides here to my initial slide here may be the slide which I discussed with you earlier yes if you look at this slide look at the fact that this is basically p type substrate.

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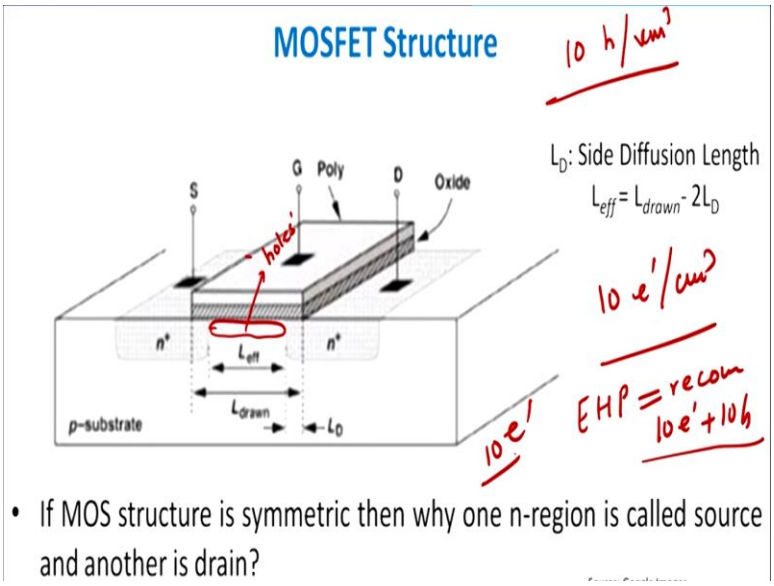

You had a large amount of free carriers which your holes here so this are primarily free charge carriers and they were holes. You have to invert it you have invert it means you have to have as many number of electrons here as where the number of holes before the channel was formed which means that let us suppose you had 10 number of holes per unit area per unit volume let me say per centimeter cube.

Then I defined strong inversion or large inversion to be that region when I will get 10 number of electrons per unit cube. So it is exactly the reverse right so what does it mean you will have suppose you had 10 holes those 10 holes have to be removed and you have to add extra 10 electrons to it then we define that to be as a proper inversion fine is it clear?

Therefore as simple common sense into the mind we will be requiring 20 holes per centimeter cube in order to invert the channel why? 10 holes will be required to just recombine the holes so we will have electron hole per combination will be there, there will be recombination how many combination 10 electrons + 10 holes will recombine and you will have depletion of charge carrier and then you have to add extra 10 electrons over it in order to have the inversion of the channel and you have formed this point if it able to do this point very easily.

So therefore coming back to initial slides here we saw that now we define threshold voltage is as VTH = Phi MS+2 Phi FS+Q depletion / Cox this is the depletion charge by unit area C oxide is oxide capacitance charge per unit area and these are all the potentials which you see in front of you and this is known as the work function difference between Phi MS.

$$V_{TH}=\Phi_{MS}+2\Phi_{F}+\frac{Q_{dep}}{C_{ox}}$$

These are all material dependent properties phi MS and 2 Phi F these are all material depends properties these this is also material depends properties and this is basically depending on the type of doping concentration which you have done.

So per say threshold voltage is a parameter which is only dependent on the process parameter of the device which means that once you have fabricated a device at this stage at least without going into substrate effect or body effect at this stage you can very well appreciate that given a device I can actually have the threshold voltage fixed if the doping concentration are fixed the dimensions are fixed threshold voltage is always fixed right.

So with this knowledge we will move to the next slide so this takes care of the basic fundamental concepts of device we now move to the next which is basically current voltage characteristics here and we will just look into the i how I derived the for the current equation in a MOSFET. So

to conclude the whole issue which we have discussed before so therefore in previous slides explained to you how a basic MOSFET works?

What are the mode of MOSFET's various enhancement mode and depletion mode MOSFET what is the meaning of threshold voltage very critical factor and therefore we are now in a position to explain to you how the current voltage current characteristics of a MOSFET is derived thank you.