

**Advance Power Electronics and Control**  
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**Lecture – 28**  
**PWM Techniques – II & MLI**

Welcome to our NPTEL courses on the advance power electronics and controls. We shall continue with rest of PWM techniques. We will start with sign PWM there after we will try to cover multiple level inverter so as we were discussing in our previous class.

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### Sinusoidal Pulse Modulation

- In this method, several pulses per half cycle are used as in the case of multiple pulse modulation.
- But width of each pulse is modulated proportional to the amplitude of sine wave.
- Gate pulses are generated by comparing sinusoidal reference signal with triangular carrier signal.
- Frequency of reference signal ( $f_r$ ) decides the frequency of output voltage.
- The ratio of  $V_r/V_c$  is called the modulation index which controls the output voltage.
- Number of pulses per half cycle depends on the carrier frequency ( $f_c$ ).

That sinusoidal PWM actually an extension of the multiple PWM where actually the modulating wave form instead the square wave we have sin wave. In this method several pulses per half cycle are used as in the case of multiple modulations. But each pulses is modulated proportional to the amplitude of the sin wave. So, in case of multiple convertor square wave we have got all the pulses with the same width.

But you will have a variable frequency variable width pulses throughout it in central of the fence you will have actually more width in the 0 crossing you will have a less width. Gate pulses are generated by comparing the sinusoidal reference signal will with triangular carrier signal. Frequency of reference signals decides the frequency of the output voltage the ratio of  $V_r/V_c$  is

called the modulation index which controls the output voltage and number of pulses per half cycle depends on the carrier frequency the ratio of this.

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## Sinusoidal Pulse Modulation (Cont...)

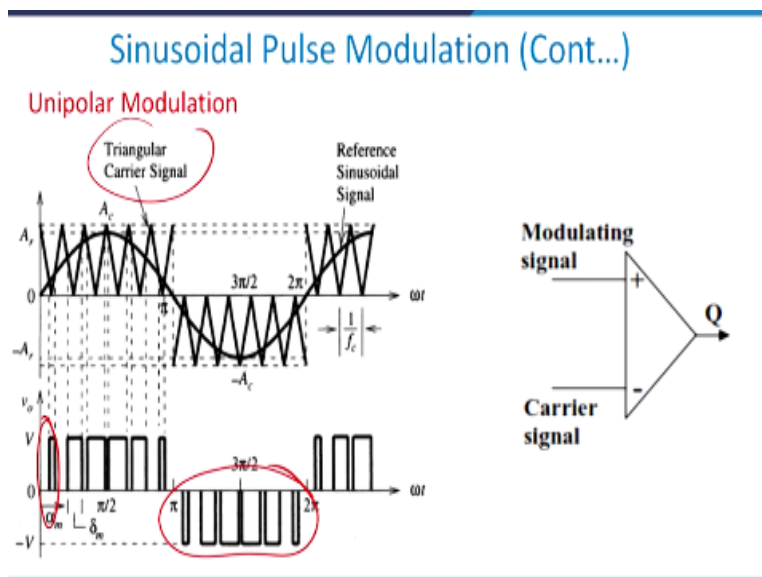
Two types of SPWM is possible generally

1. Bipolar voltage switching
2. Unipolar voltage switching

In bipolar PWM the output voltage waveform contains more harmonic content than the unipolar PWM

Actually the carrier frequency of the modulating frequency this is the two type of the SPWM one is bipolar and another is unipolar. Bipolar we will have a more harmonic and more disadvantages. For actually time constraint we are going to discuss only the unipolar switching technique the bipolar output voltage wave form contains more harmonic. Then that unipolar PWM so far this reasons our discussion considered only the unipolar PWM.

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So, this is a triangular wave and it has a frequency as much as high as actually 20 times and you have a sinusoidal form you can see that at the 0 crossing weight is less and we will carry like this and if you have this kind of pattern so this is called the unipolar modulation. It is very easy to implement so one half cycle you have a shifted wave then afterwards negative half cycle multiply with that minus one.

And we will have this shifted wave and accordingly the carrier will be gate pulses will be generated and this will be compared with the op - amp. Very simply it will circuit modulating signal and carrier signal bandwidth of the op-amp required to be at least 10 to 15 times higher than the carrier wave to operate it properly and then he will have a pulses so modulation index.

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## Sinusoidal Pulse Modulation (Cont...)

What is Modulation Index?

- ❖ Modulation index is the ratio of peak magnitudes of the modulating waveform and the carrier waveform.

$$m = \frac{V_m}{V_c}$$

- ❖ MI controls the harmonic content in the output voltage.

Modulation index is the ratio of peak magnitude of the modulating waveform and the carrier wave form. So,  $m = V_m/V_c$  so this MI moderating and controls the harmonic content of the output voltage.

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## Sinusoidal Pulse Modulation (Cont...)

- ❖ By increasing the number of pulses (N) per half cycle, the lower order harmonics get cancelled. But higher order harmonics will get increased.
- ❖ Higher order harmonics can be filtered out easily.
- ❖ Higher value of N results in more switching losses and leads to reduction of efficiency of inverter.

Let see how does it done by increasing the number of pulses in both half cycle the lower other harmony it get cancelled and what happened actually you are shifting the spectrum to the ratio types. If it is actually one kilo watts carrier frequency and a 50 year cycle should be shifting this actually this frequency band multiple by the 20 times more so but higher order harmonics will get increased that is the 04.46 ratio.

Higher order harmonics can be filtered out easily because essentially all those devices you got a copper you got an inductor. All the machines will have inductors your conducting line will have an inductor and thus all will actually help you to actually minimize the effect of the higher order harmonics. Higher value of m is more but leads to more switching loss. And that will reduce the efficiency of the inventor and moreover we have discussed about the devices.

If you know we require we have a prescribed frequency for the prescribed switching frequency for the prescribe devices. If it is GTO it cannot be operated over and above 2 kilos. So, around if you wish to go above the 2 Kilo horse you have to be settled with the 05:49 so power rating is quite low then. And then if you take a higher than this eligibility switch over to the MOSFET then MOSFET can handle power only in the range of the hundreds of watts.

So, this is basically we have to see to it that it is not that can constraint that we can increase the carrier frequency. Nowadays we have a very high processor and it can generate the digital pulses at a very high switching frequency but considered also imposed by the features.

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## Sinusoidal Pulse Modulation (Cont...)

What is Over Modulation?

When the peak magnitude of modulating signal exceeds the peak magnitude of carrier signal, the PWM inverter operates under over-modulation. During over-modulation the output voltage increases slightly.

So, what is over modulation? When the peak magnitude of modulating signal exceeds the peak magnitude of the carrier signal the PWM inverter operates under over modulation during over modulation the output voltage increases slightly but you will generate more and more harmonics.

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## Sinusoidal Pulse Modulation (Cont...)

- Harmonics of 5% is allowable in an inverter output voltage.
- But inverter output voltage contains more than 5% of harmonics.
- Filters can be used to reduce the harmonic content.
- Small size filter is enough for reducing higher order harmonics.
- But a bigger size filter is required for reducing lower order harmonics.
- This makes the system costlier and leads to poor performance.
- Hence a system without filter is needed to suppress the harmonics.

So, harmonics and there is an i triple e standard by i triple e 5.19 all those standards are there that actually tells that the value of the allow harmonics of 5% is allowable in an inverter output

voltage. So, voltage THD allowed to be around 5% but inverter output voltage contains more than 5% harmonics filter can we use to reduce the harmonic content so that is that actually the bottom line of it.

You have to when you are giving to the customer so THD content has to be less than percent smaller the size of the filter is enough for reducing the higher harmonics and thus it is become a natural choice to use sign PWM grid with high switching frequency but bigger the size of the filter is required for reducing the lower order harmonics. It makes the system costlier and leads to the poor performance of this devices.

And hence the system without filter is need to be suppressed the harmonics now you will see that let us now do the analysis of the unipolar PWM.

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### Sinusoidal Pulse Modulation (Cont...)

#### Harmonic Reduction by PWM

Several pulses per half cycle reduces the lower order harmonics.



As the waveform is symmetrical during every quarter cycle,  $a_n=0$ .

$$b_n = \frac{4}{\pi} V_s \left[ \int_0^{\alpha_1} \sin n\omega t \cdot d(\omega t) - \int_{\alpha_1}^{\alpha_2} \sin n\omega t \cdot d(\omega t) + \int_{\alpha_2}^{\pi/2} \sin n\omega t \cdot d(\omega t) \right]$$

$$b_n = \frac{4V_s}{\pi} \left[ \frac{1 - 2 \cos n\alpha_1 + 2 \cos n\alpha_2}{n} \right]$$

So, you have triggered an angle alpha again it will be triggered after angle alpha two and so on. And we will have a kind of variable frequencies so we can find it out. We have an order of symmetry that is only sign component will be preserved. And so  $B_n$  will be  $4/\pi V_s$   $\int_0^{\alpha_1} \sin n\omega t \cdot d\omega t$  thereafter – because here you get –  $\alpha_1$  to  $\alpha_2$   $\sin n\omega t \cdot d\omega t$  + again actually  $\alpha_2$  to  $\pi/2$  till this much  $\sin n\omega t \cdot d\omega t$ .

So, if you can substitute and you can get  $B_n = \frac{V_s}{\pi} [1 - 2 \cos n \alpha_1 + 2 \cos n \alpha_2]$ . Now you can actually this is a concept of selective harmonic elimination technique. You can choose you can make the value of the  $B_n$  is 0 by this 9.29 0. So, if you have 2 pulses this is an actually you can choose the  $\alpha_1$   $\alpha_2$  and salt online. To make this value 0 and particular harmony can be eliminated.

For example, you can take a case that we want to eliminate the third harmonic and the fifth harmonic and rest of the harmonic says high order. So, it can we filter it out.

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**Sinusoidal Pulse Modulation (Cont...)**

If 3<sup>rd</sup> and 5<sup>th</sup> harmonics are to be eliminated,

$$b_3 = \frac{4V_s}{\pi} \left[ \frac{1 - 2 \cos 3\alpha_1 + 2 \cos 3\alpha_2}{3} \right] = 0$$

$$1 - 2 \cos 3\alpha_1 + 2 \cos 3\alpha_2 = 0$$

$$1 - 2 \cos 5\alpha_1 + 2 \cos 5\alpha_2 = 0$$

$$b_5 = \frac{4V_s}{\pi} \left[ \frac{1 - 2 \cos 5\alpha_1 + 2 \cos 5\alpha_2}{5} \right] = 0$$

$$\alpha_1 = 23.62^\circ \text{ and } \alpha_2 = 33.304^\circ$$

Using  $\alpha_1$  and  $\alpha_2$ , voltages of 7<sup>th</sup>, 9<sup>th</sup> and 11<sup>th</sup> harmonics are found as,

$$b_7 = \frac{4V_s}{7\pi} [1 - 2 \cos 7 \times 23.62 + 2 \cos 7 \times 33.304] = 0.31555 V_s$$

$$b_9 = \frac{4V_s}{9\pi} [1 - 2 \cos 9 \times 23.62 + 2 \cos 9 \times 33.304] = 0.5202 V_s$$

$$b_{11} = \frac{4V_s}{11\pi} [1 - 2 \cos 11 \times 23.62 + 2 \cos 11 \times 33.304] = 0.3867 V_s$$

So, the equation is actually for  $B_n$  you can substitute actually all those things will be 3 so you will get this equations and for fifth harmonic you will have this and this should be called 0 and ultimately 1.018 to this equation and you can solve and will solve your  $\alpha_1$  should be 20.3 degree and  $\alpha_2$  should be 33.3 so what is the advantage of it. So, you can get eliminated  $\alpha_1$  and  $\alpha_2$  by and thus get rid of the lower order harmonic take 3rd and 5th.

And by using the same equation we should have a multiple pulses we can eliminate the 7th 9th and 11th harmonic and so you can find it out that if actually 3rd and 5th is eliminated so what should be the harmonic content of the 7th harmonic what should be the harmonic content of the 9th harmonic what should be the harmonic content of the 11th harmonic so accordingly order you are getting the THD prescribed by the standard or not.

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### Sinusoidal Pulse Modulation (Cont...)

The amplitude of the fundamental component for these values of  $\alpha_1$  and  $\alpha_2$  is,

$$b_1 = \frac{4V_s}{\pi} [1 - 2 \cos 23.62 + 2 \cos 33.304] = 1.0684 V_s$$

The amplitude of the fundamental component of unmodulated output voltage wave is,

$$b_{1, \text{un}} = \frac{4V_s}{\pi} = 1.27324 V_s$$

- The amplitude of the fundamental voltage is 83.91% of the unmodulated wave. So inverter is de-rated by 16.09%.
- Additional eight commutation per cycle increases switching losses.

Now the amplitude of the fundamental component of the value alpha one and alpha two is so you can substitute these values. So, ultimately the fundamental value we will have a 6% increment so that is 1.06 the amplitude of the fundamental component of the unmodulated wave form is actually  $4V_s/\pi$  so that value is essentially 1.27 but it will have a degradation of this value from this unmodulated form but you get lower THD.

The amplitude of the fundamental wave form is 83% of the unmodulated wave form so inverter is de rated by 16% if you wish to use this sign (()) (12:16) wave selective harmonic elimination that additional 8 commutation per cycle is increases also due to the switching losses. So, these are the few take on from the multi pulse sin wave inverter.

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## Multilevel Inverters (MLI)



Multilevel Inverter (MLI) basically generates more than two level of output voltages from the DC voltage at its input.



Sl. No.	Conventional Inverter	Multilevel Inverter
1	THD is high in the output waveform	THD is Low in the output waveform
2	High Switching stresses	Low Switching stresses
3	Not used for high Voltage applications	Used for high voltage Applications
4	High voltage levels cannot be produced	High voltage levels can be produced
5	High dv/dt and EMI	Low dv/dt and EMI
6	High switching frequency, increased switching losses	Lower switching frequency, reduced switching losses

So, now let us discuss about a very important topic that is still now we are discussing about your PWM inverter now we shall discussed inverter topologies that is multi level important why we require a multi level important. Essentially what we have discussed now we have restricted ourselves to the 2 level inverter. Why we require multilevel inverter? Is that first of all there is logic behind it.

Let us consider simple buck logic but it has to be since it has to be SC so it has to be like this. But what essentially you are doing you know you get one while you are switching on. You can have this voltage or 0 ultimately you will have that whole area match with this or you may have a sinusoidal wave form or you will actually. So, this vault area will match ultimately to match this volt area essentially what you will do.

You will inject more and more harmonics so but let us consider a simple case of a when you switch on it gives 12volt but you require a 5 volt instantaneously. So, you will match you will apply to 12 volt for small interval of time. Rest of the time you will apply t0 and thus you say that actually this volt 14.07 matches theoretically it is okay but what happened? The power quality decreases so you require a sinusoidal voltage and once you switch on.

When you have an almost a 0 voltage you are applying a whole DC voltage then what happens? You say that actually volt idea matches but within that area essentially it is fill up by the

unnecessary harmonics. But assume that you have steps you can apply 6 volts as well as the 12 volt so once you want to generate 5 volt you can turn on only 6 volt. So, there is a less instantaneous error between the applied voltage and the actual voltage require.

And thus that actually unnecessarily harmonic generation will be lower and this is the basic essence of go for the multi level inverter so conventional when means actually we say that it is two level and if it is more than 2 level. It is multi level it can be any level so as I discussed THD of this voltage wave form and the output of this two level inverter will be higher because of instantaneous difference of the applied voltage and the actual voltage.

And THD is low with the output voltage because you applied voltage and actual voltage has less instantaneous since you are switching on whole DC bus volt switch you are getting plus this actually the poll of the essential inverter goes to plus minus VDC so stress across the switches is quite high but you have a choice. You may apply  $VDC/2$   $VDC/4$   $VDC/6$  depending on the level you have chosen thus you will have less stress on this switch.

Since the device is not available to sustain high voltage and thus these two levels in water cannot be used for high voltage applications as well as the high volt applications. But it can be used since it can block higher voltages and individual switching rating. It reduced in the multilevel inverter it can reuse for that higher voltage rating and applications and high voltage level cannot be produced.

Like we require maybe the HVDC link and all those things there is a rectifications and some ways inversion operation there you cannot achieve this high voltage level can be produced by the multi level inverter since voltage drops heavily our builds up heavily while turn off volt will drop heavily while turn on across the switch and build some heavily across a turn over switch so it will be subjected to high humidity.

And all the switches has to be protected from the ill effect of the high humidity and one of the minutes of this actually high humidity is the emi. So, it will have more electromagnetic radiations and interferences since humidity is less so EMI also will be less since actually we

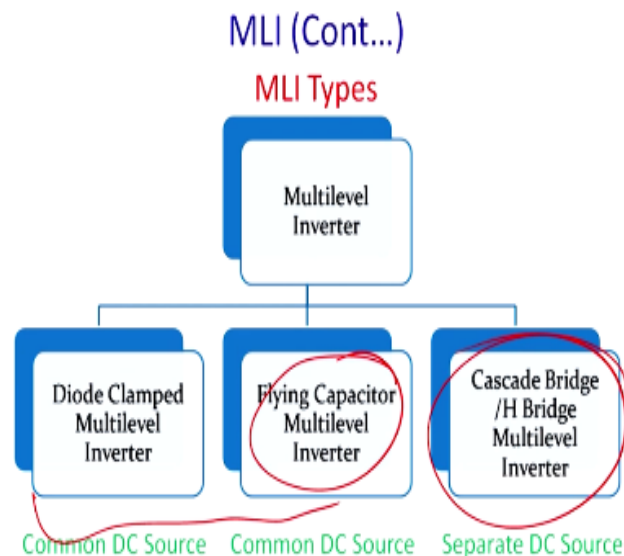
require the same output same THD because we want to ship the THD. So, if you use the two levels in water we require to increase the switching frequency.

To achieve the same THD another e site of the filter and once you increase the switching frequency you increase also the switching losses. So, it will have those more switching losses since it gives a closer THD because of the less error in the instantaneous voltage and the actual voltage. So, size of the filter is already dues you need not have to actually use high switching frequency.

And thus you can use the higher rating switches and which enhances the power handling capability. And apart from that it gives you the decent power quality so due to this all advantages now we have entered into the domain of the multilevel inverter and we have leap and we are now living in inverter on line inverter you see that actually if you have a solar inverter small solar inverter in a roof top or in any other places.

Then also multilevel inverter to reduce the size of this actually the filters and apart from the high power applications now let us sees their classifications of these inverters.

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Multi level inverter can be broadly classified into 3 categories sometimes it is actually this can be this coupled and this has been kept aside. So, anyway we decided to actually go back

conventional classification one is diode clamped multilevel inverter we see that topology we will find that actually there are many diode put into the system and if the level goes very high the number of diode is also increasing like anything.

Anyway so we shall see that advantage and disadvantage of the diode clamped multi level inverter followed by flying capacitor multilevel inverter so we will find that actually voltage multiple stage of the voltage is generated by the multilevel level inverter. There the cascade H bridge multilevel inverter these are the 4 these are the 3 multilevel level inverter these 2 can use a common this is also 1.

This source can be used for all the applications and thus we have operating advantages but up and down count will be more generating higher level. It is basically very complex and it becomes bulky and whereas in a cascade multi-level inverter require all those multi level entities request separate resource but it has a very big advantage that it is a modular in nature. You can level them up to any level by the separate DC voltage. So, these are the three main entities of the multilevel inverters.

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**Diode Clamped MLI**

**Switching Technique (5 Level)**

O/P V <sub>ao</sub>	Sa1	Sa2	Sa3	Sa4	Sa1'	Sa2'	Sa3'	Sa4'
V <sub>dc</sub>	1	1	1	1	0	0	0	0
3V <sub>dc</sub> /4	0	1	1	1	1	0	0	0
V <sub>dc</sub> /2	0	0	1	1	1	1	0	0
V <sub>dc</sub> /4	0	0	0	1	1	1	1	0
0	0	0	0	0	1	1	1	1

1. Switching devices :  $(2m - 2)$
2. Input voltage source :  $(m - 1)$
3. No of diodes :  $(m - 1) (m - 2)$
4. Voltage across each capacitor :  $V_{dc}/(m-1)$
5. Line voltages :  $2m-1$

Now let us go to the diode clamped multilevel inverter so here we can generate this is basically a five level multilevel inverter and there are some calculations as we written. So, please understand that choosing devices are  $2m-2$  so these are the IGBT are here at the switching devices. So, it is a

five level so it tells that basically you have  $2^{m-2}$  1 2 3 4 5 6 7 8 so you got 8 such devices and if it is a 3 level so you make it actually 3 here.

So, you will get 4 devices so this much to this much will give you the 3 level and number of voltage source in this case is basically what you required is a capacitor. It is basically this this they are 4 so that should be a - 1. But problem lies with a number of diodes and it is increasing obnoxiously it is increasing like anything like rumour. So, that value is physically  $m - 1 * m - 2$  so here this  $4 * 3$  that is 12 guides.

The thing about what we felt was 11 level inverter so how many diodes would be there so that is one of the drawback of this typology. It employs huge amount of the diode every diode basically consisting of the losses of 0.7 volt and it is since it is a power diode it generally have a losses around 1 to 2 volt and what happened while having a path we will find that it all is close to every single phase for us to at least one at a time.

We will discuss this conduction of different type little later and then what will happen that this leads to a huge loss of efficiency and voltage across each capacitors you can it is a same thing that is  $V_{DC} / m - 1$  and this is something while we studying the output you will get that is the line voltages here we will have a steps of line voltages that is actually 9 steps voltage will come and that is basically  $2^{m-1}$  so you see that how it operates.

So, if you wish to get the voltage at a point a pole of the inverter required to get a PDC all the upper switches all the 4 upper switches required to be on. So, just essay 1 essay 2 essay 3 essay 4 and this has a complete this has basically a simple logic. I do not have time to discuss because this switch and this switch are complementary. Similarly this switch and this switch is complementary this switch and this switch is complementary and this switch and switch is.

And we can see that we have formed this table also so all of upper switch yes is on then you get the voltage equal to PDC. There is 1 1 1 so here you get the voltage hub PDC and the lower should and all the lower switch should be off once you get one switch you get basically  $3 V_{DC} / 4$

so this voltage this switch require to be off and this voltage required to be off ultimately this will be the diode forward biased.

And till this to this it will be all on so all the 4 you will see that at a time or a set of 4 switches are on and gradually it will shift one by one it is just like a switch register. It is easy to design this kind of circuit in a digital domain so this all will be on and since the complementary. There will be 0 so you will get the voltage up plus  $3V_{DC}/4$  + and similarly if you wish to get  $V_{DC}/2$  so here this switch to be off then.

Actually D7 will take care and this 4 switches will be on and lower 2 switches will off similarly for D4 will get on and wish to get 0 voltage that all the switches should be on. Lower switches should be on and ultimately this point should be connected to that this point and assume to be the 0 voltage.

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### Diode Clamped MLI (Cont...)

#### Advantages

- (1) A large number of levels 'n' yields a small harmonic distortion.
- (2) All of the phases share a common dc bus.
- (3) Reactive power flow can be controlled.
- (4) High efficiency for fundamental switching frequency.
- (5) Relatively simple control methods.

#### Disadvantages

- (1) Different voltage ratings for clamping diodes are required.
- (2) Real power flow is difficult because of the capacitors imbalance.
- (3) Need high voltage rating diodes to block the reverse voltages.
- (4) The number of switches, capacitors, and diodes required in the circuit increases with the increase in the number of output voltage levels. Extra clamping diodes required are  $[(m-1)(m-2)]$  per phase.

Now what are the advantages and the disadvantage of the diode clamped multi level inverter the large number of levels can be yielded and thus will have a lower THD and it is a general advantage of all the MLI and not only the resembling all the phases shares a common receivers thus you not required a multiple voltages and multiple sources we will see later reactive power flow can be controlled in this kind of configuration.

We can have a DQ control at different kind of control techniques is employed mostly these are the users for the wind form applications all those cases or the high voltage application where we required to have a PQ control high efficiency for fundamental for switching frequency. That is something we require to understand it fundamental switching frequency we have seen that in case of the selective harmonic elimination is reduced by around 18%.

But here we shall see that you know it has got a higher switching higher efficiency and relatively simple controls that comes with the comparison with the other two MLIs. These are diode clamp actually cascade multi-level inverter because that incident of that clamp capacitor clamp multi-level inverter has a huge number of capacitor then each voltage is actively maintained and thus required more complex control.

Similarly the cascade multi level inverter we required to have a multiple voltage source and it is we all assume that voltage required to be constant. So, these are a few challenges are these are a few advantages of the multi level inverter but of course there are so many disadvantages. So, we shall discuss the disadvantages and we will switch over to the next multi level inverter. Thank you for your attention, we are looking forward to a very exciting next class also.