Flexible AC Transmission Systems (FACTS) Devices

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Lecture - 09
Multi Level Inverter – III

Me to our 9th lecture of facts devices, today we shall continue with the PWM techniques for the multilevel inverter.

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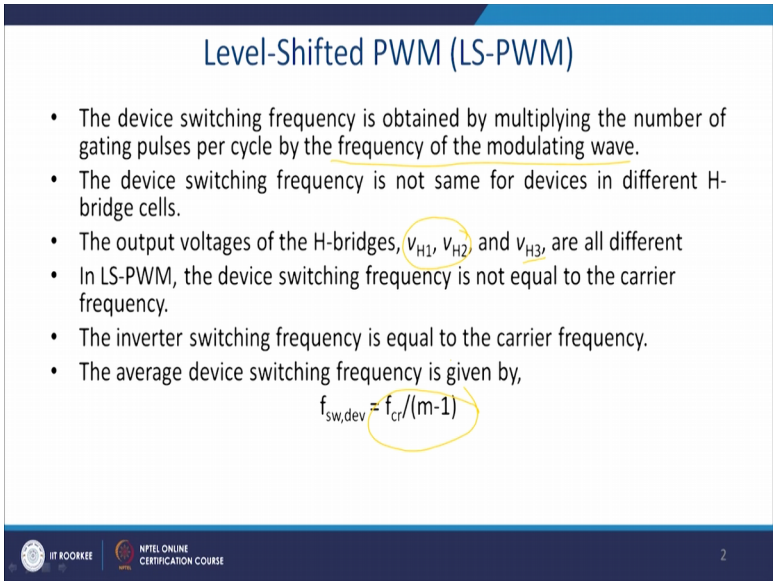

So, we were discussing on previous class with the level shifted PWM. So, what is level shifted PWM, the device the basic features of the level shifted PWM is said that the device, switching frequency is obtained by multiplying the number of getting pulses per cycle by the frequency of the modulating wave.

Moreover the device switching frequency is not same for devices in a different bridge configuration. So, this is one of the disadvantage of it, the duty cycle of the actually RMS current rating and the all those things will be different for the different switches of the H-bridge.

And, output voltage of the H bridge this H 1 2 and H 3 all are different and in level shifted PWM the device switching frequency is not equal for the carrier frequency. So, this is advantages or disadvantageous. So, if it is lower frequency, we can lower frequency and the higher current rating, we can choose a particular devices and we can choose a if there is a lower power rating and high frequency, we can choose a different current it is there is a advantage, we can we uses the advantages we also even though it seems to be a disadvantageous.

The inverter switching frequency equal to the carrier wave frequency there is no change in that and average device switching frequency will be given by actually f cr by m minus 1 where m is the level of the inverter.

Now, let us see that what happened?

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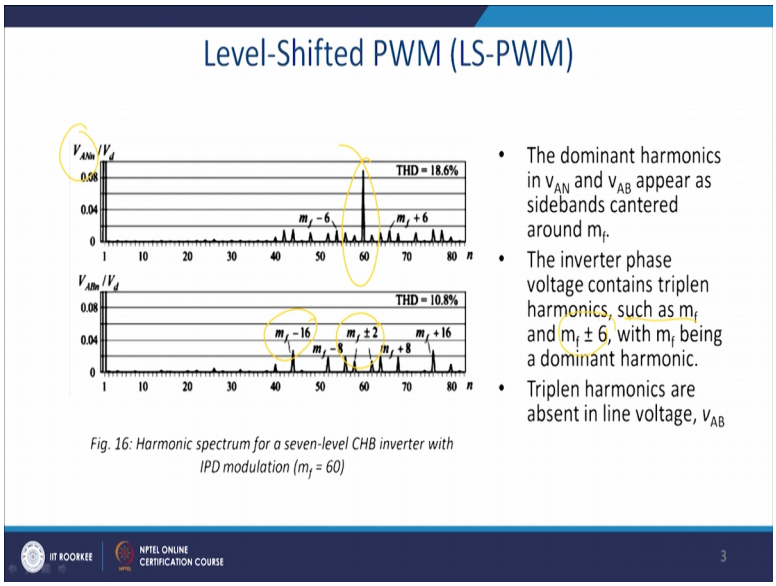

Fig. 16: Harmonic spectrum for a seven-level CHB inverter with IPD modulation (m_f = 60)

In case of the sidebands, and we can see that this is basically the neutral point or the phase voltage and this is basically the line voltage. And, it is basically approximated by the, it is the ratio of V A N by V d.

So, the dominated harmonics it can be seen that V A A N, that is the neutral voltage and

appear as sideband centred around m f. So, you will get the THD an around of basically 16 18.6 percent quite high PWM quite high THD. And in this case you will find that it is harbour around here here here. We have chosen the value of the m f in this case as 60. For example, if you are operating in a 50 kilohertz normal power supply frequency 60 time this is the 3 kilohertz is your switching frequency.

So, what happen here the inverter phase voltage considered as triplen harmonic? Though it will be not be reflected to your line harmonics. And such m f ah and such as m f this is for this reason m f plus minus 6 with the being a dominating harmonic or the triplen harmonics are absent, in the line voltage A B n it is quite clear.

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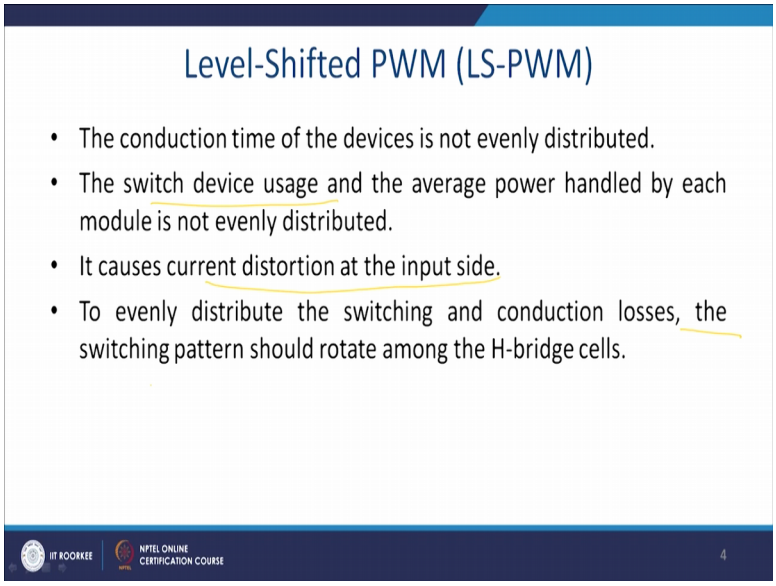

Now, what are the actually take away from this actually level shifted PWM, conduction time of this devices are not continuous and it is distributed among switches. So, thermal rating of the devices can be improved. So, we can use optimally their thermal rating. Switches and so, for this reason the second conclusion comes switch devices and the average for handle by the each switch module, are not evenly distributed. This is one of the disadvantage of it and we required to manage as much as possible by the control logic.

And, it causes current distortion and the input site that is not also advantageous. Because you know that the mf plus minus 6 is present into the harmonic. And to evenly distributing switching and the conduction loss the switching pattern should be rotated among the H-bridge cell, that is something you required to manipulate with the with control strategy.

So, first of all you try to spend more amount of current through a particular H-bridge and maybe you know after 2 cycles later the sequence may change. And accordingly actually you will find that, you will distribute the switching losses or the device rating among all the H-bridge connected in series.

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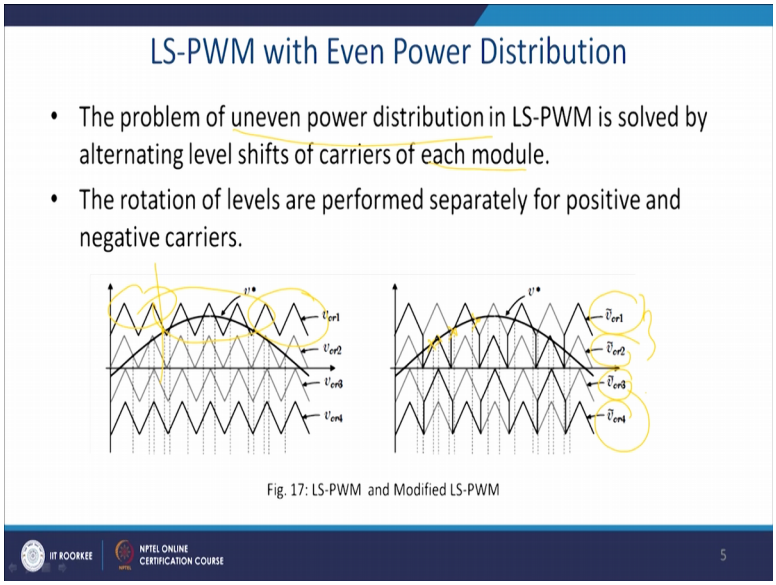

So, this is the sideband PWM with even power distribution. See, that please try to understand it the problem of you know uneven power distributions, in this line shifted PWM is solved by alternating phase shift carrier of the each module.

And, the rotational levels are perform separately for positive as well as a negative carrier. See, that here you know this is the carrier wave. So, you can see that this is the zone where it hardly actually crosses, ultimately switching is mostly done on this part of it and in this part also this is over modulation for this wave. So, there is no actually no

switching if it is a discontinuously on for this duration.

Similarly, in this duration it is continuously off. Same happen to the lower cycle. So, these can be you know something some way or other can be controlled. So, look this is the actually the point it is crosses, thereafter it will point it will crosses, something like. So, this is the carrier this is the control signals for switch 1, this is for switch 2, this is for switch 3, and this is for switch 4 you can see that this carriers are basically crossing.

But, if you interchange in some half cycle you give c r 1 and c r 2 and we can actually optimise the losses.

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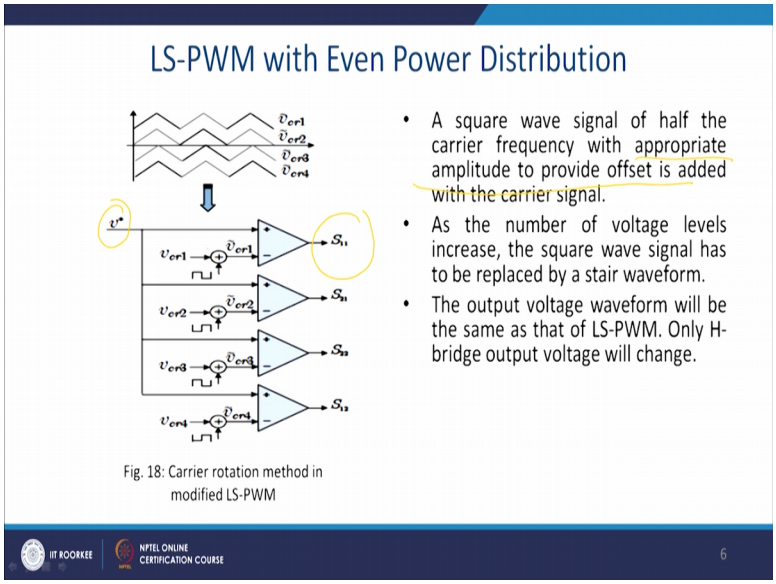

See that what happen here? This is the basically the v reference that required to be tracked the modulating wave and you know you will compare with the c r 1 and ultimately you will have the c r prime, and accordingly when this value is v star or the v reference is more than this vcr delta. So, switch S 1 will be on.

Similarly, see S 2 when we on when this reference voltage is greater than the v c r 2. So, then subsequently other switches will be on. So, what we can how you will generate it a square wave signal for the half of the carrier frequency, with appropriate amplitude to

provide the offset added to the each carrier wave.

So, you will add up. So, it will be shifting positive and the negative half cycle accordingly. As the number of voltage level increases the square of signal has to be replaced by the steer case waveform. Depending on the multilevel inverter if it is more than 3 level you required to be a steer case. And the output of the waveform will be same as that of the LSPWM only H-bridge output voltage will change, in that way this is the simple way to implement LSPWM.

Now, let us combine L S and P S then what will happen then it is said to be the hybrid PWM.

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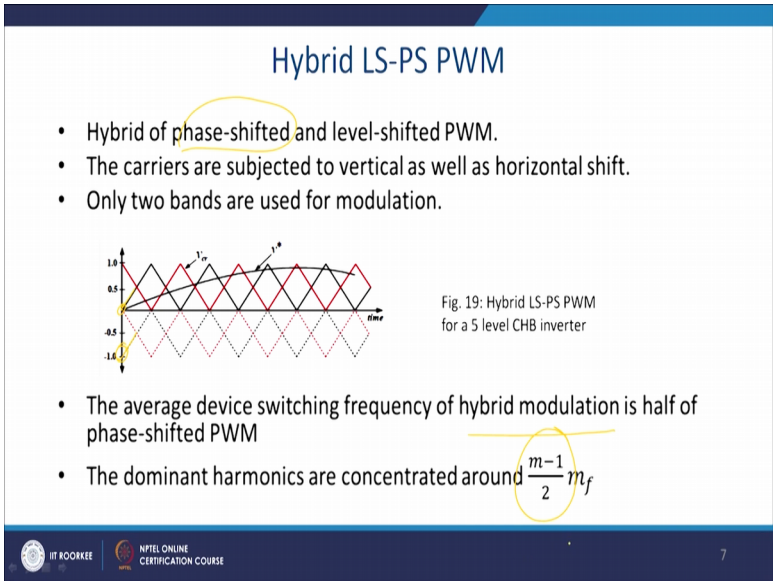

Where you will find that basically there is a there will be a minor image form here, actually there is a phase opposition disposition. So, this and these are in a same phase, but they are phase shifted, but they are sorry they are in a same phase, but the shifted by the magnitude.

So, hybrid phase shifted and the level shifted PWM I mean when you combine the phase shift and the level shift you get the hybrid 1, carriers are subjected to vertical as well as

the horizontal shift.

So, see that this black line bolded and this black line dotted are the vertically shifted. And of course, you can see that if they are they are also can be shifted there can then it is a phase opposition only 2 bands are from the modulation.

So, you automatically this actually the form so, this so, what happened in this case the average device of the device switching frequency of the modulating hybrid modulation is half of the phase shifted PWM. And the dominating harmonic thus you know will be centred around m minus 1 by 2 into m f, where m f is the actually the modulating frequency index.

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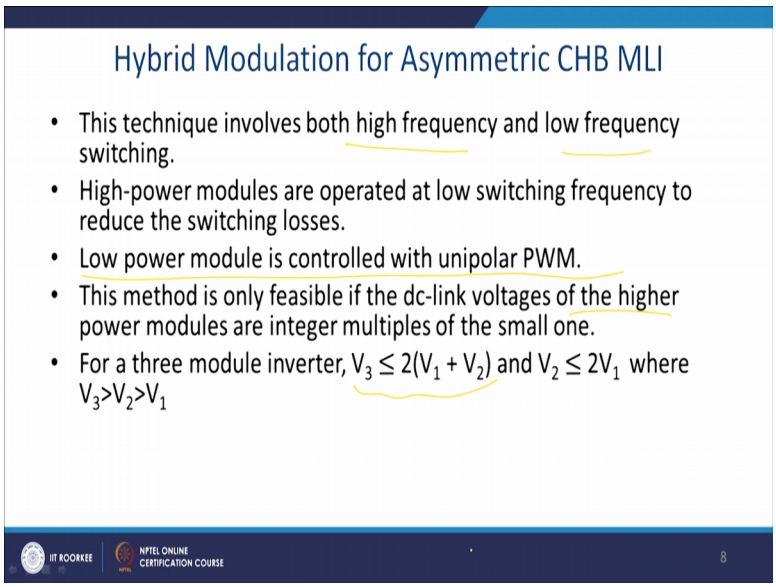

The hybrid modulating frequency index with cascade multilevel inverter will have the following features this technique involves, both high frequency and the low frequency switching, high power modules are operated at a low frequency, to reduce the switching loss we can choose a higher power device with reduced switching loss, where it is switching frequency will be less because you know that most of the cases are IGBT IGDBT I mean current real.

So, if the rating of the IGBT is more then it is switching frequency is been reduced. Where low power module is controlled by the unipolar PWM. So, this is a very simplest way to implement it, what you have studied in the 2 level inverter this method is only visible if DC link voltage of the of the higher power modules all the integer multiple of the small one.

So, we have to. So, if you put 40, another you required to put 80 and so on something like that and this kind of application is highly visible in case of the solar inverter. Solar inverter you can actually have a parallel, you can have a separate strings and string size of the module can be changed by this equations and thus these are actually a perfect fit for with this control strategy.

Moreover, this 3 module inverter having this is the reason you know V 3 should be less than to V 1 V 2 and again V 2 should be less than equal to 2 V 1 in that way actually we required to make this consider this constraint to be satisfied. So, V 3 should be greater than V 2 it should be greater than V 1.

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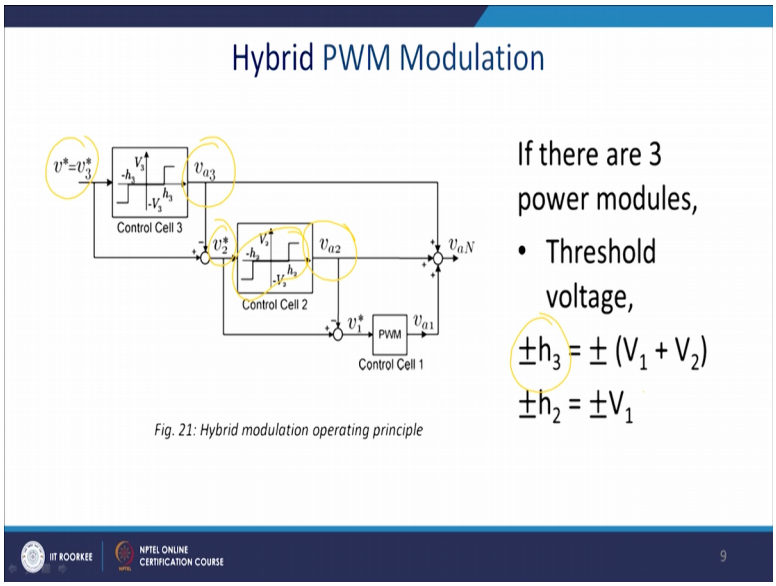

Fig. 21: Hybrid modulation operating principle

So, how you will do that as I told you know instead of square wave you will have a actually steps kind of waveform. So, you will have a V 3. So, from there you have a

control logic it is something hysteresis loop in X axis. So, you will then thus you will have a v a 3.

And v a 3 actually will be subtracted from V 3 and thus you get a v a 2. And v a 2 again we will have a hysteresis loop in a control cell same way it will generate v a 2 and again you will have this control cell and ultimately you will get this v a 1. And v a n will be summation of all the 3 voltages v a 3, v a 2 and v a 1. If, there are 3 power module so, this is the logic. So, plus minus H 3 should be equal to v a 1 plus v a 2 and H 2 should be equal to plus minus v a 1 something like that.

Now, see that hybrid PWM modulation.

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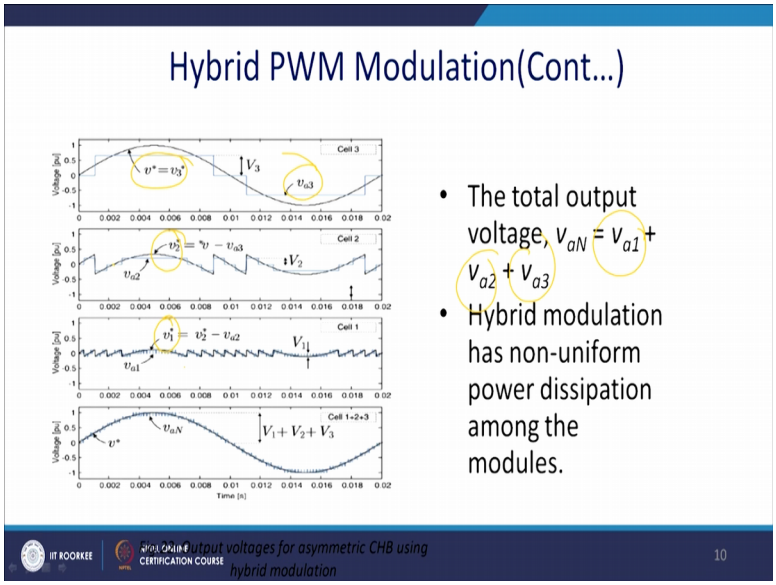

As we have discussed the power output voltage van should be V a 1 V a 2 and V a 3. So, see that you know this one is actually this should be the ultimate modulation wave form and this one is your V a 3. And, you required to generate also V a 2 and this blue one is V a 2 and this one is v a 2. So, this difference of the step kind of waveform is basically V 2 minus V a 3.

Similarly, and you will find that there is a less ripple. Here power handling this device

will hold a maximum power handling and this is the middleman in the road and you can see that there is a ripple. So, it has to handle also the middle of the switching frequency. Same way v a 1 you will find that it is when and thus it has to track this actually the error voltages and which will be high frequency. For this reason it is a low power device with the high frequency it will be exactly fitting this application. So, thus ultimately you will get actually this kind of waveform in voltage and which can be eliminated with the help of actually low pass filter.

Now, we have discussed different kind of PWM technique, now let us discuss the same PWM same space vector modulation technique, which we have discussed in case of PWM. In case of the 2 level I was just extended to the 3 level. We considered actually plus and minus there or 0 and 1 there and here since actually we have 2 upper leg short then switches or we will say that this state as P.

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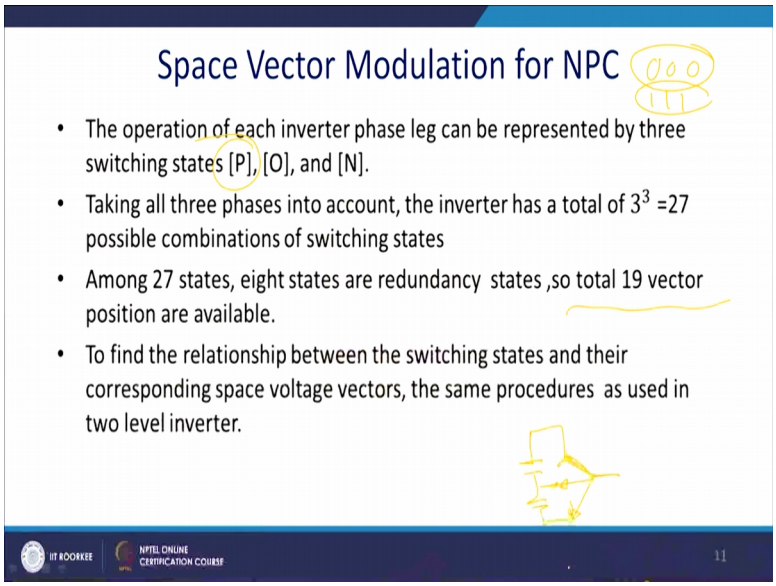

And, when it is actually we have realise please recall this actually this 3 level inverter with a triple throw single pole switch. So, in this switch is connected at this position and this is the midpoint of the capacitor and this is the point when it is connected this position. Then what happen then actually it is connected to the P, when this switch is connected this position we say that it is connected to 0 or opposition. And, similarly

when it is connected to the lower of the dc link voltage we will say that it is connected to the n.

Now, since it has to so, this had a 2 combination since there is a 2 switching combinations for a leg 1 and 0. So, there is a possibility of the 8 state 0 0 0 to 1 1 0 0 to 1 1. Now, in this case you will have actually 27 states. Now among this state we shall see that few will generate the null vector and total 18 state will be there. And so, in that in case of the 2 level inverter for the SPWM you know that actually 0 0 0 and 1 1 1 will give you the null vector.

But, here you will find many combination of it to generate null vectors. So, you have a more redundancy with the switches and then that is gives you more flexibility and the reliability. And, what you required to do we required to find out the relation between the switching state and their corresponding space vectors, the same procedure we have used for the 2 level inverter.

So, let us whatever we have discussed in the 2 level same thing is applicable here based on their magnitude of the voltage vector can be divided into the 4 groups. One is 0 vector or null vector. So, these are basically when you 0 voltage is applied. So, this is actually all the upper switches is closed or all the middle switches are closed that is 0 0 0 and all the lower switches are closed.

Similarly, there will be small vector these are V 1 to V 6 having magnitude since you know that when you we have talked about the DC bus, we have talked about this is actually total voltage total voltage is 2 by 3 V dc. So, in this case is small vector or half vector will call it then this value will be actually V dc by 3. And each have a small vector with 2 switching state 1 containing plus P.

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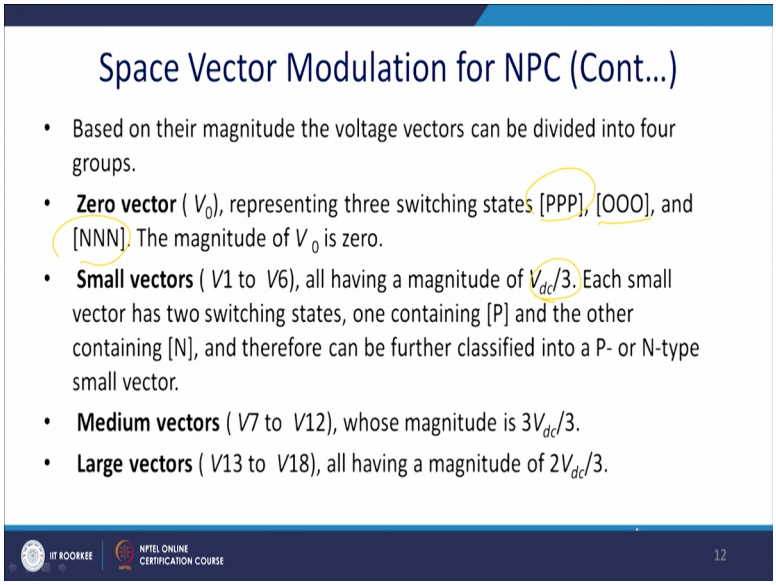

And another containing minus e and therefore, ssscan be further furnish into P or N type small vectors.

Now, similarly we have a medium vector these are called half angle vector sometimes. And, we denote them for 1 2 from 7 to 12 and whose magnitude will be actually V dc by 3 and it will be 30 degree. And there will be large vectors and which was the present in case of the two-level inverter also and this will be present and that value will be V dc by 3. If you only use this large vector then actually then this 3 level inverter falls down to the two-level inverter.

So, let us see that we have calculated the time in case of the 3 level 2 level inverter can it be extended here.

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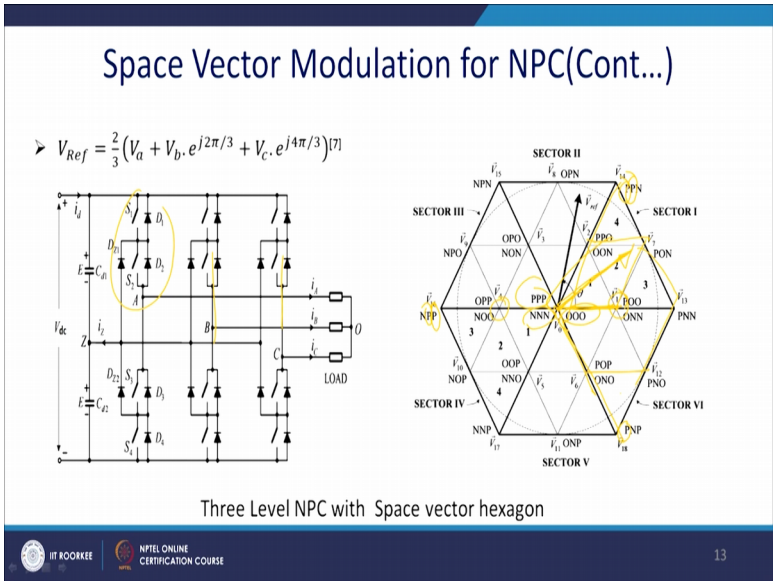

So, this is the diode clamped 3 level inverter and this is the reference. So, see that PPP that is positive positive positive then what is P, when S 1 and S 2 is closed for a leg. So, NNN, that is all the lower leg are closed and 0 0 0. In 3 combinations you will find that you are not applying any voltage to the line. So, it is null vector. So, this is set to be the V 1, you can generate V 1 with plus 0 0, that mean plus this and this or you can also use 0 N N, if you use plus 0 0 we say that it is a P class of half vector and if you generate by ONN we say that N class of half vector.

Same way there will be a mirror image it is OPP you can have or you have N 0 0, V 1 and V 4. So, see that this vectors this half vectors can be generated there is a 6 half vectors and we have a 4 combinations. So, you have a more amount of the flexibility. And you know considering that the phase V a V c and a and till this 180 degree. Actually you can see here from this point the phase a get positive till this time actually it lies positive. So, this is the basically the phase difference for positive phase or phase A. So, minus 60 degree to plus 60 degree.

Similarly, you can see that for phase B this P starts here and ends here and here actually for phase C phase C starts here as well as ends here. So, we can we can actually find it out where is the actually the, we can find it out the voltage V and theta let us say you are

here and I have shown it is here. So, what happened here? You can think of that this voltage is made of V 1 V 7 and also V 13. And, what we required to do you know actually since we can we can think of that this voltage this it is required to you and later shift is origin here and ultimately when you shift is origin here. So, and you take this X X A X 7 and you will find that this one this can be treated as a 2 level inverter. And same calculations what you have done for the 3 level inverter is valid same way for this leg also.

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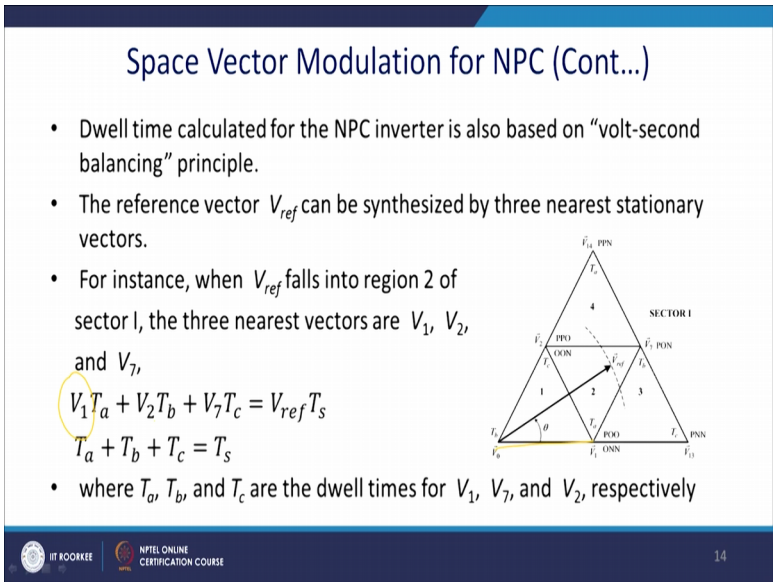

So, thus let us take out that portion of the triangle and find it out what should be the value of a T 1 T 2 or in this case actually T a T b T s. So, dual time calculations for the neutral point clamp converter is based on the volt second balance what we have done in case same thing we have done in case of the two-level inverter.

The reference vector V ref can be synthesised by the nearest 3 stationary vectors, in this case we can see that it is with V 1 it is applied for this time T a with V 2, it has been applied for the time T b and V c, that is equal to T s and in between we have a null vector that that will be there. So, we required to calculate same way the T a T b T c and thus we required to know that for which time duration what will be applied. And you see that in between how it will work? So, when you apply when you apply PPP.

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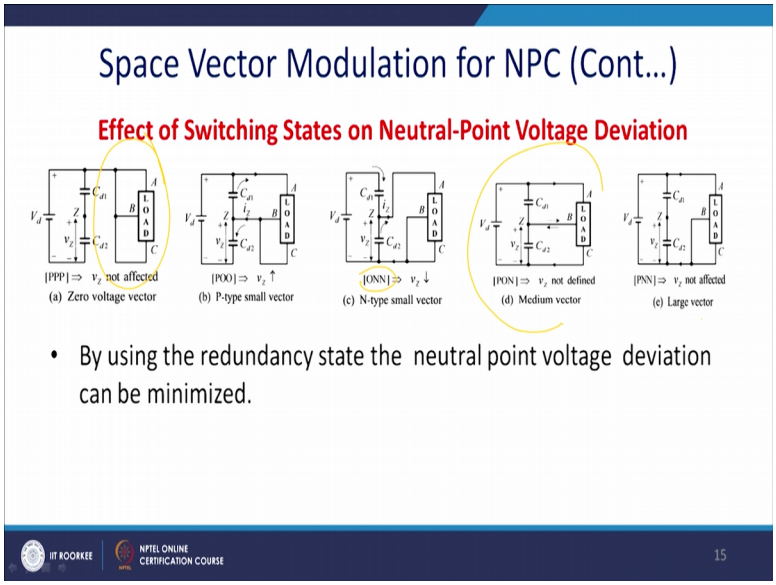

So, you your load configuration is this. Similarly, when you apply P 0 0 your load configuration is this f s is connected to the positive of the DC bus voltage and it is connected to 0. Then you can also connect and that will also give you 0 that is 0NN so, you get this voltage.

Similarly, it is PON, then you get this kind of configuration and PNN you get this kind of configuration. Now you require to I give it to the assignment what you have done in case of the 3 level 2 level inverter to find out T a T V dc. I am not deriving here and you are expected to derive and the solve it for T a V T c for the calculations ok. Thank you, we shall continue in the next class and this is our last lectures for the PWM technique, for next class onward we shall start with the actually the facts devices practical fact devices and it is control and it is applications.

Thank you.