**Flexible AC Transmission Systems (FACTS) Devices**

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**Lecture - 07**
**Multi Level Inverter - I**

Welcome to our video lecture series of Flexible AC Transmission Systems Device. Today is our 7 lecture we shall discuss a detail about the Multi-Level Converter or Inverter. It is used for actually we shall use the abbreviations of multilevel inverter as MLI.

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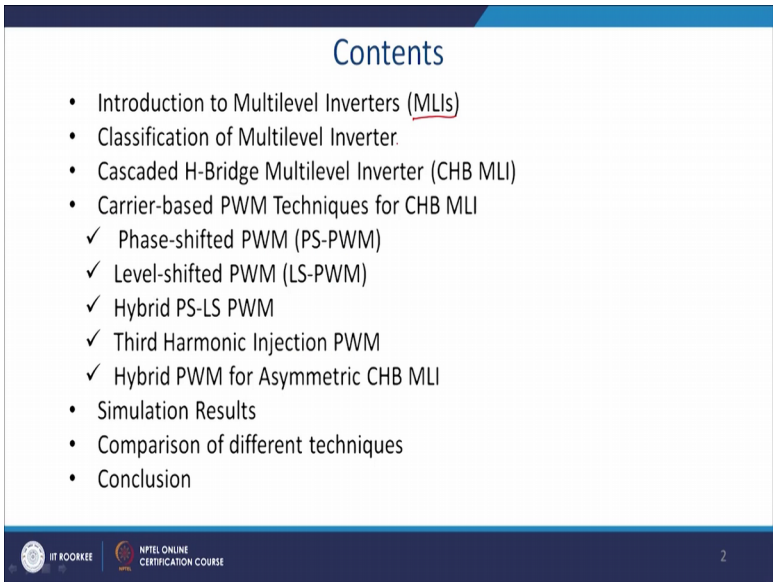


And, you know classification of the multilevel inverter can be actually cascade, then first we will discuss about the classification of the multilevel inverter, then cascade H-bridge multilevel inverter will be discuss in details one for the multilevel inverter.

And, thereafter different kind of PWM technique required to operate this multilevel convertor or invertor properly, that is career based PWM for H-Bridge cascade multilevel inverter. There are phase shifted PWM we have a level shifted PWM, we can have hybrid PWM and third harmonic injections and hybrid PWM of asymmetric the condition and we will show some simulation results, and we will compare with the

different type of PWM technique in our content.

So, why multilevel inverter? Multilevel inverter is actually a composed of the series of the our array of the power electronic semiconductor with a capacitive voltage sources.

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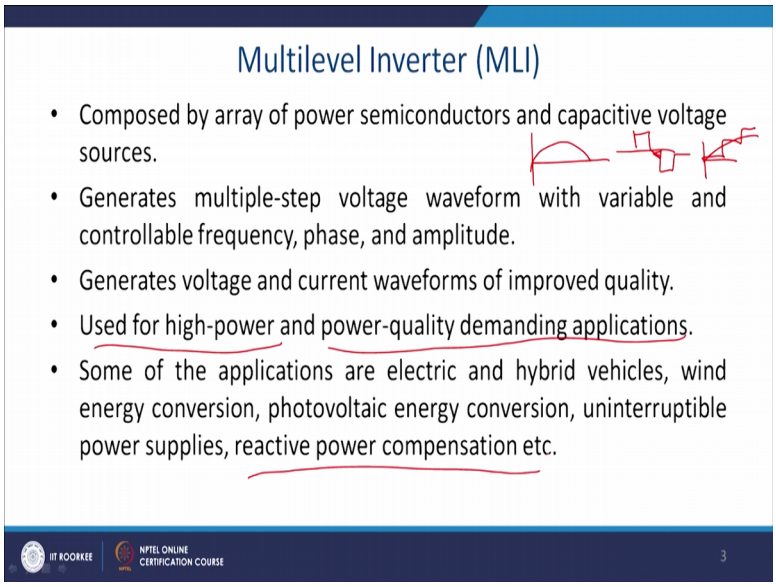


It generates voltage in multiple step, because the we generally generate required to generate sine wave, but in case of the PWM we generally actually give plus minus V dc. So, there is a huge instantaneous voltage error between the actual voltages required by this inverter and so, actually the PWM generate voltage.

And, here in case of the multilevel inverters in it is applies voltage in steps. So, more will be the steps more actually to be closer to the sinusoidal. So, thus voltage waveform with variable and the controllable frequency phase and amplitude, and again moreover it generates voltage and current waveform with the improved quality, because the instantaneous voltage that required to be inject by the inverter. And actual voltage injected by error voltage injected by the inductor was inverter is less in error because you can apply voltage in steps.

Since, power electronic costs of the power electronic devices go high with the rating. So,

we required to increase the power handling capability of the device by connect them in series for this reason, it is used for the high power and the high quality power management applications. And it is one of the basic need for our facts devices. And some applications are of course, all the application is facts devices STATCOM SVC we will see later these are basically, now uses multilevel inverter apart from that you can have hybrid electric vehicle wind energy conversion system, photovoltaic energy conversion system, UPS and reactive power compensations STATCOM, SVC's etcetera.

Now, what are the features or what are the desirable features of the multilevel invertor or the essential drawback is that you require more number of switches. So, what should be the advantage of having a multilevel inverter the higher voltage operating capability since the devices are connected in series?

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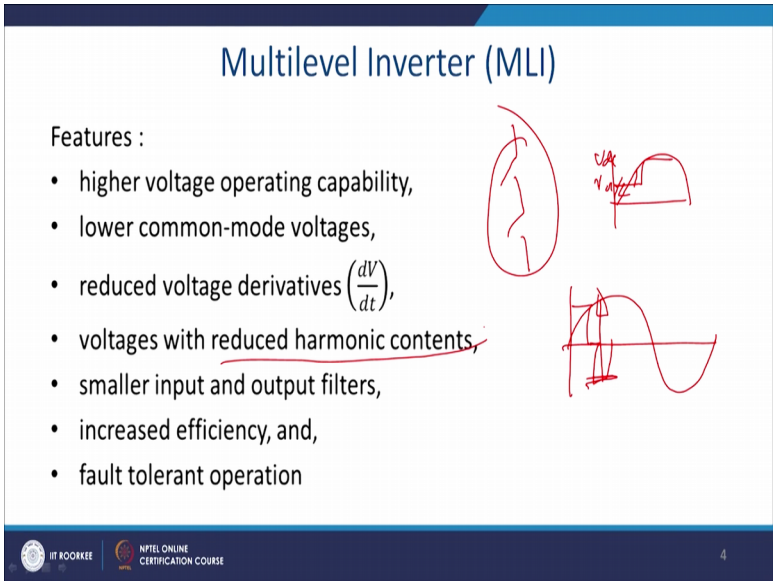


So, voltage blocking capabilities gets doubled. Most of this facts devices are connected and distribution system or 6.6 Kb for this reason, we have to mandatorily use this devices. Thereafter lower common mode voltage and reduce the voltage derivative timidity.

Since, you know it can works on a voltage on a steps. So, you can see that instead of the

it can apply V dc it can apply V dc by 2. So, like this. So, we can find out the rate of change of V dc with time is actually less compared to the 2 level inverter.

Voltage says with reduced harmonic content as I told because you know let us say we required to generate this is the voltage and if it is a PWM you generate this voltage or this voltage to generate. So, when you are applying this voltage you have huge instantaneous error. And, that is the one of the source of the harmonics, but in this case what happened? Since, you can apply something like this instantaneous error is half? So, if you go to the for the 3 level inverter if you go to the many more level. So, this instantaneous error get diminishes and what else?

So, since due to that this harmonic content will be reduced. Since, harmonic content will be reduced and thus you require smaller filter smaller size filter to eliminate. And, it increases the efficiency we can find it out because there is a if it is a hard switching. So, hard switching losses of the 2 level inverter quite high compared to those multilevel inverter even the number of switches are more. And, we can actually put redundancy in the circuit and thus we can introduce the fault tolerance capability with this multilevel inverter. Now, this is the example.

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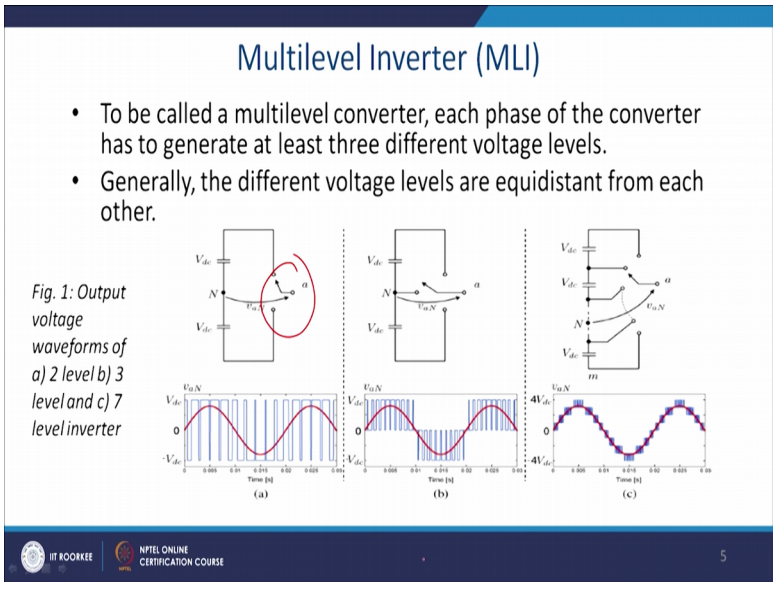

We try to realize the multilevel inverter with simply a mechanical switch. In this case it is a single pole double throw switch, in this case it is single pole triple throw switch, in this case it is single pole multiple throw switch. So, this is the realizations of the two-level inverter.

So, when it is connect like this then it is connected to the upper dc bus voltage. So, you will get a voltage V dc and once you connect a lower dc bus voltage. So, you get minus V dc. So, voltage will swipe from plus V dc to minus V dc thus you can see here; the how huge instantaneous voltage error?

And this is actually a 3 level inverter and this is the multilevel inverter, where actually voltage is switching over 0 to plus V dc, it can be connected V dc, it can be connected to 0 and that is N point of the midpoint of the DC link capacitor voltage and it can be it can converted to lower end of the switches. Thus you can directly you can see that stress here is halved and instantaneous voltage error also will halve. You can have the multilevel inverter and you can see that actually this error is minimized are greatly. Now, we shall come written the application aspect of this multilevel inverter multilevel inverter can be broadly classified into single source.

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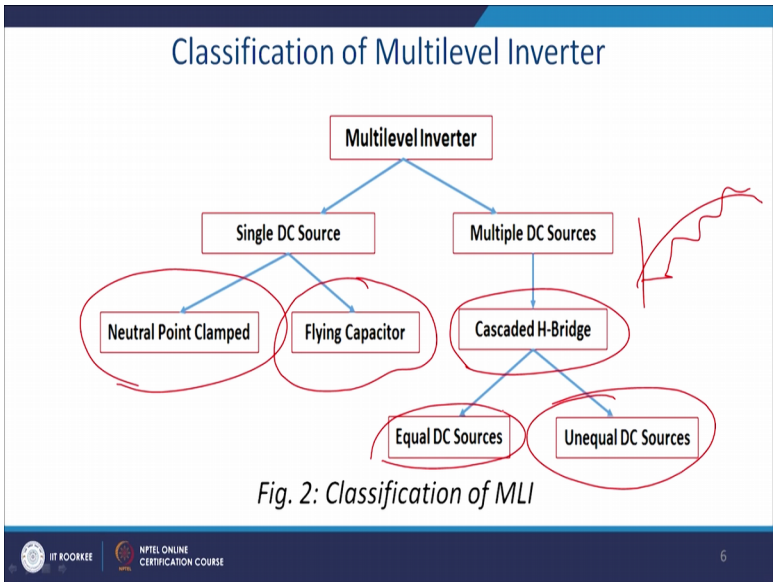

Fig. 2: Classification of MLI

Generally, you will find that this is the most used topology, that is neutral point clamped that is or diode clamped topology. And you will also have a capacitor and it is a simplest topology and it is find much more application.

And, next topology is the flying capacitor here actually voltage applied through the different charging and discharging of the capacitor, but to operate it properly you required to charge and discharge the capacitor in a controlled manner to get the desired voltage, thus there is a complex constraint is involved. And you can have a cascade multilevel inverter. So, you have a modular kind of setup you can increase the number of module by simply using the number of the modular switches, but disadvantage is that you know in case of the cascade multilevel inverter you required to have a separate DC source.

Nowadays, this application finds this kind of topology find lot of application is solar inverter, because you have a solar panel that is can be treated at a isolated DC sources. And so, thus you can generate a different kind of voltages. So, you can you can have an equal DC source voltage or you may actually try to generate this. So, that you can actually replica obvious your sine wave. So, that can be used for the unequal DC source.

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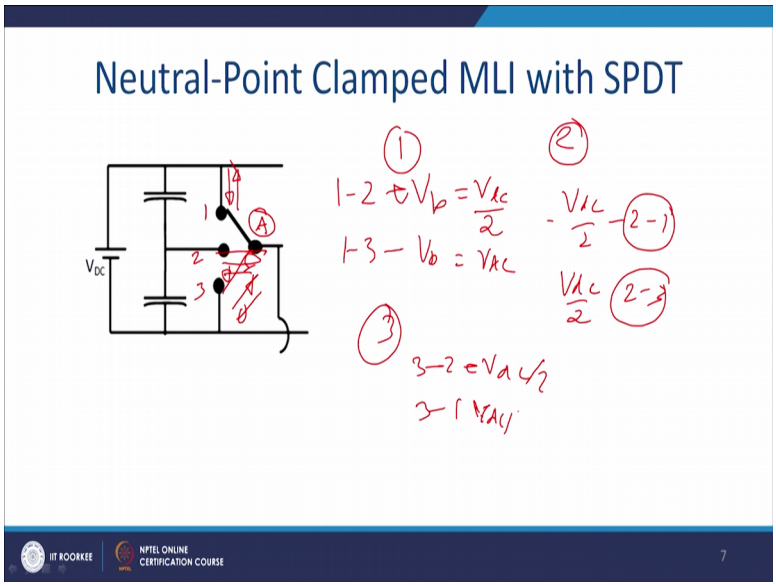

Now, let us understand the application of the simple neutral clamp or the diode clamp inverter. Now, let us understand so, 1 2 and 3 these are the points. Now, it is connected to the 0.1 let us say of the pole A, then current can be bidirectional let us see that what kind of switch is required here? Current can be bidirectional so, you require to have a switch that require actually the bidirectional blocking bidirectional current conducting capability. And also within the 0.1 and 2 you require to 1 and 2 the blocking voltage V b required to be V dc. Or here in this case it is V dc by 2, same way with the blocking voltage between 1 and 3 required to be V A C.

So, this is all other cases. So, how you realize it? And when you put this is the position 1, same way what about position 2? When you placed the switch here again actually it should have a bidirectional current capability between the 0.2 and A. So, we require a switch that is by that can actually allow to current to flow in bidirection, again it can block the voltage of V dc by 2, in between the 0.2 to 1.

So, there is one minus sign involved and this is it required to block the voltage of minus V dc. And same way V dc by 2 you will find in between actually 2 to 3, this is the condition. Same way where it is put into the position 3, same way current required to be bidirectional and the it required to block the voltage between 3 and 2 that is V dc by 2 and 3 to 1, that is V dc by that is V dc.

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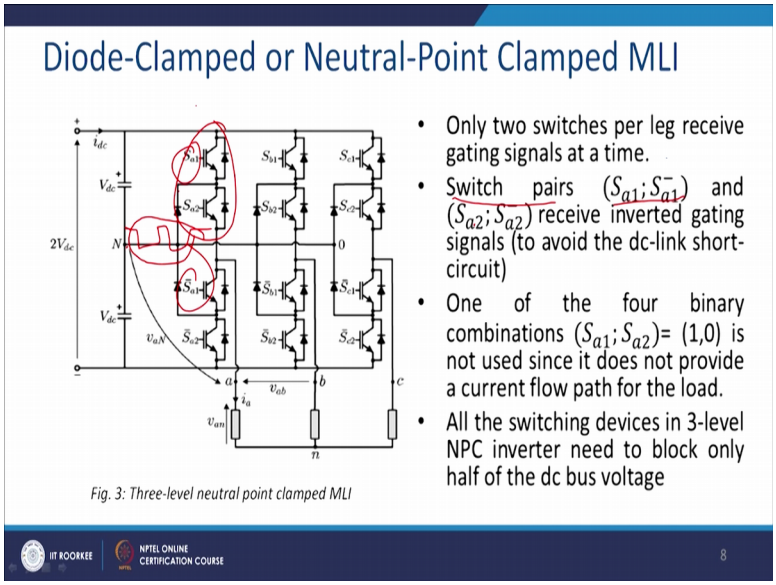


So, how you will realize it with a switches; Now, this is the switch before that we can take a whiteboard to explain it.

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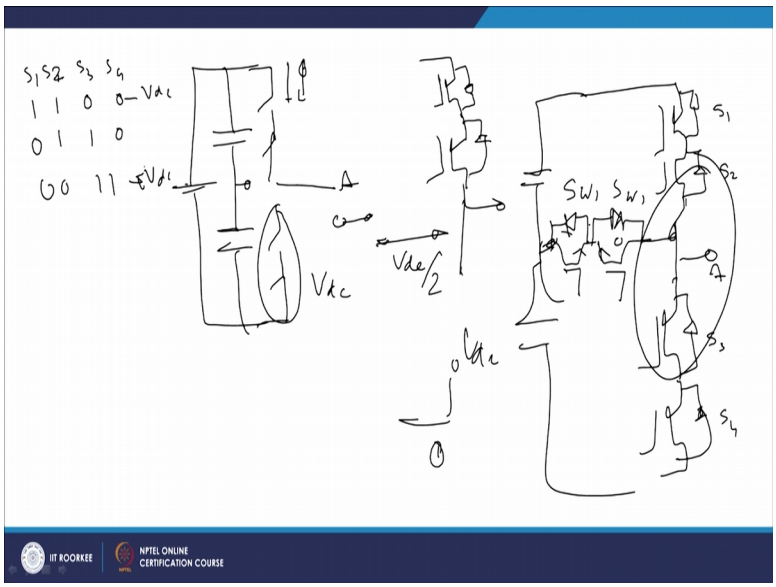


So, what it does you know it require. So, this is the point let us say A and this is your the DC bus voltage and you have a diode clamped circuit. Now, you realize that when it is

connected with it required to block the voltage. So, when you want to connect this voltage required to block the voltage of V dc. So, we can and it current required to be bidirectional.

So, what we can think of you know we can connect the switch here with antiparallel diode, that another switch with antiparallel diode and this point. Then have to it has to block the voltage of V dc and this point is a midpoint of the capacitor, it has to again block the voltage V dc by 2 in this configuration.

Now, in next similarly when you come to the this is actually position 1, same way when you come to the position 2, then what happen this switch get shorted. So, and it has to be bidirectional for this reason we require to have a switch that is in bidirectional in nature. So, we can realize a 4 quadrant operation of the switches. So, here you know. So, you required to have a antiparallel diode. So, and have a bit you have 2 switches. And similarly you have in when it is connected to the position 3 it will be a same position for 1. So, you have these circuits.

But, you see that to realize for one lag you require the 6 switches. So, can we have some kind of redundancy here this and can we not minimize it. So, here you can see that let us name it S 1 S 2 S 3 S 4 and name it S W 1 and S W 2. And, what happen here? When we want that this pole a to be connected to the upper end of the DC bus voltage. Then of course, what are then actually we write that actually S 1 S 2 and S 3 S 4 if you write. So, S 1 S 2 should be 1 S 1 S 2 should be 1 and S 3 S 4 should be 0. So, you will connect it into the lower switch in that positive DC bus voltage.

Same way if you wish to connect, there is a redundancy where you can connect because you know you have a capacitor midpoint. So, this point will be connected here. You can find that if you connect a diode simply through this point and it can walk. Anyway and so, if you so, if this switch is on and ultimately, this switch can walk. So, similarly if you have if you wish 1 1 0, that is when you connect them then these two is on.

Then what happen? We can have some kind of redundancy here this generated voltage can generate 0 in this configure. In this case you get V dc and when it is 0 0 1 1 you get

V dc minus V dc. And, how you get 0? There is a many combination now see that you I can switch over to the practical circuit and here you know, we have put 2 switches here. Instead of that we can connect a diode and you can use the switch S 2. And thus what will happen you know these 2 switch and similarly in a lower half this diode will conduct. So, instead of this switches we can replace it by a diode. So, this is the optimal circuit you will get and ultimately this is the diode clamp realizations and where when you give pulses accordingly switching will takes place.

So, what is the switching configuration? Only 2 switch of the upper lag receive the signals to generate plus V dc, on the 2 switch for the lower lag you will get a single for generating minus V dc. So, for this reason switch pairs S a 1 and S a 2 receive receives the positive signals and S a 2 and S a 2 receives the getting signal and to avoid DC link of a short circuit condition.

Similarly, here this paired of switch will receive the inverted signals and this paired of switch will get a positive signal. One or the 4 binary combination is sufficient to represent those switches. So, we can we I have shown in the black previously, that the combination of the switches S 1 and S 2 S 3 S 4 will be combined in a such a way and we will find some kind of redundancy of here. When S 1 S 2 is on that is connected to the positive DC bus voltage then what essential you get here you get a voltage V dc.

Similarly, when this S 1 bar and S 2 bar is closed you get minus DC bus voltage and when S 2 and S 1 bar is closed you essentially get 0. So, thus you can actually one aspect you can see, let us write it again and see that what happen?

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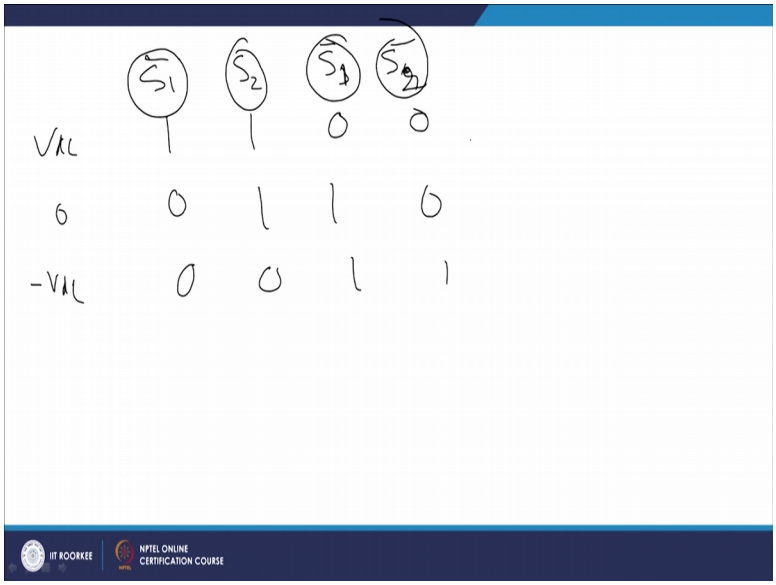


So, the switches are S 1 S 2 S 3 S 4 now and we have already proved the switches you have seen it is S a 1 bar and S a 2 bar.

When you required to generate V dc, that 2 2 upper switch will be closed let us make it upper switch closed by 1 and other will be 0 when you want 0. So, it will be the condition, when you want minus V dc you will have this. So, from there you can see this the truth table that S 1 and S 3 are complementary to each other and S 2 and S 4 are complementary to each other.

So, far this reason S 1 can be written as S 1 bar S 4 can be written as S 2 bar. So, thus this nomenclature is used there. So, see that it is S 1 bar S 1 and S 1 bar. So, to avoid shot we required to ensure that switch pair S a and S 1 receive a positive signals and S a S 1 and S and S 2 and S 2 bar receives basically the inverted signal, because it is a complimentary logic and that will ensure a never shorting condition of the dc link voltage.

One of the 4 binary combinations that is let us make S 1 and S 2 is not used, since it does not provide the current path to the load. All the switches of the 3 level inverter need to be block only half of the DC bus voltage and since you know that when you can choose a

single switch operating of V dc, but instead of that because here you can choose a half of the rating.

Generally cost of the switches increases pretty high with the rating and thus it helps to reduce the switch rating. And, another aspect the uniformity all the switches having a same blocking capability of V dc by 2, that give some kind of redundancy in our design.

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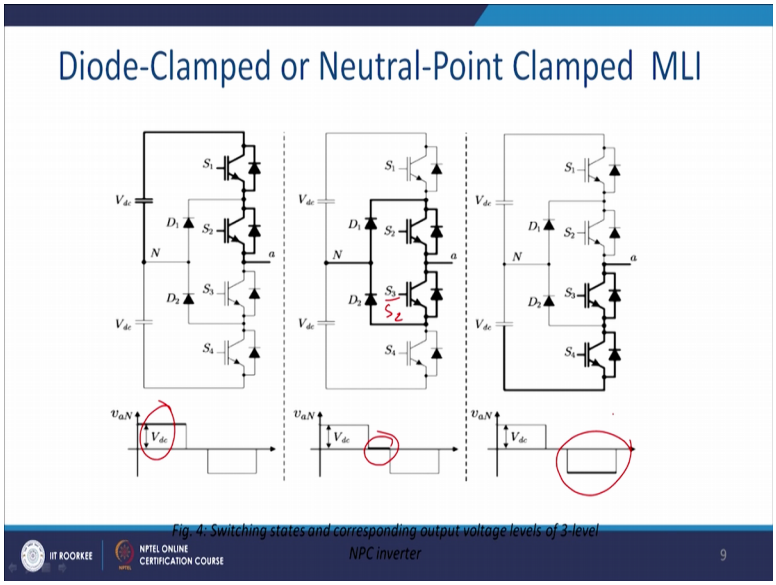

Fig. 4: Switching states and corresponding output voltage levels of 3-level NPC inverter

Now, this is the board of conduction, when upper 2 switch on it has been bolded so, S 1 and S 2. So, you get a positive DC bus voltage in between the point N and A. So, you get this voltage.

Similarly when these 2 S 2 and S 3 are on later we can write an S 2 as S 2 bar. So, what will happen here, you can find actually the 0 voltage here.

Similarly, when lower switch is on S 3 and S 4 you get minus V dc across van this is the simple operation and you can extrapolate to the any level and one of the advantage of it this is the simplicity of the operation. Now one of the advantage of that clamped or the neutral point clamp MLI.

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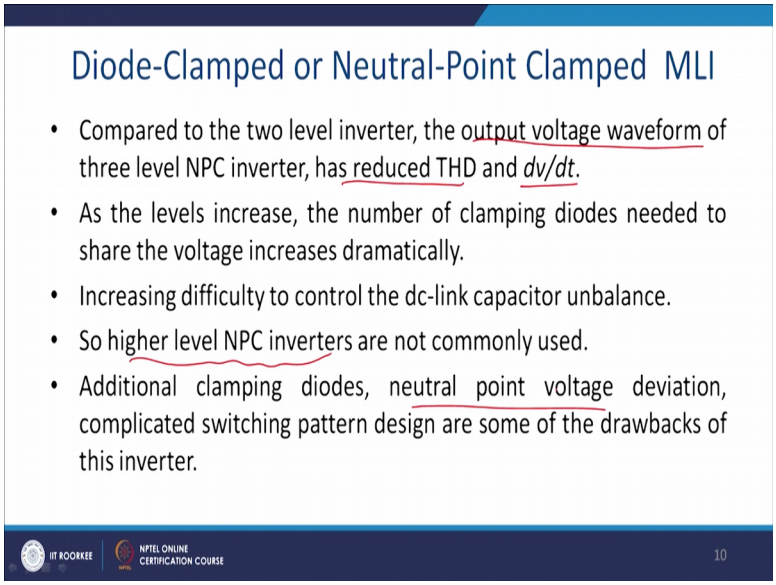


Compared to the two-level invertor the output voltage waveform of the three-level invertor has reduced THD; it is because instantaneous error of the applied voltage and the generated voltage by the inverter is less. And, also less timidity same case because state of change of voltage or multilevel inverter are in steps not plus minus V dc.

As the level increases number of the clamping diode needs to be needs to be shared the voltage increase dramatically. Increasing difficulty the control the DC link voltage unbalance. So, let us understand what happened there? So, we have shown the case here.

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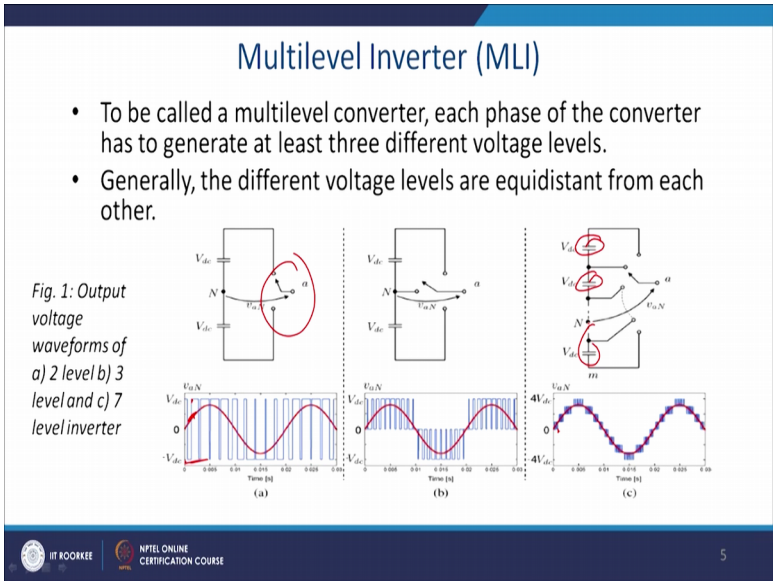


So, this is basically the multilevel inverter. Since, this capacitor voltage is not actively controlled. So, current coming and discharging current coming into the system and going out will basically give the status of the amount of the charge and that will be reflected to the voltage available at the DC link.

So, in this case is all of a sudden there is a mismatch of the current pattern then one of the DC link voltage may discharge faster and thus it will generate unequal voltage distribution this is one of the disadvantage of the diode clamp inverter. And this problem this for this reason we required to solve this problem and for this reason, we required to actively charge and discharge the capacitor that we usually do in case of the capacitor clamp multilevel inverter.

So, for this reason we find that very high level NPC are not recommended and it is restricted only to the 3 level 4 level inverter. And more over additional clamping diode in an neutral point neutral point voltage deviations is complicated design pattern it gives for the analysis and this is also one of the disadvantage of the diode clamp multilevel inverter.

Now, we shall start to play the capacitor clamp multilevel inverter it will continue to the

next class and basically, we can also realize capacitor clamp three-level multilevel inverter with the help of the SPDT or SPST mechanical switches. So, you know this is the point A and this required to be controlled.

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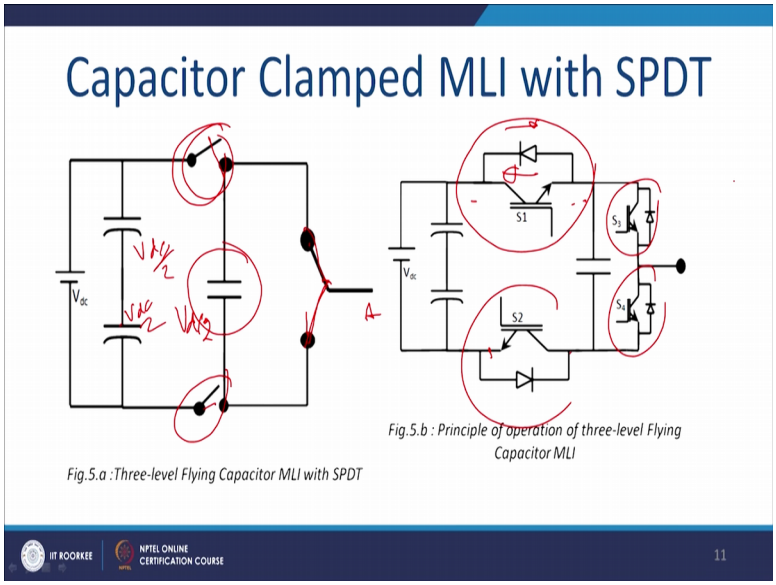


And you know, if you wish and ultimately if this switch is closed then it will be connected to a DC bus voltage.

Again, similarly if this switch is closed and if this position is here it will be connected to the negative of the DC bus voltage. And, here you can change the polarity, while you are in this position, and if you open this switch and close this switch then you apply minus V dc from and should be subtract minus V dc by 2 will be you assume that is voltage is V dc by 2, and this voltage is V dc by 2 and this voltage is also V dc by 2.

Here, you will actively monitor the voltage of it while it will be applied here. If you close here, it will be essentially minus V dc by 2 and if you put this position then it is minus V dc by 2. If you close this switch and if you keep this position, then essentially you get minus V dc by 2, same way if you close this switch and if you put it here you get plus V dc by 2.

So, in that way you can generate a multiple state of the voltages and here this disadvantage is not there, because you are controlling the voltage actively, but one of the disadvantage or diode clamp voltage is that complexity of the complex circuit that I am calculated.

So, how you realise with the switches? Essentially this can be realized by these switches, because current required to be bidirectional this configuration of the IJBT gives you the bidirectional current and unidirectional voltage blocking capability between these 2 points.

Similarly, it is gives a bidirectional current and unidirectional voltage blocking capability. And, you can close any of the switch, here and here accordingly you generate the voltage V dc and minus V dc by 2 and this is the simplest way of realizations of 3 level diode clamp diode clamp multilevel inverter. Now, in this is the actual circuits of the diode clamp realizations.

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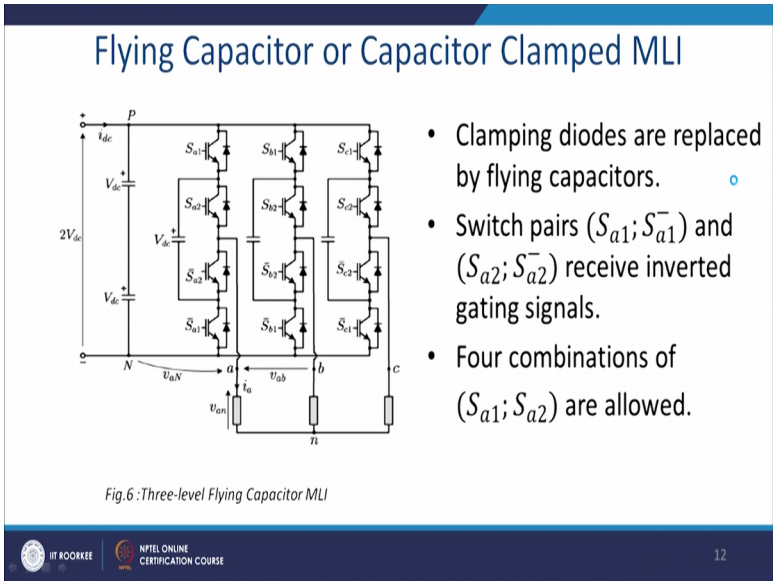


And, we shall continue with these circuits in our next class and we shall discuss it what is the advantage and disadvantage of this flying capacitor multilevel inverter. Why it is called flying that also will be explained now.

Thank you.