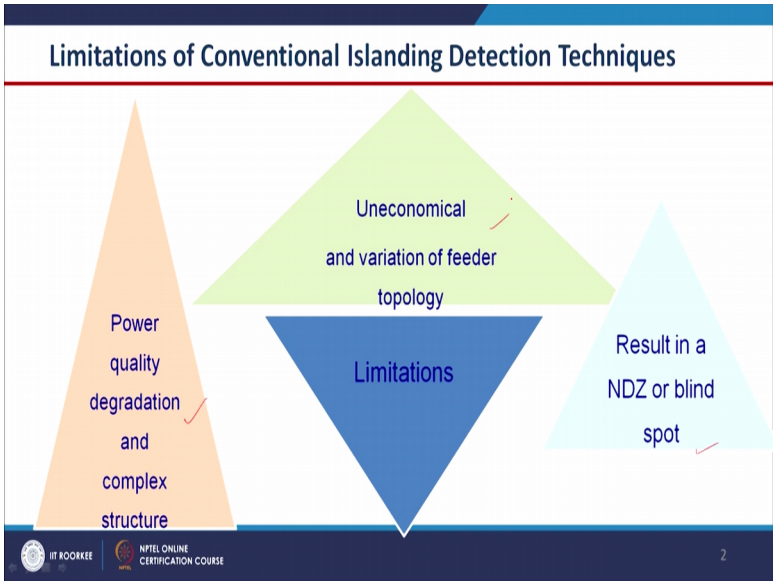
Introduction to Smart Grid
Dr. Premalata Jena
Department of Electrical Engineering
Indian Institute of Technology, Roorkee

Lecture – 17
Islanding Detection Techniques – II

Good morning to all of you, in this lecture we will discuss about one of the passive Islanding detection techniques that is the rate of change of superimposed negative sequence based impedance method. Now, before that I will discuss what are the limitations of previously discussed islanding detection base technique, passive islanding detection base technique?

The first one is the power quality degradation.

(Refer Slide Time: 00:50)

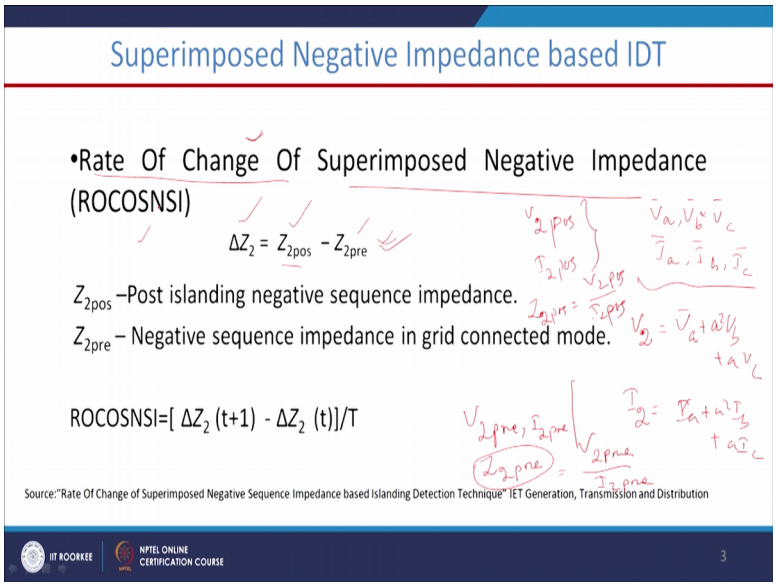


And also complex in nature, the power quality is one of the major issues in case of active islanding detection base technique and also in sometimes in if you could see that , the rate of change of frequency that we have discussed in the last class this NDZ the Non Detection Zone is one of the major problems.

Now, and also we have sometimes on economical and due to the variation of the feeder topology or line length or expire show some of the techniques are also affected. So, due to different limitations in this particular running like, in our research laboratory we have

discussed or we have development one technique. And that is basically the rate of change of superimposed negative sequence base technique and that particular technique here we will discuss in this class.

(Refer Slide Time: 01:51)



Here what we do the superimposed negative sequence impedance is going to be calculated first, the first step is we have to collect the voltage 3 phase voltages V a, V b and V c and also we have to collect 3 phase currents I, I b, I c at the terminal of the DGs or at the terminal of the DERs. Now, after getting this phases; you know we are calculating the phases as the terminal of the DERs using list error square base technique.

Because the list error square base technique can extract the fundamental if the signal is having decaying DC component. And also if the signal is having some how many components then also we can calculate the fundamental component.

After relating this we will just calculate the negative sequence component of the voltage V 2 that is basically V a plus a square V b plus a V c and next we will calculate also I 2 that is the negative sequence component of the current, that is I a plus a square I b plus a I c. Here I just want to mention one point that mostly our distribution network is unbalanced in nature. Due to the presence of a single phase loads unbalancing occurs and due to that the negative sequence voltage, negative sequence current both are present even before the disturbance or before the islanding mode of operation.

By exploiting this V 2 pre information and I 2 pre information, we are interested to calculate this Z 2 pre that is known as this negative sequence impedance of the micro grid system and the terminal of the DGs. When the system is not disconnected or there is no disturbance present in the micro grid system or smart grid system; that is known as Z 2 pre and this Z 2 pre is calculated using this V 2 pre divided by this I 2 pre.

Now, suppose some islanding, islanding is there. So, during this islanding mode of operation again we will also because it is a continuous process. You know this islanding relays mounted as the terminal of the DERs, where continuously we calculate or we measure the voltage and current and the corresponding phases degree sequence components of the volts and current are going to be calculated continuously.

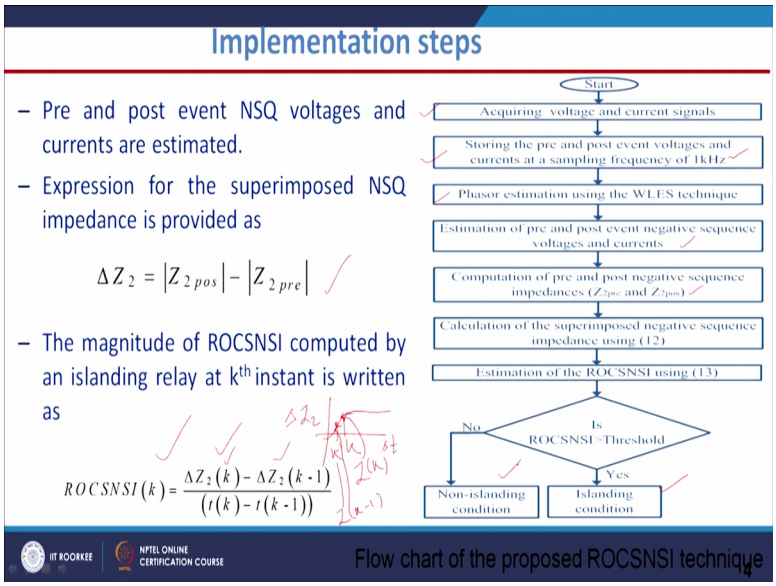
Continuously this Z 2 is going to be calculated at the terminal of the (Refer Time: 04:45) resources. Now, when this says islanding is there again and so this V 2 island or pos I have mentioned here, post after the disturbance V 2 pos and I 2 pos are also calculated. Using this two quantities so we will calculate the parameter.

So, Z 2 pos is equal to V 2 pos divided by I 2 pos, now after relating this, this is the after the disturbance and this is before the disturbance. The difference between these two impedances is known as the superimposed negative sequence impedance, this one we have to understand, what is this superimposed term? What is the superimposed says?

The superimposed term of the definition of the superimposed quantity is that the difference between the post quantity and the previous quantity, pre quantity or the superimposed parameter means the difference between the post parameter and minus the pre parameter. Here this is the superimposed parameter or the impedance, if it is superimposed voltage.

So, it will be del v is equal to v post minus v pre, if it is superimposed current del I is equal to I post minus I pre, in this case we have taken superimposed negative sequence best impedance. And again we have taken the rate of change of this is important, rate of change of superimposed negative sequence impedance and in short form ROCOSNSI.

(Refer Slide Time: 06:32)



Now, if you just see that how to take this rate of change of superimposed component in time domain k th instant, that k th instant what is the value? This del 2 this delta Z 2 k minus delta Z 2 K k minus 1 divided by t k minus t k minus 1. If this is the series of this particular I mean the values of this z value; this is the delta Z 2 if it is delta Z 2.

Now, we will take the rate of change means the consecutive samples, the consecutive values this delta Z 2 this is at kth instant to this at kth instant in this is for k minus 1, you can make it k here this is k minus 1. So, this z k represents this point and this z k minus 1 represents this point the previous sample, the previous value. .

Difference between these two values that is Z k minus delta Z 2 k minus delta Z 2 k minus 1, divided by the time the corresponding time this is the t axis our delta t I mean, the difference between 2 consecutive values of this delta Z 2, but the time gap. If we are taking this as 1 milli second, if the sampling frequency is basically how much, it is 1 kilohertz the corresponding that is going to be 1 milli second, if it is something else that is going to be where it. So, based on this recursive manner we will just calculate the rate of change of the negative sequence based superimposed impedance.

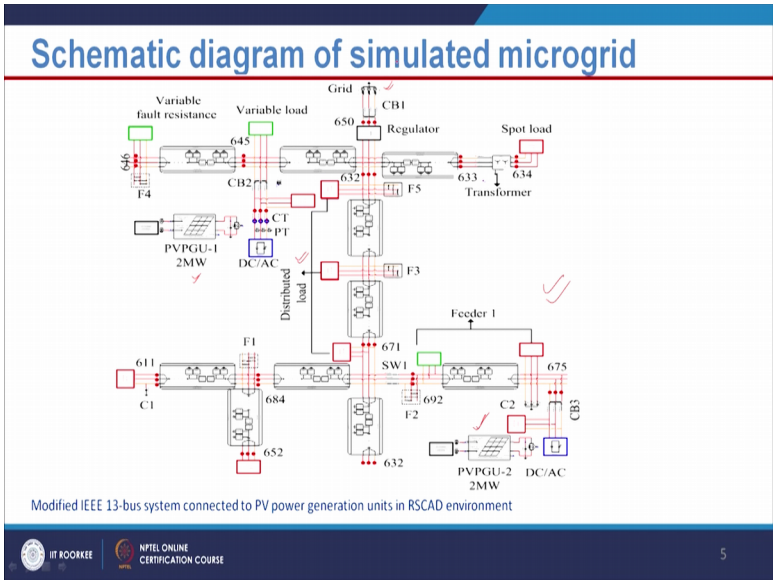
In other steps so according this volt is current signal at the DG terminal and storing the pre and post event voltage currents data which has sampled at the rate of one kilohertz. And next we will estimate the phasor using the WLES means list wait and list error

square base technique and then we will calculate the pre and post even negative sequence, voltage and same current and final this Z 2 pre, Z 2 post.

And we will calculate this is equation in our pre for our to mention this 12, 13. So, here it is basically the delta Z 2 and finally, the rate of change of the impedance and if this is greater than certain phase showed then islanding is there and if it is not if it is below certain iteration then there is no islanding.

Yes of course, this particular technique is also dependent on the threshold values and but however, this technique works find so 0 power mismatch condition.

(Refer Slide Time: 09:11)

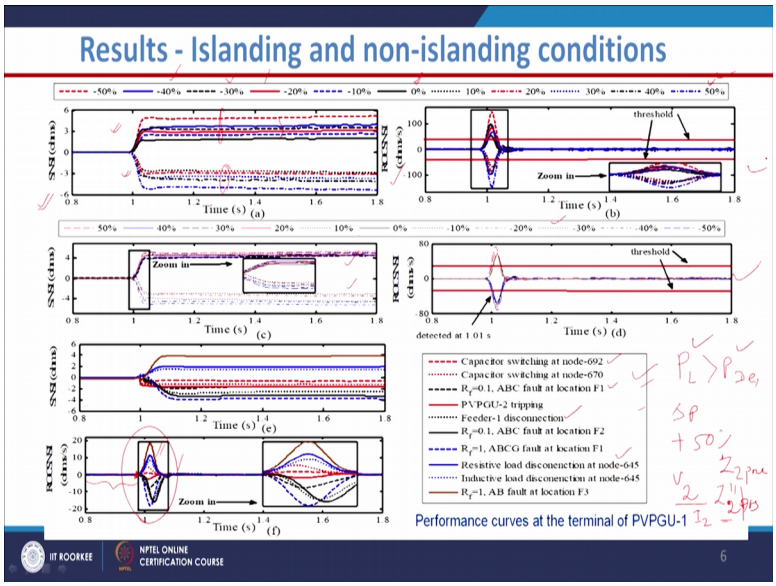


To realize this particular technique we have taken one sample system like this we have let us say 13 bus i e triple 13 bus system there we have this PV generation this is our PV system.

And here we have another PV system and different types of loads are also connected, here loads. So, based on this micro grid system and here is our main grid and the system is simulated using the RSCAD software which is present in real time digital simulator, that is RTDS. Inside the RTDS we have one software it is called as RSCAD. Just like a PSCAD, RSCAD and usually this RSCAD software we have simulated this ith triple e 13 plus system to realize the technique.

Now, if we see the first figure.

(Refer Slide Time: 10:01)



Here it is written S N ird is the superimposed negative sequence impedance right. So, SNSI SNSI stands for make Superimposed Negative Sequence Impedance. And he could see that for different positive result power mismatch like one is 50 percent, 40 percent, minus 30 percent and we went up to plus 50 percent. The variation is also I mean we did for 80 percent because of course, if we exceeds I mean if we be close to the higher percentage of power mismatch the factor is very good.

But it is a difficult situation for low power mismatch condition. So, in every algorithm it is desirable to test the performance of the technique for lower percentage of the power mismatch. Mostly for 0 power mismatch condition and also we can see here for 0 power mismatch condition also we have this 0 percentage power mismatch where the technique is working properly. Now, see for minus 50 percent this is the, first one is for 30 power mismatch minus 50 percent minus 40 percent the corresponding graph is in the basically on the positive direction.

And for the plus, that is plus 10 percent, 20 percent, 30 percent the particular SMSI lie this particular values, this is values lie on the negative direction. So, this is in the positive direction altogether and these are in the negative direction. Why? What is the reason behind it? It is a good analysis point that during this positive power mismatch condition already we have discussed that this P load, this is the P load is greater than P Dc. That means, load is more and generation is less and I am talking about for the islanded micro

grid operation, at this condition the micro grid is islanded and we are we are we have calculated the superimposed negative sequence impedance and then you have shown here.

For different percentage of power mismatch; now, this if it is this delta P is let us say plus 50 percent; that means, my P L is greater than this , PD g in that case what happens the V 2 basically this V 2 is decreased, the V 2 value because the voltage decreases the load increases, voltage decreases right. So, if the voltage decreases this I 2 that means, my Z 2, Z 2 value.

Also decreases and what happens to Z 2 pre? this is my Z 2 post and this is my Z 2 pre, but before this is islanding the Z 2 pediments constant unless until you are going to change the system because the system is not going to be change the anymore, the system is as it is. But during this islanded mode of operation due to the different disconnection of the DGs or disconnection of breakers the V 2 and I 2 are going to affected or impedance of the circuit is going to be affected.

So, this Z 2 post is different for different power mismatch situations, now if it is lower than this my Z 2 pre the difference of this superimposed negative sequence is going to what, it will be negative. And that is why this plus 50 percent altogether the SNSI are the negative direction; that means, as if this Z 2 post is less than my Z 2 pre.

And similarly if we will come for the minus that is the negative power mismatch situation, in that case my impedance Z 2 we are expecting assuming this Z 2 post is greater than my Z 2 pre and that is why the all are in the positive direction. So, keeping in this particular concept and we have taken this negative sequence part of this active pre (Refer Time: 14:12) part and this is also positive part of the reactive part and the corresponding figure this one here.

Now, coming to the rate of change of part, why this is 0? Let us say this islanding has occurred at the 1 second and up to 1 second from 0 to 1 second; this SNSI rate of change of SNSI 0 because before disturbance this Z 2 post is equal to Z 2 pre. The distance between 2 consecutive impedance values basically it is constant, that is why the before the disturbance or before the islanding this Z 2 post is equal to Z 2 p and the difference is going to be 0.

And that is why this rate of change of this SNSI up to the inception of this islanding event 0. And when this island has occurred or islanding event has occurred then there is remarkable change in this SNSI rate of change of the negative sequence superimposed impedance.

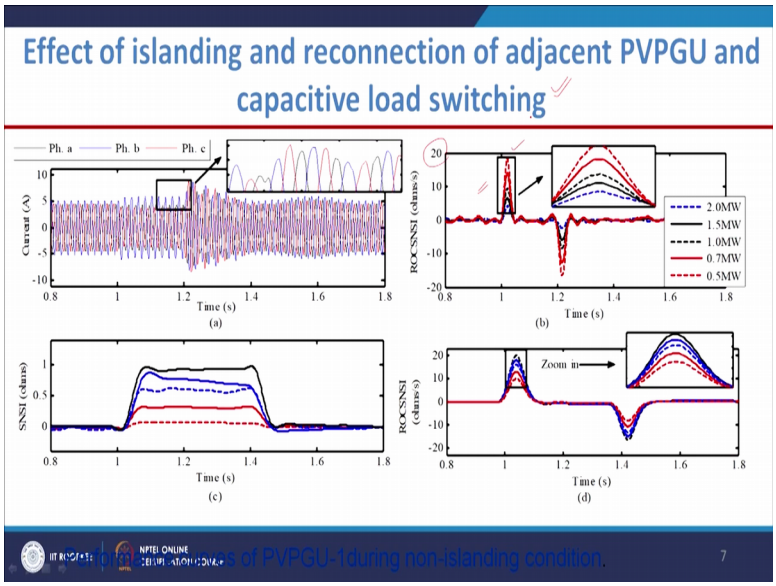
Now, taking this particular change, like exploiting this particular change we will decide whether we are, we have to give trip command or not. Whether the islanding relay is going to give some trip command or not right. And of course, we have to see whether this rate of change of negative sequence impedance has crossed the limit or threshold value that is also important.

And in this case we have maintained 20 as a threshold value for our purpose like for 1 kilohertz sampling frequency. If the value of this rate of change of superimposed negative sequence crosses 20 then we will declare it is a these are islanding event. Otherwise it is non islanding event, also we have tested this particular technique for different types of non islanding events like you could see here the capacitor switching and also different types of faults like AG fault, BG fault and feeder disconnection here and yes disconnection, connection of the loads right inductive load, system loads.

So, these are all non islanding events, the islanding event is the disconnection of the micro grid from the main grid. And disconnection or connection of the DERs within the micro grid system with the condition that the main grid is connected those condition is known as non islanding conditions. Capacitive switching faults, so those are also non islanding events and also we have tested for this non islanding events; what will be the performance of the proposed technique.

You could see here that this figure shows this rate of change of SNSI, then you get super imposed negative sequence impedance here. The values you could see that it crosses, it is here, this is the threshold; threshold value this is threshold value and the corresponding characteristic here you can see ROCSNSI; these are the corresponding figures.

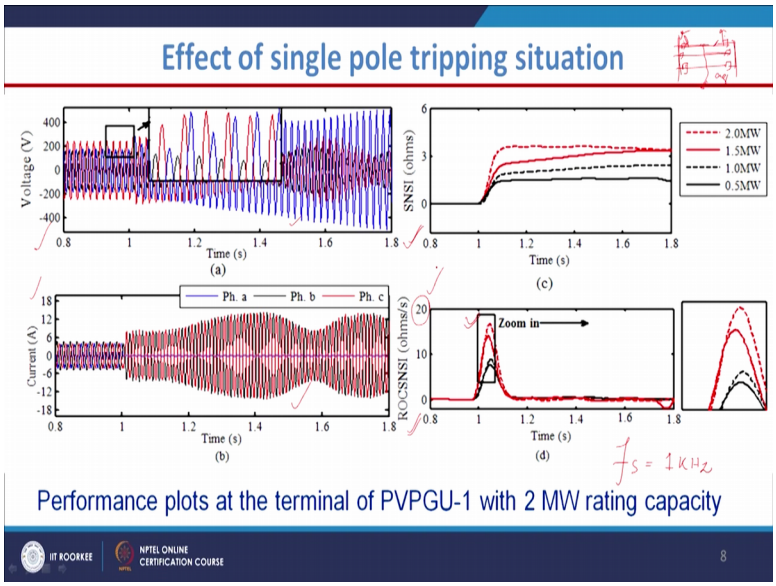
(Refer Slide Time: 17:25)



Now, we will go for one effect of islanding and reconnection of adjacent PVPGU and capacitive load switching case, this is one of the non islanding event. And here you see that for this case, this is the rate of change of superimposed negative sequence current. Here you could see the value is within 20, within 20; as already I have mentioned that in case of this islanding condition the threshold we kept 20, if the value is crossing 20; then it will be declared as the islanding event otherwise it is not. So, we have tested for different type capacity switching mode; here you could see that this value is below 20, that means it is not and islanding situation. .

Also we have tested the performance of the propose technique for single pole tripping situation, what is single pole tripping situation?

(Refer Slide Time: 18:21)



Suppose this is one bus, this is another bus and within this bus 3 lines are present and the corresponding poles like up the circuit breaker are present. And due to certain fall let us say in phase a if any fault ag fault occurs, the breaker of one particular I mean the breakers both the sides are opened; that means, this.

If it is open then this is also opened that particular phase is out of service, we can keep it like this, it is open. So, this condition is known as single pole tripping situation, keeping are the 2 phases healthy other phases like b phase and c phase they carrying the power whereas, the phase a is faulty: so, it is taken out of service. So, this condition is known as single pole tripping situation and this situation leads to unbalancing, because one phase is out of service and it is quite good chance of generation of what the negative sequence components and of course, the fault is there, fault is isolated.

So, this negative sequence component also may lead, mislead that it will we just say it will say that it is an islanding situation. So to test that because our technique is based on the negative sequence component; so we have to also test the performance of the technique for the single pole tripping situation right;so in one of the feeder we need the test.

And you could see here this is the voltage and current for that particular event single pole tripping situation. You could see here we have fault in phase a that is where the phase a current is almost 0 here and this black one and this red one corresponding phase b and

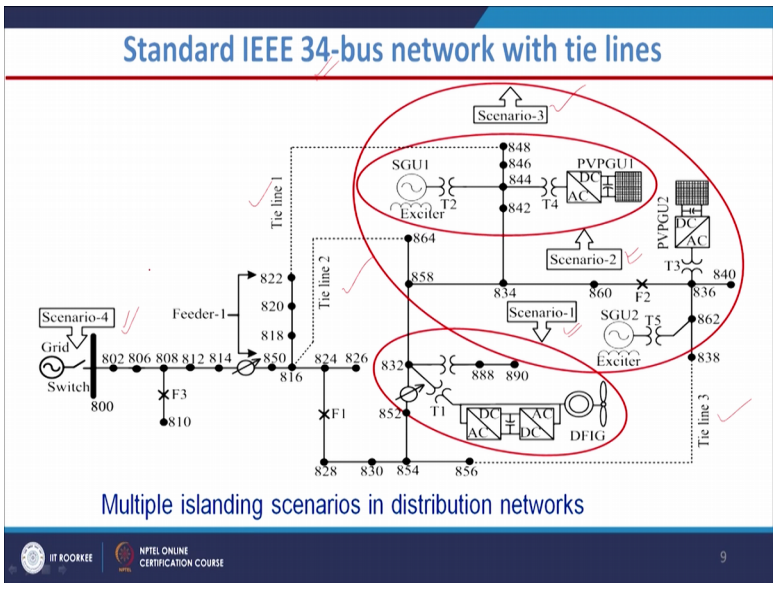
phase c current. And you know during single pole tripping there is slow oscillation which is experienced in current way form as well as the voltage waveform.

Due to the power mismatch, that is due to the basically the mechanical power and the electrical power and this is the corresponding SNSI, the superimposed negative sequence impedance and this is the rate of change of SNSI. See, the value of this ROC SNSI is well within 20 because this 20 is our threshold, for 1 kilohertz sampling period.

See I will also discussed in further sections that the sampling frequency also decides the threshold, the sampling frequency is different and; obviously, my delta t is also going to be different. So, then my threshold is going to be changed and this is the also one of the demerit of this particular technique, the sampling frequency varies, then the corresponding threshold is also going to be changed and this is for sampling frequency fs is equal to 1 kilohertz for this case.

When the sampling frequency is to 1 kilohertz and for this single pole tripping situation this is declared as a non islanding situation, it is not declared as a islanding situation. Now, we have also tested this performance of the proposed technique for different tie line connections, for that purpose we have taken this IEEE 34 bus system.

(Refer Slide Time: 21:43)

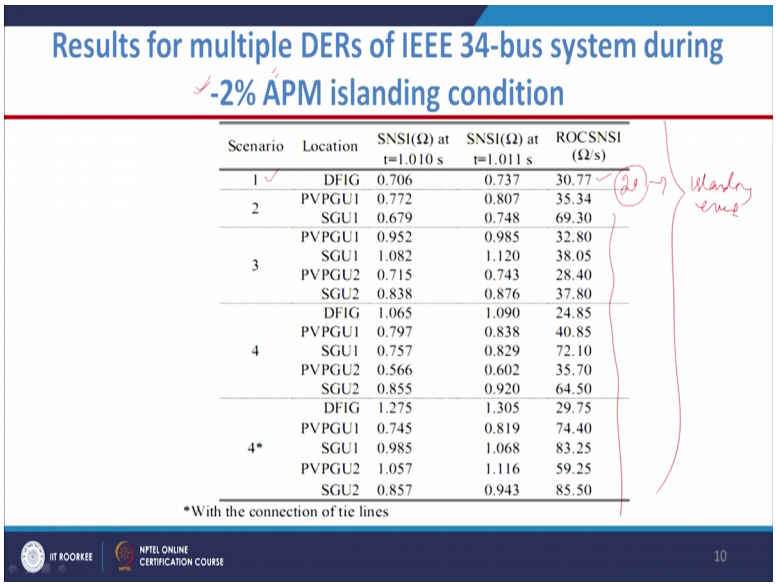


And here you can see that different types of tie line like, tie line 1, this is our tie line 2, this is line 1, this is tie line 3. By connecting and disconnecting this tie lines, we have

treated a 4 scenarios like scenario 1, this is scenario 1 and this is our scenario 2, this is scenario 3 to this 2, this is 3 and also here we have scenario 4.

So, based on different combination of the tie line connections or disconnections, we have decided different types of scenarios.

(Refer Slide Time: 22:26)

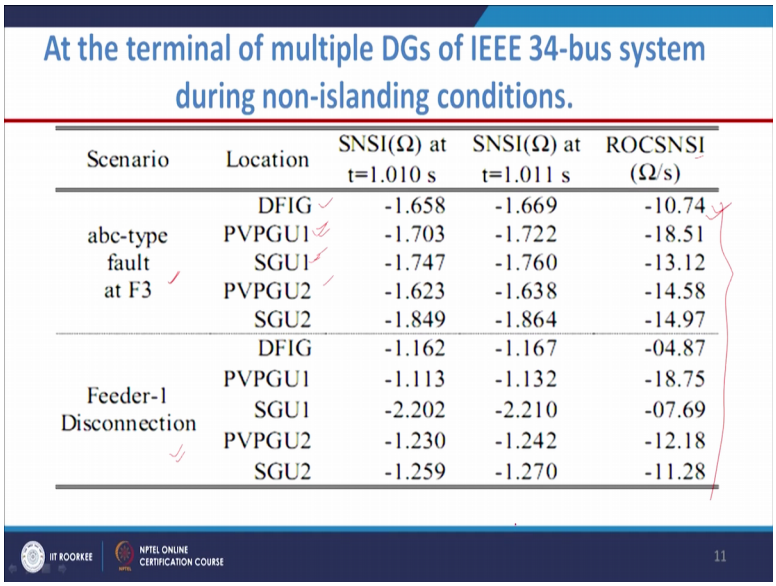


Based on this scenarios here we have tabulated the corresponding values of SNSI and ROCSNSI, if we will take the scenario 1 this is one. So, the corresponding SNSI values 0.737 and this ROCSNSI is 30.77. That means, if it is crossing 20 and it is declared as an islanding, islanding event and you could see here throughout this table all are basically the values are above 20 and that is why all the scenarios are treated as islanding event with connection of this tie line system.

That means it indicates this tie line connection has no impact on the performance of the propose technique, these are as would as it is declaring that this is an islanding event. And yes we have taken here for minus 2 percent active power mismatch, this A stands for active, power P stands for power M stands for mismatch.

Similarly, also we have tested for non islanding event for this particular i triple e 34 bus system.

(Refer Slide Time: 23:47)

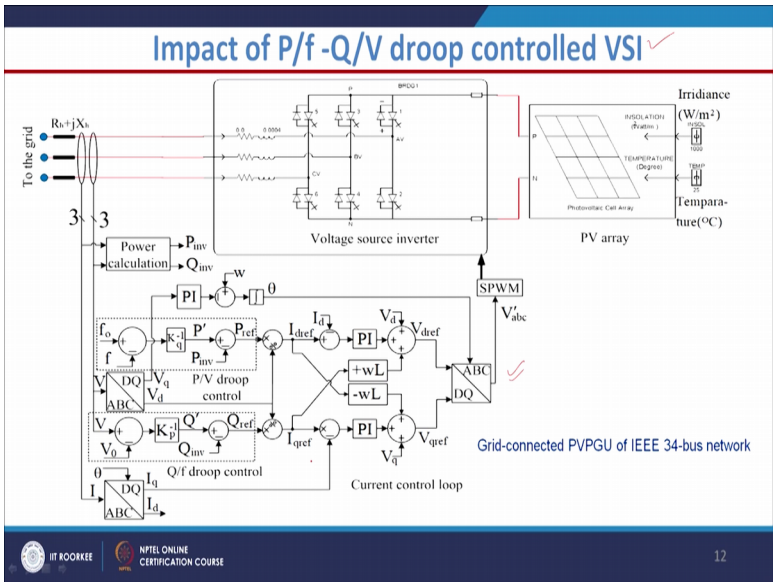


And here we have created abc type fault at F 3 location and feeder 1 disconnection, these two basically taken by considering the location of different DGs like DFIG, PVPGUI this DFIG basically the wind system and this is your PV system and this is synchronous based DG system.

A different type of renewable sources also considered to test the performance of the technique. Now, you could see here finally, I will just come to this column where we have written this rate of change of superimposed negative sequence impedance and you could see very clearly there all the values are below minus 20 or plus 20 right. So, that is why we can say that this particular system is very I mean technique is very robust.

Even for the different type of non islanding conditions the technique logs well. Also we have tested for different type of control strategies which are used for the inverter of the different type of renewable sources. Let us say for our solar system and wind system we use like P by f Q by V droop controlled system for the voltage source inverter this is vsi that a technique used in the inverters.

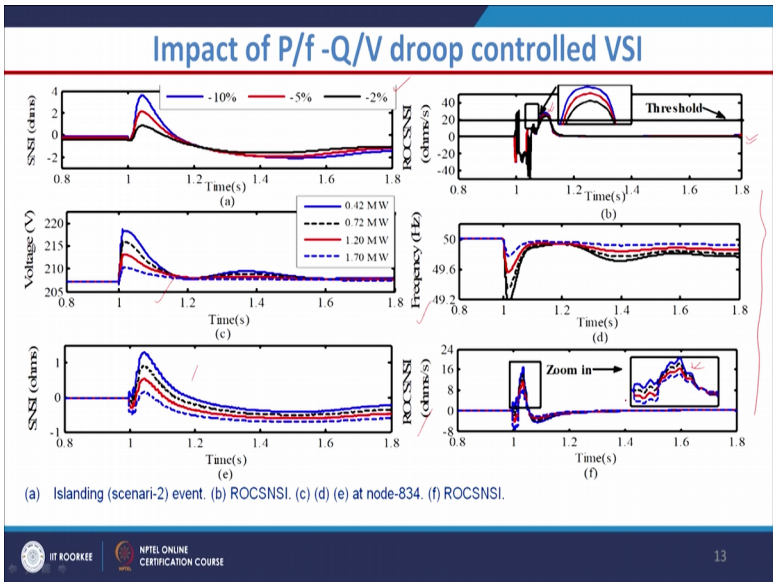
(Refer Slide Time: 24:56)



Now, for different types of converters controllers whether this technique is working fine or not, yes of course, because you know when we are designing certain islanding detection technique; we should test the performance of the technique for different type of controller strategies. Because, it may happened that for certain control strategy this technique will work or it may happen that some other technique it may not work.

So, that is why it is very necessary that we should test the performance of the technique for different types of control strategies. Now, for this case this is the block diagram, suppose solar base technique and this was system we have simulated using this RSCAD software of the RTDS system that is a Real Time Digital Simulator.

(Refer Slide Time: 25:47)

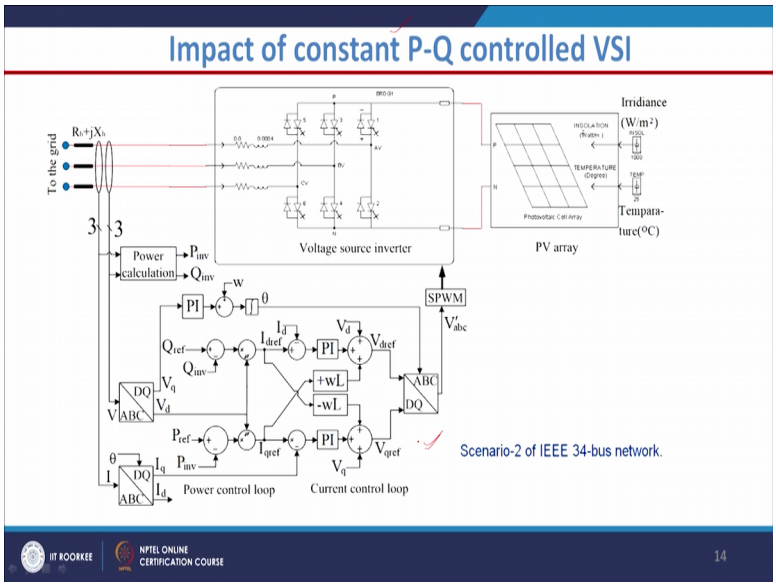


And it is from that the technique bogs well like for 10 minus 10 percent, 5 percent 2 percent this is SNSI and this is the corresponding voltage and this is SNSI and here to some extent you could see that very close to the threshold.

You know it will be very difficult to decide whether this is an islanding system, the islanding condition or not that is also one demerit we got, it is not demerit it is detecting the islanding situation. But it is very close you could see here it is very close to the threshold right. And these are for the frequency based relays and also we have given one comparison with the existing islanding relays, existing this is the frequency rate of change of you see and I both together compare.

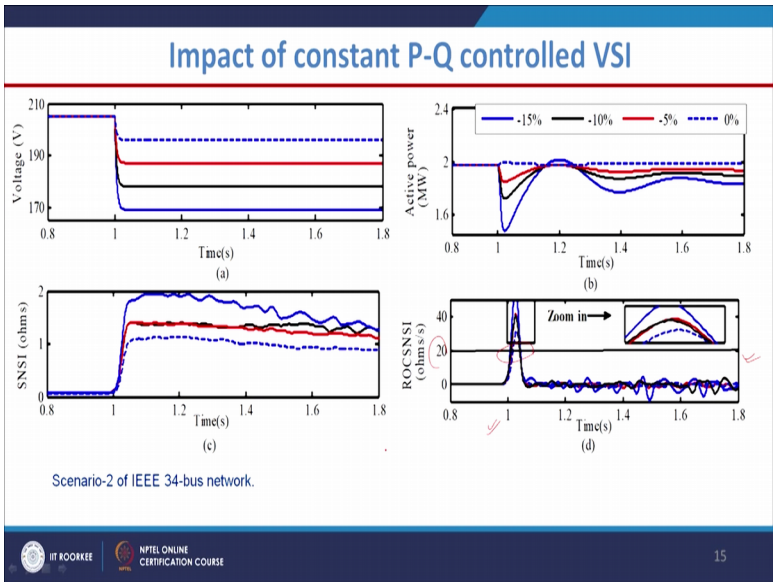
And to some extend this is also oscillatory in nature also, this not very straight forward what we have seen the previous results.

(Refer Slide Time: 26:47)



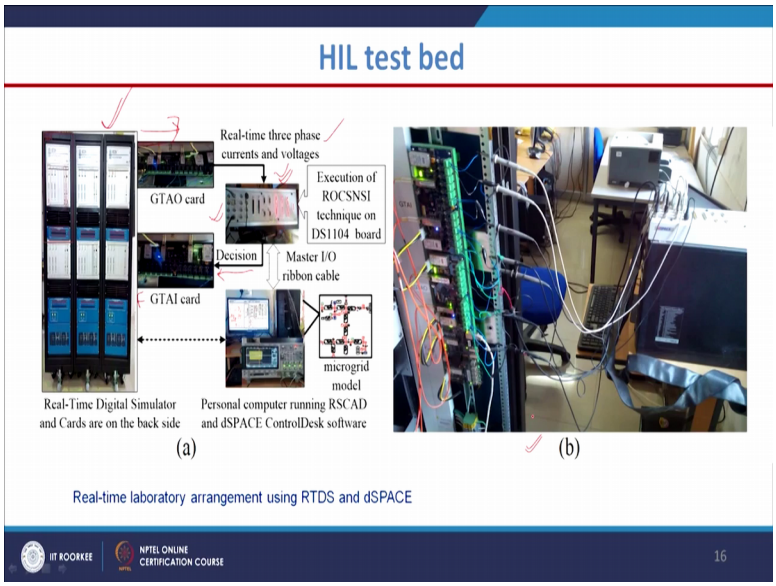
Next way constant P Q type control strategy which is used in ways I of the solar system also we have tested and the total blog diagram are present inside this RSCAD software of the RTDS and here also we have tested and this is the corresponding diagram.

(Refer Slide Time: 26:59)



If you see here the rate of change of final figure, you could see here that this rate of change of super sequence current it exceeds the threshold, this threshold is 20 here and he exceeds the threshold value.

(Refer Slide Time: 27:19)



Finally I will discuss one HIL test bed which is also very important for us to learn what to know, ah.

In our laboratory in the department of electrical engineering we have this HIL test made facility, for this HIL, this HIL stands for Hardware In the Loop system and for this HIL test bed we need the RTDS Real Time Digital Simulator and this base 1 and 1004. Here I have just shown here, this is our RTDS and this is our dSPACE, DS1104 and you could see that the system was already I have discussed whether it is IEEE 13 blog system or IEEE 34 bus system.

Whatever and this two systems are going to be simulated using this RSCAD software of the RTDS. And after this simulation we will just tap, we will take this GTAO card means this analogue output card because RTDS has analogue output and digital output card and also it has digital input and analogue input cards.

So, there are through this analogue output card we will take the analogue signal to the dSPACE and inside the dSPACE our algorithm is running. The impedance superimposed rate of change of superimposed best technique it is basically coded inside this dSPACE, dSPACE works on the in the medium of MATLAB.

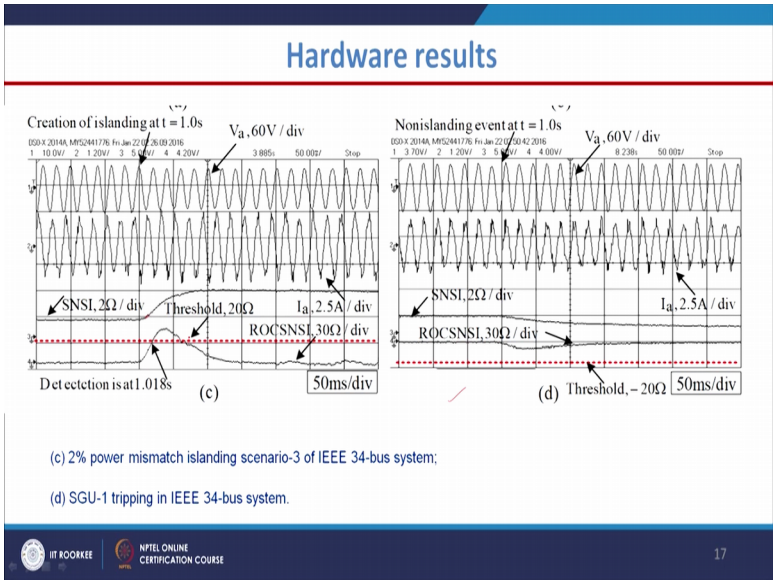
So, MATLAB 13 13 a 2013 software which is used inside it, this space that the quotes are written are embedded. And using this analogue signal, the voltage current signal it

will calculate the rate of change of superimposed negative sequence impedance and the corresponding decision is going to be fade again to the RTDS.

Through this GTAI card ai means analogue input card. So, this it will go to the RTDS and their the corresponding circuit breaker of the DGs or renewable energy sources are going to be opened. So, that the our DG will be shut down, if any islanding is there. If there is no islanding so there is no necessary to open the circuit breaker which is present near to the DGs. So, this is how this particular HIL test bed looks like.

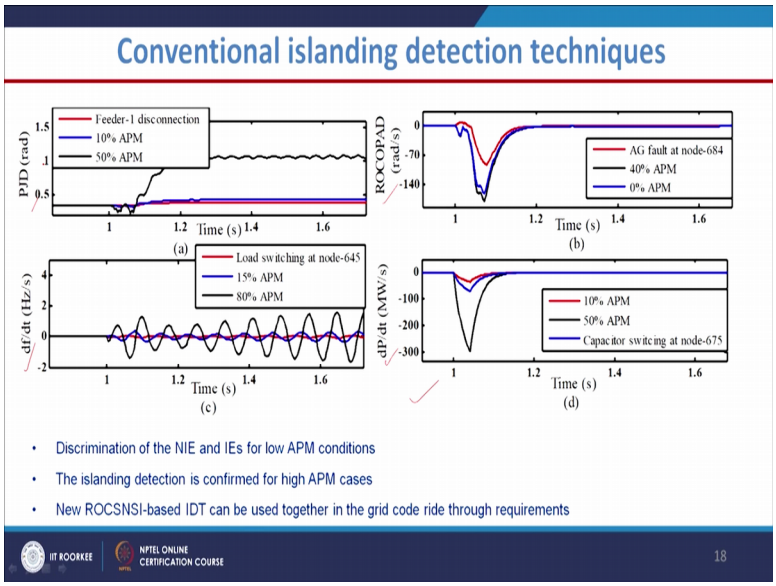
And here some of the practical pictures we have provided.

(Refer Slide Time: 29:40)



And this is one of the sample result, as far the hardware is concerned you can see this is the SNSI and it crosses the threshold; that means, the trip signal is going to be generated.

(Refer Slide Time: 29:54)

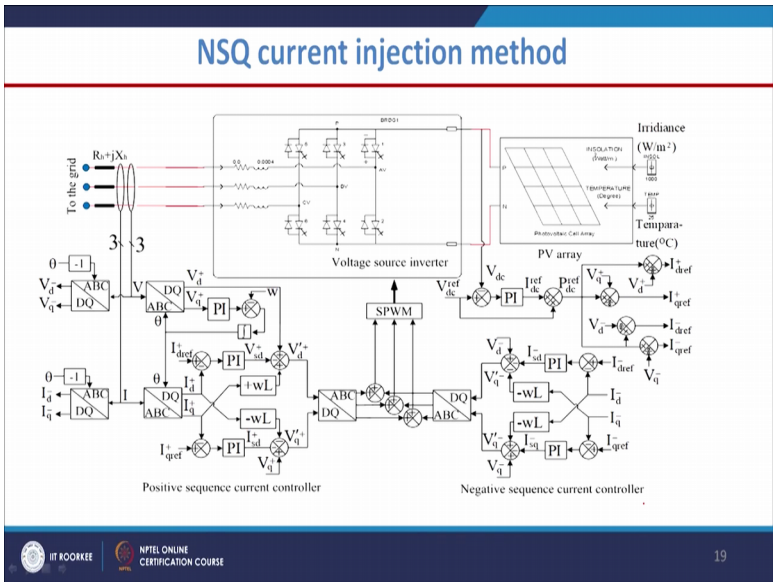


These are some of the comparison with the conventional techniques, this is for the rate of change of power and this is dP by dt and rate of change of frequency and phase jump techniques.

We have seen that in all the cases this integer is a common problem, if it is like a non detection zone basically 0 power mismatch condition, then the most of the conventional techniques. Well, whereas, this rate of change of negative sequence base technique basically operates and this is also one of the technique.

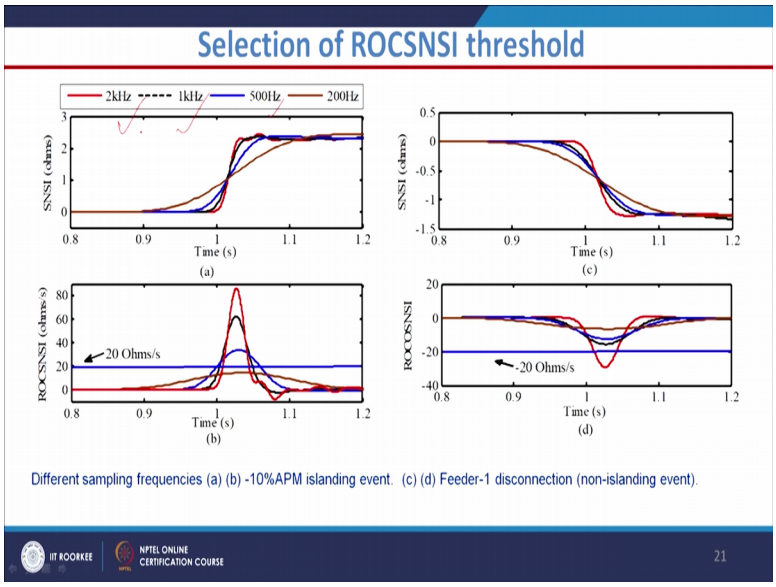
We have also realized negative sequence current injection base technique.

(Refer Slide Time: 30:28)



This is one of the acting, in of the next class I will discuss about this active islanded negative base technique, there we will discuss in more detail and this is one of the another result.

(Refer Slide Time: 30:46)

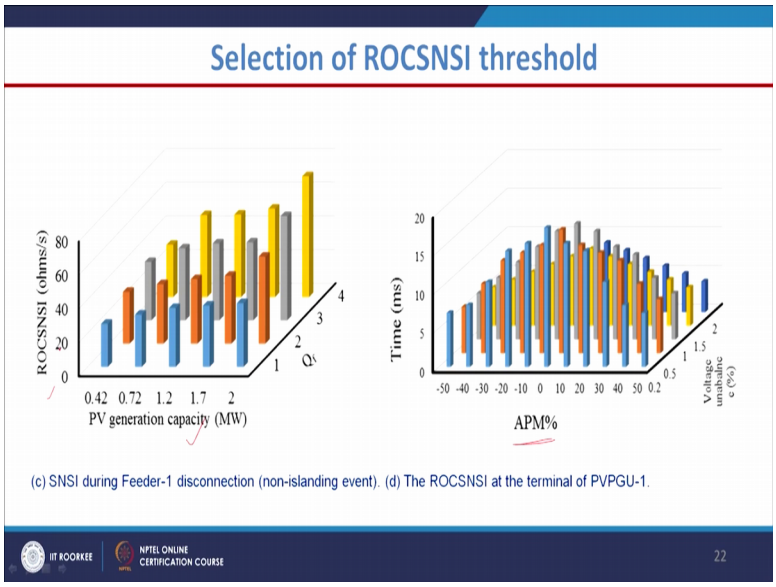


And how to select this threshold also we have studied very rigorously, where varying this sampling frequency 2 kilohertz, 1 kilohertz, 500 hertz, 200 hertz.

For different sampling frequencies also we have simulated and all corresponding superimposed negative sequence impedances and its correspond rate of change of

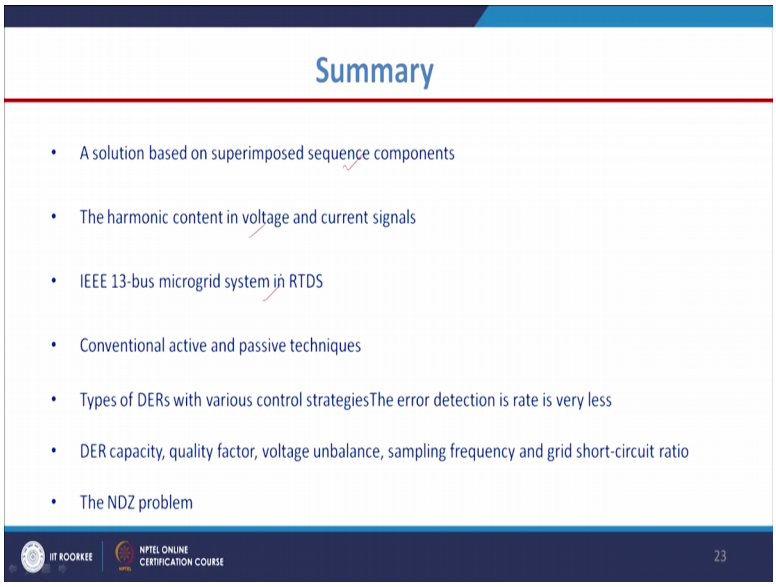
superimposed. We could see it is impedance also we have calculated and we found that based on this varying this sampling frequency the threshold also varies, that is one of the demerit of this particular technique.

(Refer Slide Time: 31:19)



And this is how this percentage of active power mismatch and the time and this is the PV generation capacity and the corresponding parameter that is rate of change of SNSI varies.

(Refer Slide Time: 31:30)



Now, in summary I will just discuss here that a solution we have provided here based on the superimposed negative sequence components and the harmonic, if present inside the voltage current signal by using a least error square base technique; we can always extract the fundamental voltage frequency phases. And in this case we have taken one 13 IEEE 13 bus system and also we have simulated 1 IEEE 34 bus system where we have also taken the tie line switches.

And single port tripping situation, high impedance faults, different islanding and non islanding situations are created and the corresponding results are basically tabulated and it is also figured out. And it is the final conclusion for this particular technique is the; it needs rigorous simulation practice by varying the sampling frequency, how to set the corresponding threshold. That is one of the major drawbacks of this particular technique.

Thank you to all of you.