

Basics of software-defined radios & practical applications
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Lecture – 08
Distortion Parameters – Part II

So, in the series of basics of software defined radios and practical applications, we have been discussing distortion parameters and it is continuation of that module. So, we have been discussing the effect of phase jitter at the output.

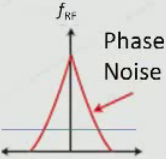
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Distortion introducing elements in receiver

Phase jitter effect example: 100 MHz clock. For having dynamic range equivalent to quantization noise from 12 bit system, what should be rms jitter (seconds)?

$$SNR_{jitter, dB} = -20 \log(2\pi f_{in} t_{j,rms})$$
$$t_{j,rms} = 0.317 \text{ ps}$$

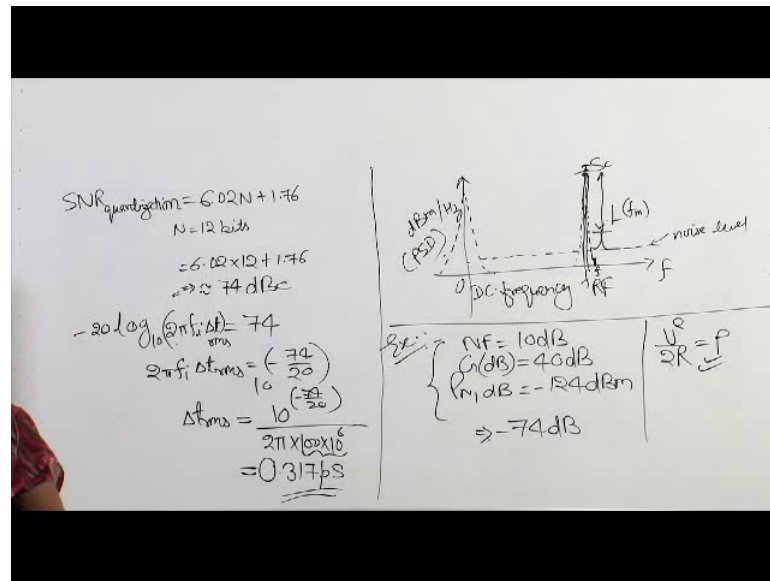
Phase noise in representation in frequency domain.



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So, we were discussing one example where we have the clock frequency of 100 megahertz, and we wanted to know what should be the jitter in seconds for having the dynamic range of it, which is equivalent to the quantization noise from the 12-bit system. So, the formulation says the SNR of due to jitter NDB is given by the formation of minus 20 log 2 pi f in and jitter in time. So, we will be using this formula again, but first of all we will be calculating the SNR due to the quantization noise.

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So, SNR due to quantization. So, we know it is 6.02 times N into 1.76 and we know that N is going as 12 bits. So, 6.02 into 12 plus 1.76; so, it becomes almost 74 dBc, now we have to know that how much jitter, how much phase shift in time in terms of rms, because it is a fluctuating parameter will be required to receive this SNR.

So, we will equate this SNR minus 20 log 10 2 pi fi in and del t rms. So, by the calculation it will become 2 pi fi del t rms minus 74 divided by 20 and it will be 10 to the power. So, 10 will go there and we can calculate our rms as 2 into pi into 100 into 10 to the power 6 hertz and 10 to the power minus 74 divided by 20.

So, by keeping this value we will be able to calculate del t jitter and it is coming out to be 0.317 equals second. So, if we want to achieve this performance only with the jitter then we have to be very small jitter in terms of pico second which is very, very hard to achieve. So, basically from this equation you can also see, that if we keep increasing our f value this value then this del t requirement will become more and more distant at it we have to get small and a smaller shift which is not possible.

So, where we have to maintain our t and we have to work on those frequency levels, where it can be manageable. Now, we have talked in terms of the time domain till now, because this del t is shift in the time domain platform, but if we plot the same thing in the frequency domain then in this diagram it is showing our frequency signal at the RF frequency.

Now, we have 2 kind of systems homodyne and heterodyne, in the homodyne system our fRF is coming directly from the lo synthesizing with lo and it is that lo has this phase jitter and this noise is here, then it will have that phase noise, will have this kind of shape and near the DC offset near the 0 frequency, it will be more concentrated and as it goes beyond the DC frequency, 0 frequency then it becomes lower in lower it becomes smaller.

Now, in case of heterodyne in this structure we have two stages and in both the staged if we have this jitter effect then it will also look like this one. So, in this diagram basically this reducing kind of curve is phase noise and this constant line is actually the quantization noise, we can say it is equally distributed it does not have any pdf of similar to the phase noise. Now, phase noise appear in the frequency domain it is easier to see there and jitter is mostly observable in the time domain.

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Relation between phase noise and jitter:

$$\sigma_{jit}^2(\tau) = \frac{2T_0^2}{\pi^2} \int_0^{f_{offset}} (L(f) \sin^2(\pi f \tau)) df$$

$\sigma_{jit}^2(\tau)$: RMS jitter in seconds

T_0 : Time period of the clock

$\tau = NT_0$

$L(f)$ = PSD of phase noise at frequency f w.r.t carrier (dBc/Hz)

f_{offset} = maximum offset frequency of interest

- Jitter measurement equipments are much less sensitive than the phase noise measurement ones.
- Jitter can be then estimated from phase noise.

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Now, phase noise is not only because of that jitter in the time domain apart from that in itself, it can have some phase in the synthesizer which is the oscillator. So, this is a relationship between this phase noise and jitter. Now, we have to remember that jitter measurement equipments are less sensitive, because jitter are very small and we are not able to capture the exact moment always precisely so it is possible that we are not able to measure them precisely, but the phase noise measurement systems are more precise.

So, by this theoretical relation between these 2, what we can do that we can use the measurement of the phase noise and then once we have the phase noise measurement in the frequency domain then we can use this formulation to get our rms jitter in seconds. So, this rms jitter depends on the time period of the clock, which is it is proportional to the square of this time bit of the clock, than this variable tau which is actually being measured after N time intervals, this tau is actually time elapsed during the end time intervals and this rms jitter is the function of this, that tau itself in this function we are integrating the multiplication of $L(f)$ with the sine square and which is a function of πf and tau.

So, f is frequency over which we are integrating and the integration limit the highest limit is f_{offset} which is the maximum offset frequency of interest which we are covering to know the effect of jitter. Now, this $L(f)$ is the psg of the phase noise at frequency f with respect to the carrier. So, if we have in frequency domain phase noise something like that. Right?

So, at 0 frequency or DC frequency at RF frequency, again we have our carrier signal and then very small phase noise will be there around the because of the carrier. So, it is not in the main information, but in the carrier signal. So, this is a S_c which I can call carrier signal. So, the main voltage here with respect to the PSD, here at this f this is what is represented by an f here.

So, PSD of the phase noise at frequency f here and PSD of the carrier signal. So, this axis here will be dBm per hertz, which is representing PSD. So, by this formulation if we know our frequency representation, we can easily calculate the rms jitter in seconds. Now, apart from the jitter and the inherent phase noise and we have seen the relation between these two also.

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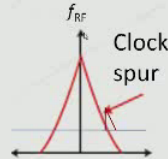
Distortion introducing elements in receiver

Spurs in clock: Spurs in frequency domain appear due to leakage from other oscillators, modulation within oscillator.

Impact of spurs in jitter :

$$\sigma_s^2(\tau) = \frac{T_0^2}{\pi^2} \sum_m I(f_m) \sin^2(\pi f_m \tau)$$

$\sigma_s^2(\tau)$: RMS jitter in seconds
 T_0 : Time period of the clock
 $\tau = NT_0$
 $I(f_m)$ = amplitude of spur w.r.t carrier (dBc)
 f_m = frequency of the spur



All spurious components have to be considered separately.

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There is something called a spurts in the clock in practical scenario, sometimes when you have your signal and this is your lo signal at f_{RF} for the homodyne signal. You can see this kind of structure which you can identify as phase noise, but sometimes you see these small a spurts, a small fluctuations in the frequency domain and these are called a spurs and which is appearing, because of the leakage from other oscillators and it can also be modulation with it oscillator by itself, it is reflection is intermingled with this one and you can see them small component here.

Now, this a spurs because they are in frequency domain, they will have an impact in the time domain too. So, this is the formula which is relating the rms jitter in seconds to this a spurs. So, if you compare it with our previous metric which was the phase noise, if you look at this it has very similar formula only difference here is that instead of using $I(f)$ we are using $I(f_m)$. So, this $I(f_m)$ is actually amplitude of this spur with respect to carrier.

So, previously we are talking about the phase noise, now we are seeing let us say it is the noise level and this is the spur here. So, the level between this two the difference between this 2 is given as $I(f_m)$. So, of course, it is very similar to the phase noise case we are dealing in the frequency domain and we are measuring our distortion which was phase noise before, now it is this is a spur formerly she is very similar and it is expected, because both are happening in the frequency domain and both are relating that frequency domain parameter to the time domain.

So, after this once we have seen then impact of different kind of noises on the ADC normally when we calculate that voltage noise level it is mostly for the full-scale usage of the ADC. So, whenever we are calculating the dynamic range of ADC, we are doing this formula 6.02 into n plus 1.76, which gives us the dynamic range in dBc, basically it is applied when we are using your ADC to the full voltage.

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Distortion introducing elements in receiver

ADC noise level for any signal level:

$$V_{n,tq} = \sqrt{10^{-3} Z_{in} \times 10^{\left(\frac{FS_{dBm} - SNR_{dBc} - S_{dBFS}}{10}\right)}}$$

$$FS_{dBm} = 10 \log \left(\frac{10^3 V_{FS,rms}^2}{Z_{in}} \right)$$

Z_{in} - Input Impedance
 $V_{FS,rms}$ - Full Scale Voltage
 SNR_{dBc} = Measured Signal to noise ratio
 S_{dBFS} = Chosen signal level

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But, we should be able to calculate the noise level also for any signal level. So, ADC noise level for any single level is given by this formulation, this formula requires the knowledge of input impedance which is given again by Z_{in} , it also require a full-scale voltage knowledge. So, that this f s dBm is can be calculated and this parameter can be used in the formulation.

Apart from that it requires the measured signal to noise ratio. So, suppose our signal is coming and it is not up to full scale, but because of the attenuation it is somewhere in between the amplitude ranges this is the measured signal to noise ratio, whatever we are saying in the signal and while this is the signal to noise ratio this s dbfs is the actually the actual amplitude level of that selected signal. So, by using this formulation we can easy calculate the ADC noise level for any particular signal level, not only the full scale.

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Including noise of ADC in overall system level noise:

- We have calculated the system noise power, including detector as follows:

$$P_{N_{tot},dBm} = P_{N_{av},dB} + NF_{RX} + G_{dB} + 10 \log(B_d)$$

$P_{N_{av},dB}$ is the available noise power (in decibels)
 G_{dB} is system gain (in decibels)
 B_d is the detector bandwidth.

ADC is voltage driven component, therefore to include the ADC noise (thermal and quantization), it is convenient to use input referred noise voltage.

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So, after covering all this thing which are impacting our ADC noise performance, let us have a look at the noise of ADC in overall system level noise. So, if you remember previously, we have calculated in the system level noise power which also includes the detector, it has 4 components P and dB, which was the available noise power which was available at the input at the antenna.

So, in the normal case, if there is no noise available there a still they have the thermal noise and if you remember we kept rotated to be minus 174, it was calculated from $k T$ naught B, now $NFRX$ is actually noise figure of the chain and we had calculated this noise figure in the previous lectures for a chain by using the cris formula, now GdB is representing the overall gain of the system, which is given in the decidels and this Bd is actually the greater bandwidth and we take the logarithmic of this because all of this are given in the dB form.

Now, if we do the calculation for this one, let us take few values, let us say noise figure is equal to the, if NF is equal to the 10 db gain is given as 40 db and we also require detector bandwidth let us say $PNdB$ is minus 124 dBm, then we want to calculate the this PN total and we have calculated in the previous example by using this factors, it was coming out to be minus 74 db.

So, this total power we have calculated earlier, now we want to see that what will be the effect of excluding ADC noise in the overall system level noise. So, first of all we should

appreciate that we had done all the calculation in the power domain till now. So, basically what we had done that we have taken, whatever voltage was available there and we had done V^2 into $2R$ calculated into power and then we had done the a convert it into dB a scale.

Now our ADC is a voltage driven component it means, that if you want to include our ADC noise it will be easy to appreciate if everything in the voltage form. So, these are the step for including the ADC noise and to get the actually voltage of the total noise of the whole system including our RFIF components including our ADC quantization noise etcetera everything.

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Steps for including ADC Noise:

1. Convert the noise power to voltage, by using input impedance of converter.
 - *Input impedance of ADC is quite high (up to 1 K Ω) and it has to be matched to 50 Ω .
2. Calculate the input referred noise due to ADC (including quantization noise)

$$V_{N,ADC} = V_{FS,rms} \times 10^{-\frac{SNR_{ADC}}{20}}$$

$V_{FS,rms}$ = full scale rms voltage for ADC

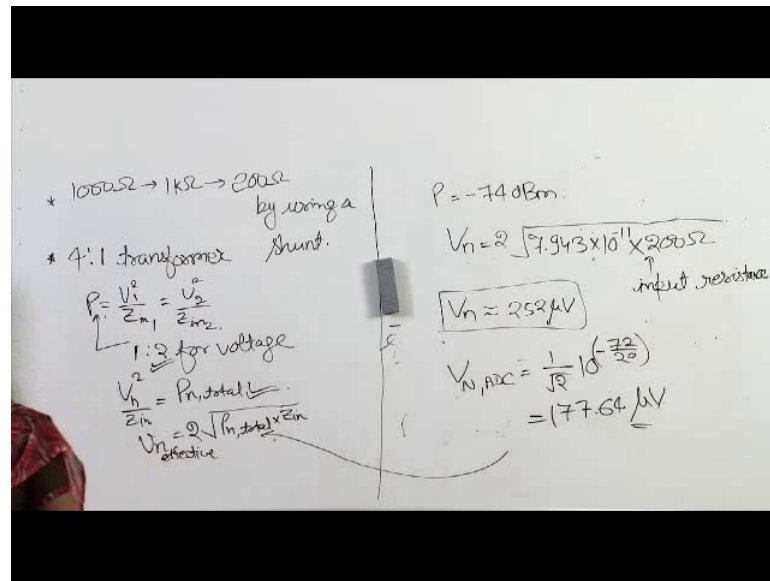
Example: 14-bit converter, SNR of 72 dB and 2 volt peak to peak full voltage.
(noise due to ADC: 177.64 micro-volt)

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So, first of all first step will be calculate, sorry convert the noise power to voltage by using input impedance of the converter. So, first of all we have to remember that input impedance of ADC is quite high up to 1 kilohertz, now in the previous lectures I have mentioned that in the RF domain most of the cables, they are meshed mesh to the 50-ohm load, but because of our impedance of ADC is up to 1 kilo ohm and it has to mesh to 50 ohm.

So, first of all we have to do the calculation for that one. So, how do we do that we have to convert it into voltage. So, we can do 2 things this impedance has to be eventually matched to the 50 ohm.

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So, in the first step you are we will be brought down to 200 ohm, by using a shunt what is 10 it is 200 ohm, it has to be meshed to the our 50-ohm system. So, then we use 4 ratio 1 transformer. So, by using this transformation 200-ohm impedance is brought down to 50 ohm and it is meshed to the cable impedance required, now because we are doing this transformation then our voltage, because this is the power even with the transformer action we have to convert this power. Right?

So, if the impedance ratio is 4 ratio 1, then voltage ratio will be what it will be 1 ratio 2 for voltage, because we want to conserve our, we will have the same power. So, we are conserving the power it is the same and the voltage ratio will be 1 ratio 2, now first step was to convert our power into the voltage.

So, we will convert it back into this, but we have to remember that we have this ratio of 2 also. So, our V_n actually becomes, twice of whatever we will calculates from this formula. So, V_n effective becomes twice of under root of P noise total into Z_{in} , basically we will be calculating our voltage; so for our previous example, when we had minus 74 dB our output power.

Then, this we want to use here, but it will be in the form of watt. So, let us convert this minus 74 dB into watts. So, we will start up a calculation from power to voltage level our original power level. So, our original power level was minus 74 dBm. So, we will

convert it back into a voltage and then this way we can calculate our V_n 2 times, because 200 ohms is our input resistance.

So, with this calculation we will get our voltage and it will be in the very small range. So, after calculation this is the voltage we are getting, first calculation of this voltage. So, once we have this voltage at the input of the ADC, because of the system which was attached to ADC, before the ADC means due to RF and IF components and the receiver chain.

Now, apart from that let us calculate the input referred noise, due to ADC which also includes the contention noise. So, we can see the formulations in this slide, that it is dependent on 2 things first is full scale rms voltage for ADC and the second one is actually, SNR which is the full scale is SNR which we calculated by using our dynamic range formula and by this we are able to get our voltage ADC noise.

Now we can do it calculation for the 14 bit converter and SNR of 72 dB and 2 volt peak to peak full voltage we have to calculate the noise in the volts. So, it is a 14-bit converter and we will be having S_n of 22, 72 dB, because there is some noise. So, that SNR of 72 we can put in this formula here, now V_{fs} rms has to be calculated for 2-volt peak to peak full voltage. It is 2-volt peak to peak. So, from 0 to peak it will be only 1 volt. So, we will calculate the rms of this and we will apply the formula there.

So, 14-bit information is not being used, because SNR is already being given here and it is impacted by other noises. So, we will just ignore this information and based on these 2 information we will do over calculation. So, $V_{N1ADC} = 1 \text{ upon } \sqrt{2}$ which is the rms value there and then minus 72 upon 20 and it is on the 10 to the power.

So, by this calculation we will get our value it should again should be very small, because it is a noise value. So, by calculation it is coming out to be in micro volts range again 177.664 micro volts. So now, we know the voltage equivalent of the noise because of the all the RF chain, we know the voltage equivalent because of the ADC and the total noise contribution will be the addition of these 2 rms value.

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Distortion introducing elements in receiver

3. Noise contribution can then be combined together.

$$V_{N,RX} = \sqrt{V_{iN,IF}^2 + V_{N,ADC}^2}$$

* Represents noise at ADC, including RF, IF, analog and quantization steps.
* Impact of other noises can be investigated on ADC SNR and final calculations can be done for new SNR.

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So, the voltage value of the IF chain and then voltage value of noise due to ADC they are added together in the square sense and then we have taken the square root.

So, when we calculate our noise like this then we have total noise, because of ADC RFIF n log and all the quantization steps. Now in this calculation, we have used only the impact of SNR given 2 us and other noises can also be investigated by including those effect in the SNR of ADC and then final calculation can be done for new SNR for that one. So, for this for our given example, what will be the overall noise contribution.

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$V_{n,IF} = 252 \mu V$
 $V_{n,ADC} = 177.64 \mu V$
 $V_{n,RX} = 308.1 \mu V$

$P = -74 \text{ dBm}$
 $V_n = 252 \mu V$ (induct resistance)
 $V_{n,ADC} = \frac{1}{\sqrt{2}} 10^{\left(\frac{-74}{20}\right)} = 177.64 \mu V$

So, previously VN1IF we have calculated and VN1ADC, we have already calculated VN1ADC is 177.6464 micro volt and our previous value for IFs was 252 microvolt. So, and total VN1RX chain will be the squaring of this and this information value is coming out to be again in the micro voltages for my calculation it is coming out to be 308.1 micro volt. So, in this we can do the calculation for this one.

Now, we have seen that what will be the effect of noise in voltage for the ADC, because it is a voltage driven component, but it is still interesting to know the effective noise figure of the ADC. So, at least theoretically; so, that if we know the noise figure of the chain and we want to incorporate this element ADC at the end of the receiver, then we can do. So, this formula is giving the relation between different parameters with the noise figure of the ADC.

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Effective noise figure of ADC:

$$NF_{ADC,dB} = 10 \log \left(\frac{V_{ADC,rms}^2}{Z_{in} 10^{-3} s} \right) - SNR_{ADC} - 10 \log \left(\frac{f_s}{2B} \right) - 10 \log \left(\frac{kTB}{10^{-3}} \right)$$

$V_{ADC,rms}$ is the rms value of the ADC input voltage range.
 f_s is the sampling frequency (in hertz).
 Z_{in} is the converter input impedance.
 SNR_{ADC} is the signal-to-noise ratio of the converter.
 B is the bandwidth (in hertz).
 T is the system temperature (in Kelvin).
 k is Boltzmanns constant (1.38×10^{-23} J/K).

Calculate: noise figure of an ADC for 100MHz sampling rate, $B=1$ Hz, $Z_{in}=200\Omega$, 1 Volt peak voltage input to ADC, S/N of 76 dBc.

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So, as we can see it is dependent on the rms voltage value of the ADC, which is applied at the input voltage input port then Z_{in} is the converter input impedance in our case it was 1 kilo ohm in our previous, example SNR ADC which is signal to noise ratio at full scale.

So, it is again the theoretical SNR the f_s is the sampling frequency here and B is basically the bandwidth for which we are calculating this. So, this bandwidth is taken in the hertz and this is again the noise component which is coming from the temperature, k is the Boltzmann constant B is the bandwidth again.

So, as an example before the next lecture let us calculate the noise figure of this ADC, if you are given that f_s which is the sampling rate it is equal to 100 megahertz, the bandwidth is given as 1 hertz input impedance is 200 ohm and the voltage which is applied to is given as 1 volt peak voltage, please note it is not peak to peak voltage it is only peak voltage and you are given that SNR of this ADC is 76 dBc.

So, keeping this in mind let us calculate the effective price figure of the ADC. So, in the next lecture we will start from this example and we will see what the noise figure we are getting and then we will continue with the distortion parameters.

Thank you.