Basics of software-defined radios & practical applications

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Lecture – 05
Software-defined radio architecture Part III

Hello everyone in the series of basics of software defined radios and practical applications. We were discussing the software defined radio architectures.

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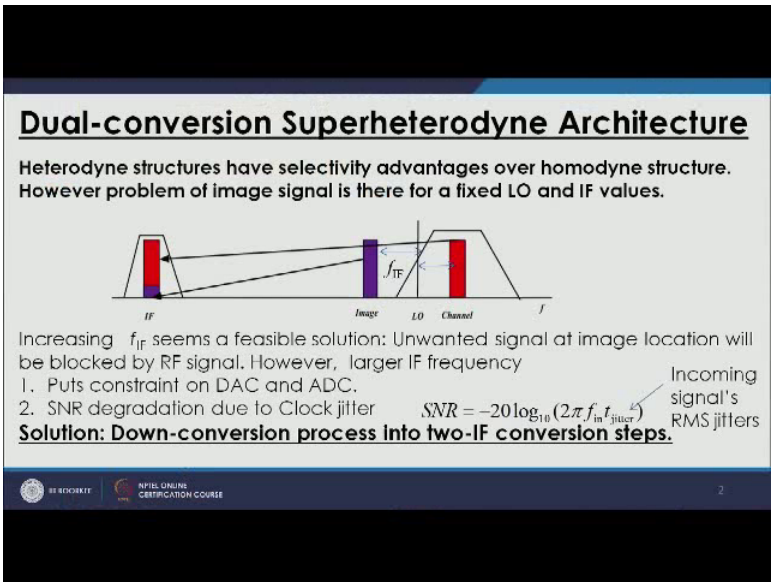

And this is part 3 of the same series. So, we have discussed Homodyne architecture, we have discussed super Heterodyne architecture, and we know that Heterodyne a structures have the selectivity advantages over the Homodyne a structure, but we has seen that there is a problem of image signal which appears at the higher frequency if it is a particular distance from the LO.

So, we had seen that in the Heterodyne condition, we can actually select our LO and we can tune out this image signal, but in the real practical scenario basically this LO value and the I F values they are fixed values, they are pre-selected values, we are not supposed to change them.

So, what could be one of the solution, can be making the I F so, large that the band pass filter will not select any component of this image frequency, and in this case the unwanted signal at the image location will be blocked by the R F signal. So, it will looks

like a very easy and simple solution. So, what is the catch here? What is the problem? The problem is that when we have the larger I F frequency than our a to d converter and e 2 a converter.

They have to deal with this frequency and then by the nuquist criteria, we have to have the sampling rate which is more than twice of it is I frequency which is the maximum frequency it will be achieving their. Now we do not want to put that constraint on the DAC and ADC, and that is why we have gone to Heterodyne architecture in the first place.

So, it is one of the reason the another reason is that if we have clock jitter in our clock, which is sampling for the ADC and DACs then there is a certain SNR degradation re degradation. So, we can see this degradation it is minus negative of 20 log 10 2 pi f in t jitter, this t jitter is actually the fluctuation of the sampling clock in the time domain.

So, basically what happens that because there is some phase noise their it is not starting at a particular stands, it is it can jump little bit here and there. So, it is called the in coming signals r m s jitter, which is coming from which is collating with that LO, and the second factor in this expression is f in which is the incoming frequency.

So, for sure when we have high IF ADC or DAC has to deal with this I this fn, and then signal to noise ratio goes up. So, it is degradation and signal to noise ratio. So, what can be the solution for this one, one solution can be to avoid the high If, but providing the same IF in 2 convergent steps.

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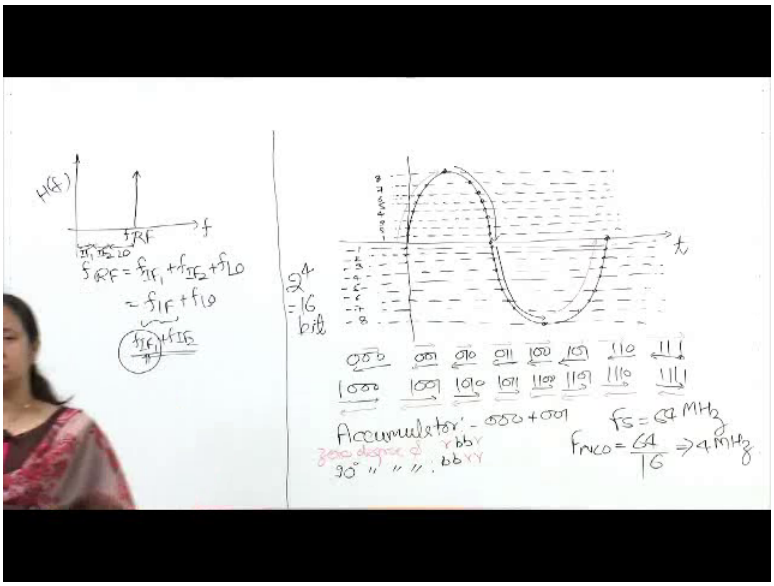

So, if it is frequency domain and let us say this our amplitude of the signal system response, then is suppose this is the R F signal we have to reach, it can be sum of IF 1 then IF 2 and then LO right. So, R F, f R F is the sum of fIF 1 plus fIF 2 plus fLO, it is equivalent to fIF plus fLO where is this fIF is actually summation of IF 1 plus IF 2.

In that case because our ADC is dealing with only the last stage convergent stage, before it is applied to actually ADC, then this is the frequency which will be actually reaching at the ADC and the sampling constraint will be decided by this frequency which is small. So, some period required will be small, similarly the SNR which is defined by f in which is also decided by this fIF 1. So, the one solution can be down convergent process into 2 IF convergence steps, now we know that we can increase the number of steps, but then in the Heterodyne structure complexity increases.

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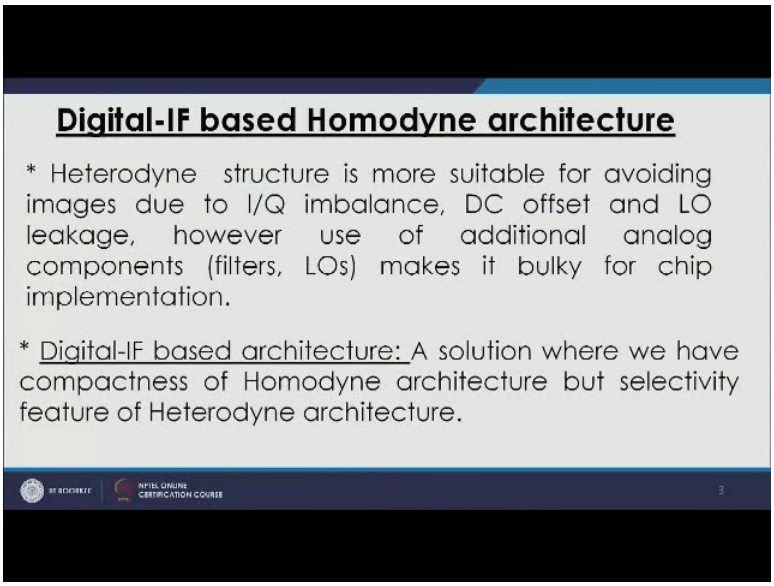

So, we can avoid images due to I/Q imbalance DC offset, we can also avoid LO leakage, but it is on the at the cost of making the structural bulky.

In dual down convergent structure it becomes even more bulkier because we have 2 steps, two kind of LOs two kind of filters mixers everything will be twice. So, then what can be solution that we want to retain the properties of the Heterodyne structure, but we also want to have a compact design. So, the solution comes in the form of digital IF base architecture. So, this is solution where we have the compactness of the Homodyne structure, but selectivity feature of the Heterodyne architecture.

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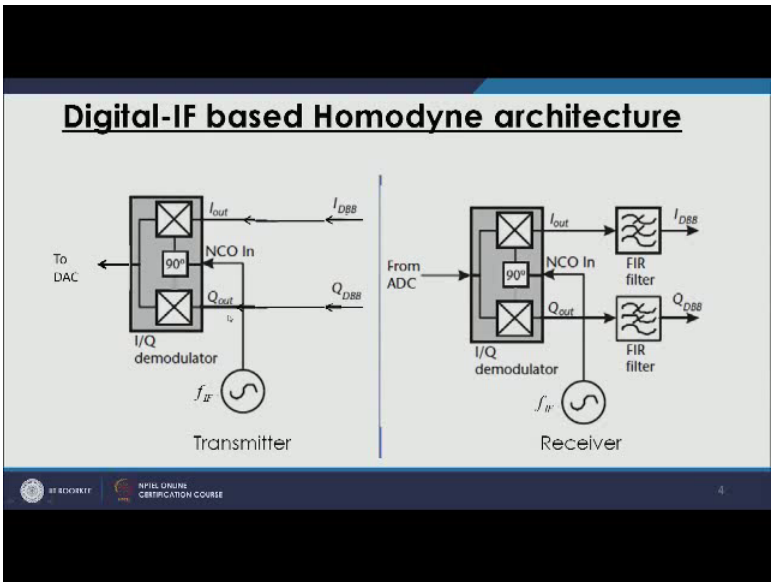

So, this is the block diagram of the transmitter and receiver, which is the digital IF based architecture. So, you can see that from the baseband we are directly having our I and Q data in phase data, and then digital numerically control oscillator, is actually giving the sine and cosine components of both the directions, now the I/Q modulator it is at the frequency, but this frequencies is synthesized in the additional domain basically, and it is provided to DAC.

So, it is already I F converted, but it is has only structures which are required for the Homodyne structure, because we do not need additional LO 1 which was required in the original Heterodyne structure, similar in ADC the is signal is coming here and we have received over in phase and out of phase by multiplying it with respective I and Q components and after that, doing the filtering, low pass filtering to achieve over exact I baseband data, and Q baseband data. So, what is the main component here? The main component in this architecture numerically control oscillator, here additional we are using the basically analogue oscillators.

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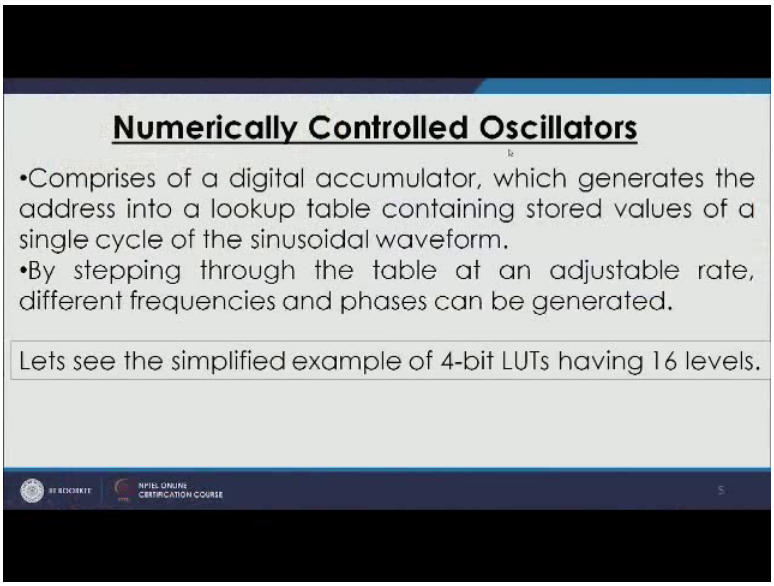

Now, this is something which comprise of a additional accumulator which generates the address into a look up table, which contains this stored value of a single cycle of the sinusoidal waveform. Now we can step for this table by giving that particular address and accordingly at a adjustable rate, we can have different frequencies and we can different phases also. So, if we want to said properly let us have an example of the 4-bit LUTs, which have 16 levels. So, so let us say this is example of single sinusoidal case with respect to t, this is our sinusoid. So, it is 16 level. So, 8 level upper, and 8 level lower right.

So, we have these values. So now, what happens these values they will be stored in a particular address there right. So, these are these values which we want to read. So, if you see we have 1,2,3,4,5,6,7,8 minus 1, minus 2, minus 3, minus 4, minus 5, minus 6, minus 7, minus 8, these are the different levels here, now each of these values are given in a particular address book, for example, if you want to read 1 the address will be our positive values were. So, it will be 3-digit value only because we has 8 levels we are. So, it will be 0 0 1, 0 1 0, 0 1 1, 1 0 0, 1 0 1 and of course, we have 0 0 0.

So, these are the 8 levels which are giving these amplitude values, and similar in the negative side, we will put 1 to signify the negative value and we can have our all these values. So, we just put 1 is in front of each of than, and which is have positive value we can have negative value, now let us see. So, we have seen that the upper positive levels

are shown by this values and the lower values minus 1 minus 2 are achieved by putting 1 in front of this is the metal value they are representing the negative amplitudes. So, suppose you want to read these values these amplitudes there.

So, we will read first this value, this address instituting this amplitude, then this address is storing this address, then this one is storing the next one, and as we keep going to this addresses this is showing this direction. Now I want we want to read this this sequence, then we will start going to in opposite direction. So, we will start decreasing it by 1 values again, when you want to go that way it is still decreasing. So, negative values will be write there, and once it goes to this direction, then it will start becoming less negative.

So, in this way these are the locations where we have stored this particular amplitude value. So, suppose you want to start from 0 phase. So, we will start our Accumulator will start with 0 0 0 and then it will keep increasing 1 bit of that, and it can read the other values in this direction, suppose you want to have 90 degree shift, then we will have the shift we will start from this point from this point in it will start reading these values, and when it will start reading this values it is the actually following this path. So, for 0-degree phase it is red black black red combination, 90-degree phase difference it will be starting from black. So, it will become black black and then it will be red red.

So, the black is the direction when you are address is our decreasing in nature, and when you are the address are becoming positive in nature then in their represent by black. So, similarly by 1 at 180 degree you can have given at black red red and then black. So, it will keep repeating like this. So, you can see that it is actually a rotation of the addresses, which we are achieving here.

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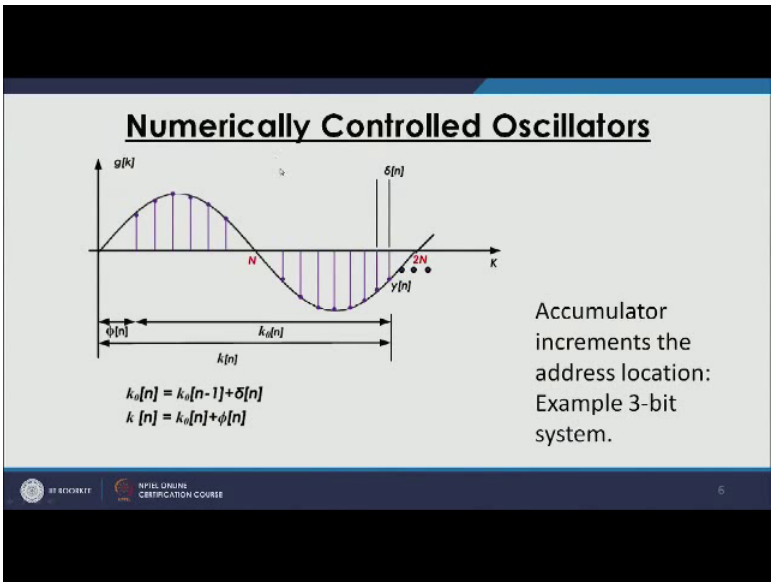

So, for an example of 3-bit system 8 address location will be there and this is the diagram which is showing that how we can read it, there delta n is actually the sample is difference and difference between 2 samples they are, k naught n is representing your address location and as you can see this address location is updated by del n.

So, k naught n minus n was the previous address and we add to it and we achieve the next location in the k direction, now if you want to have a phase shift the phi n ways represent it here this phase shift you can achieve y multiplying delta ns by the number of location you want to miss, and from that shift you can again take up the value of k n shift at the thing.

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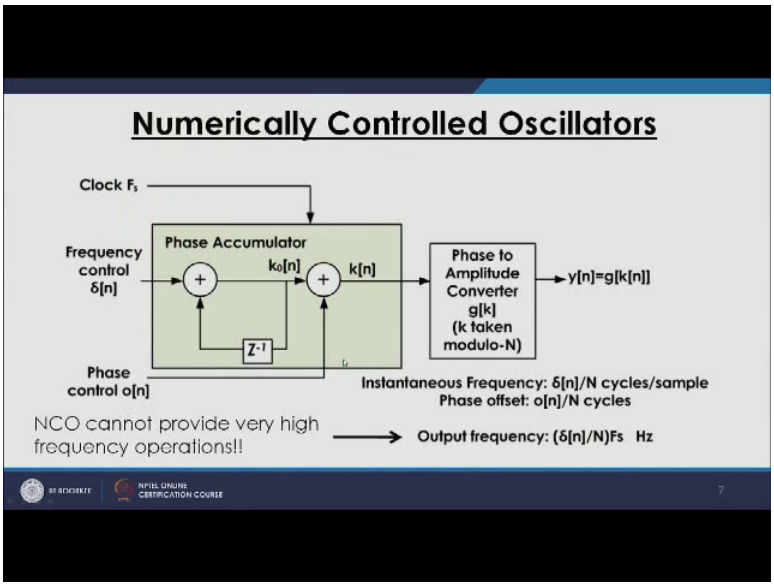

So, this is the block diagonal how it is applied basically you have a sampling clock here, which is going into your numerically controlled oscillator, and frequency control is applied by del n, this k naught n is implemented by a delay element which is which keep updating the address value, and if you have to jump the address value according to some phase control, that on is added here.

So, that it can directly jum to that address from where you will start reading it, now you have seen this this example how you can see the phase shift there. Now suppose you want to have the frequency you want to increase the frequency how would you do this. So, as you can see in this example that you had your 16 level. So, you have you have 16 addresses. So, if you sampling rate is less than 64 megahertz, Fs is equal to 64 megahertz. So, it is sampling all this is this is 1 by 1 and it is doing 16 times to actually complete 1 sinusoidal.

So, what will be the frequency of the oscillator? If what will frequency of this sinusoidal, it will be actually 64 divided by 16. So, 4 megahertz will be the frequency of this sinusoid if the frequency of the sampler is 64 megahertz. So, in this way we can also control the frequency of our sinusoid. So, if you want to increase the frequency what we have to do, we have to actually increase the either sampling frequency itself Fs, or we have to decrease our number of levels, similarly if you want to increase sorry if you want

to decrease, your and few frequencies sinusoid frequency then you can increase the level, and you will have first output frequency from this system.

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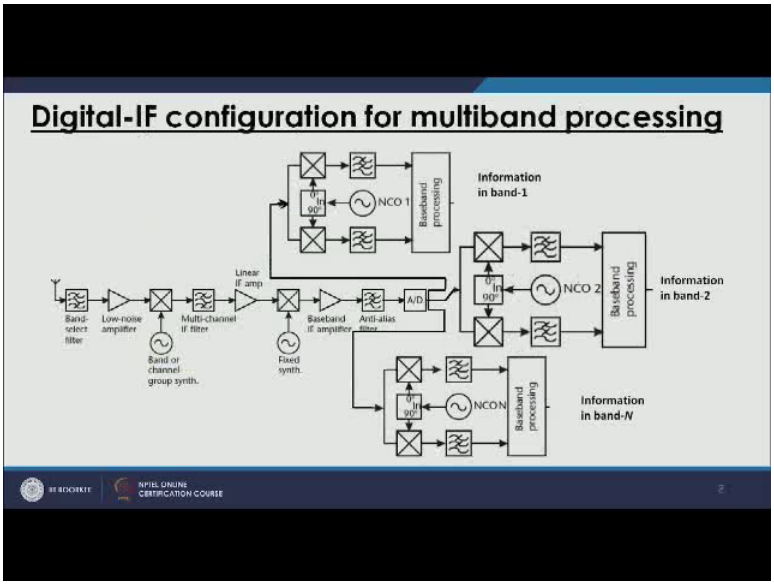

So, the good thing is that in the system you are doing everything everything digitally. So, everything is much precise you have save this addresses with exact amplitude at this particular addresses and by exact shift you can achieve proper phase and frequency. So, if they are very precise as compare to their analogue counterpart, now where can we use it they are very useful because there everything is happening in digital domain, when you have to do the filtering you can do in digital domain it is post processing it is much easier than the analogue filters, analogue filters also have the tendency to have some errors, they are not perfect in digital domain you can define and you can also reconsider this properties. So, basically you are returning the value and advantages of Heterodynes structure, but you have a smaller structure like Homodyne structure.

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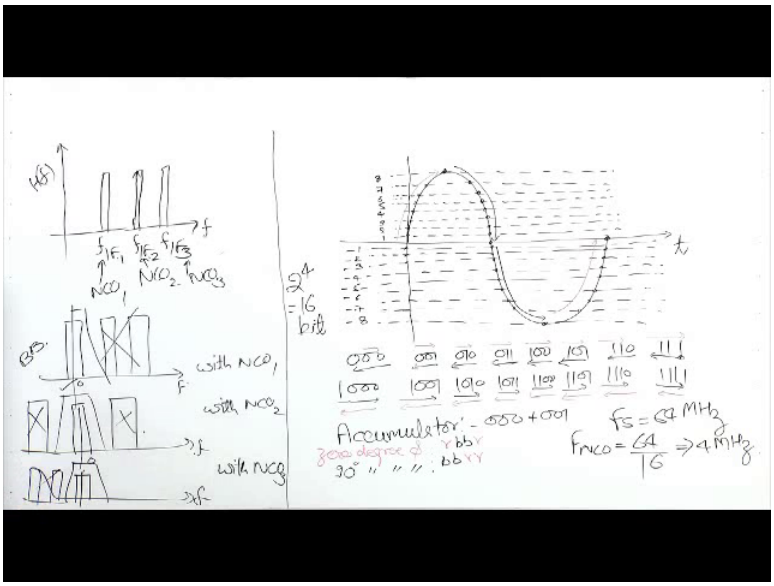

So, how we can use it for the multiple processing there is one example here. So, in current scenario in modern communication systems, we are most dealing with multiple channels, means you might be using 3 also, you might be having 4 G option yours cell also, and whenever you are not catching 3 G or 4 G even you will be catching 2 G. So, your handset should have the option for a receiving all this frequencies.

So, this kind of architecture say this kind of frontend or multichannel multiple frontends for example, if this is the frequency this is a fRF 1 for one channel, fRF 2 for the second channel, fRF 3 for the third channel. So, it is possible that you will have 3 frequency is coming or most of the cases we will be have only one of the frequencies, but your frontend should be able to support any of those. So, when this is single is there and these 2 or not, it is able to receive it and then it is summing and these 2 are not there it is a still should be able to receive them.

So, this is that kind of structure. So, in that see we can see we have band select filter. So, it is multi band kind of filter, it will allow all these three frequencies to come whenever they are available, there then low, low noise amplifier is there. So, that we can have the good sensitivity when it reaches the ADC, after that we have multiple IF filter after doing the first IF conversion there, again we have amplification because they will we have some losses in this filter.

Now after that the same signal till now we are using same IF frequency right. So, this is this is fixed frequency we have do we have done the A to D conversion. So, in digital domain all this singles are there. So, they were fRF 1, fRF 2, fRF 3 before now they have become fIF one, fIF 2, and fIF 3 in the system.

So, there in if domain now they are near the baseband, but they are still there; so how can we receive them, we can we will be dealing them like their multi carrier single system, and after that by demoliting them by using different NCOs we will be getting your particular band. So, NCO 1, 2 and 3 will be used to select this.

So, NCO 1, NCO 2 and NCO 3 will be down converting them in the digital domain, we do not need hardware for that they will be done and that 2 components with respect to the NCO will be removed. So, for this one it will be here with NCO 1, and other two will be here and then you will be a low pass filter, which will not allowed this to come and you will get this signal, the second one with the NCO 2, how will it look?

This is the baseband representation mean say it is very much near the 0 frequency. So, in this case when you do the down conversion with this frequency, than your middle signal is here, and the next signal is here, and the previous signal is here, and then again you select only this signal and these 2 signals will not be there, same with the NCO 3 in the third case, other 2 signal will be away from here.

So, you will be able to get third signal. So, if this can be repeated for and frequencies at shown in this figure, things are happening in digital domain. So, we are saving lots of cost in terms of hardware secretary. So, that till now we have covered the Heterodyne architecture Homodyne and then we have seen the digital If, digital IF we can also do the down load conversion because in digital domain and it will not have extra cost, there may be processing cost, but that is more accurate as compare with their analogue counterparts, now or let us go back to our original SDR concept, way which was the concept of pure digital RF frontends when we wanted to have the DSP, and you wanted to send this DSP to a digital to analogue converter and receive directly at that analogue to digital converter and do the processing.

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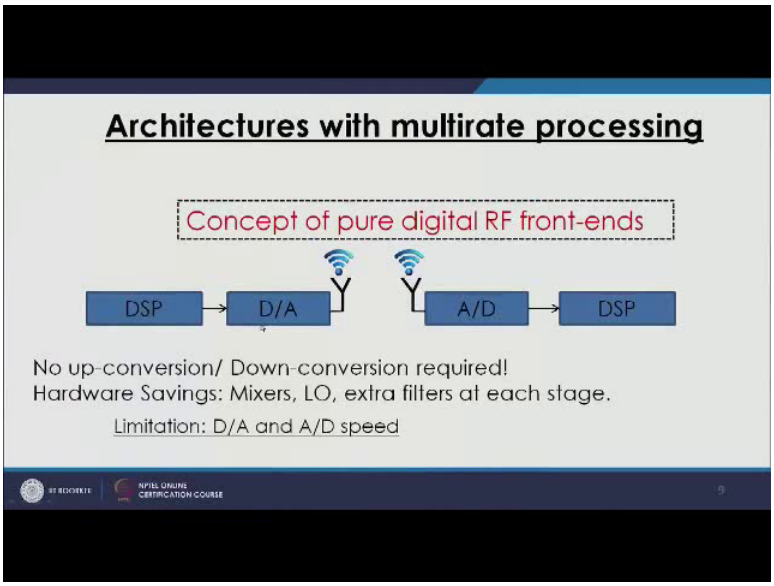

We do not want any other analogue components here. So now, up conversion down conversion is required, and we will be saving the hardware which are mixers LO extra filters h at each stage. So, what is what was the limitation here? Limitation was D to A and A to D speed. So, in the next lecture we will be covering these two components that is this feet limitation of D to A and A to D structure.