

Power Electronics with Wide Bandgap Devices
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Lecture-9

GATE DRIVE FOR DYNAMIC CHARACTERIZATION – Continue 2

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Welcome to the course on power electronics with Wide Band Gap devices. Today I am going to discuss an example of gate drive design. So you have already seen, how we can design the gate drive or what are the parameters that consists in gate drive circuit. So these parameters and what are the conditions we need to consider with respect to each parameter that already I have discussed. Now today I will take an example and discuss in details how the parameters value should be. So I will take an example of silicon carbide device and take some parameters from the data sheet of that particular device and design gate drive for that particular device. This method can be utilized for designing gate drive for any other circuit.

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Case Study

Part number	Breakdown voltage	Rated current	Gate charge	Turn-on $\frac{dv}{dt}$	Turn-off $\frac{dv}{dt}$	Turn-on Voltage (V_g)
C2M0080120D Wolfspeed	1200V	24A @ 100°C	49.2nC	35V/ns	47V/ns	20V

Turn-off voltage (V_{EE})

-5V

Gate Resistance (Internal)

4.6 Ω

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So let's consider one silicon carbide device. So the device part number is, so I am writing the part number of the device so that you can actually get the parameter of the device from the datasheet. So this is the part number of the device C2M0080120D. This is from Wolfspeed. You can use any other silicon carbide device or GaN device for the design. So this device data sheet if you open you will get the required parameters. So the required parameters are first is the breakdown voltage of the device. That is 1200 volts. Second is the rated current. So whenever we consider any device, then first thing we need to look in the device data sheet is

rated voltage and rated current. So this is 24 ampere at 100 degree Celsius. Temperature is very important because as temperature changes current rating will also change. Then gate charge. So in designing of gate drive the important parameter is the input capacitance of the device. Which we can actually consider the capacitance and the charge required to charge that input capacitance. So, that is given in the data sheet as 49.2 nanocoulomb. Then other things which is required for common mode transient immunity is turn ON and turn OFF dV/dT . That is 35 volts per nanosecond. Turn OFF dV/dT is 47 volt per nanosecond. So you can see two different dV/dT is given with respect to turn on and turn off ok. Now another thing important is that what is the required voltage so if it is one only one voltage so then we can give that if two different voltage levels are required so during turn off time for silicon carbide and gallium nitride they need negative voltage. So that also is very important for designing of gate drive. So basically the turn ON gate voltage or VCC this we have represented in previous discussion in terms of VCC. This is 20 volts. Then turn OFF voltage which we have represented in terms of VEE in previous discussion. This VCC that is VEE, this is given as minus 5 volts. So, now we have almost all the parameters which we need for the design. The last parameter which we need is the gate resistance. So, generally the gate resistance will be given in the data sheet that will be with respect to the internal gate resistance of the device. So, the internal gate resistance of the device, it is given for this particular silicon carbide device is 4.6 ohm. So, these are the required parameters, which we need for designing of gate driver, ok. So now you can write down all these parameters or you can just open the data sheet and take all these parameters from the data sheet if the device is different. So, all these associated parameters for particular device you can just note down then you can follow the same procedure.

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Signal Isolator-Case Study

Step 1: $V_{iso-si} > V_{BD} (= 1200V)$
 $V_{iso-si} > \underline{1200V}$

Step 2: $CMTI > \max\left(\frac{dV}{dt}(on), \frac{dV}{dt}(off)\right)$
 $\frac{dV}{dt}(off) > \frac{dV}{dt}(on)$
 $CMTI > \frac{dV}{dt}(off) (= \underline{47V/ns})$

Step 3: $f_{sw} = \underline{100KHz}$

Step 4: $t_{pdsi} = 1\% \times \text{switching period}$
 $= 1\% \times \frac{1}{f_{sw}} = \underline{100ns}$

→ Step 5; Select the suitable signal isolator.
ISO7841x from TI



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So, then the procedure, the first component in the procedure is signal isolator. So, signal isolator if we have to design or select any particular signal isolator, so then few condition it need to satisfy with respect to particular device. Because you know we cannot utilize any signal isolator

for like designing of gate drive. So, what are the parameters that this signal isolator should satisfy? So, first thing is the first parameter we need to consider is the voltage isolation. So, isolation voltage in case of signal isolator, signal isolator, so that should be more than the breakdown voltage of the device. So, in the previous slide already I have shown, the breakdown voltage of this particular device is 1200 volts. So, basically this should be greater than the breakdown voltage of the device. So, I am representing breakdown voltage of the device in terms of VBD. So, then this V isolator, so isolation should be more than 1200 volts. So, this V breakdown is given for this particular device is 1200 volts. So, it should be anything more than 1200 volts. So, V isolation for this signal isolator should be more than 1200 volts. So, you can choose any isolator that can provide that much voltage more than 1200 volts that will be given suitable for this particular device gate drive. So, now the second thing which I told you like there are two parameters important in this signal isolator. First is the isolation level and second is the common mode transient immunity, or CMTI. So, CMTI, if we have to consider then what we have to do? So CMTI depends on dv/dt rating of the device. So, it should be the CMTI rating should be more than maximum dv/dt either during ON or during OFF. Okay, so maximum dv/dt whenever it will occur either ON condition or OFF condition. So, in the previous parameters, I have written dv/dt for turn ON and turn OFF time. So, for turn ON time it is written 35 volts per nanosecond and for turn OFF time it is written as 47 volts per nanosecond. CMTI is greater than maximum of dV/dt(on), dV/dt(off).

$$CMTI > \max\left(\frac{dv}{dt}(on), \frac{dv}{dt}(off)\right)$$

dV/dt(off) is greater than dv/dt(on).

$$\frac{dv}{dt}(off) > \frac{dv}{dt}(on)$$

So then, dv/dt during OFF time is maximum and that is equal to 47 volts per nanosecond and this value is so CMTI we have to select, so CMTI we have to select more than dv/dt of time. because during off time we will get maximum dv/dt. So, it will be equal to 47 volt per nanosecond.

$$CMTI > \frac{dv}{dt}(off) (= 47V/ns)$$

So, this value we have to consider for designing of CMTI. So, you got the isolation voltage and the CMTI. These are the main parameters for designing the signal isolator or selecting the signal isolator. The third parameter is we have to consider switching frequency. Either like for your application the switching frequency will be given or you can assume switching frequency based on the application or like based on your design. So here let's say in this design we are considering switching frequency of 100 kilohertz. Now, so this, let's say this is step 1, step 2, step 1, step 2, then step 3. Okay, now switching frequency is selected. Switching frequency if we have then the last parameter we need to consider in this

particular component is the propagation delay. So, propagation delay it should be generally considered as 1% of the switching period. Means the propagation delay, if we have to consider, so generally propagation delay for signal isolator, so this we can consider 1 percent of switching period. means 1% of 1 by switching frequency. So switching frequency we can get from the previous step that is 100 kilohertz. If we put this value here then it will come around 100 nanosecond. So now you can see, so these are the parameters we need to consider, the voltage, isolation voltage, the CMTI, switching frequency, propagation delay. So switching frequency we directly not require, so basically propagation delay is required for this. signal isolator and it can be calculated by using switching frequency. Now if we have all this parameter then the last step we have to select, so we got all this parameter from this design like you can get the parameters different parameters from the data sheet and then once you have all this parameter, now the last step step 5, select the signal isolator suitable, so in this particular design based on the ratings the signal isolator which is selected so that is ISO7841X. This is from Texas Instrument. So this is the signal isolator which satisfy all the required conditions and this is manufactured by Texas Instrument. So, this will be suitable for this particular device as signal isolator. Now, we got the signal isolator.

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Isolated Power Supply-Case Study

Step 1 :- $V_{iso-ips} > V_{BD} (= 1200V)$
 $V_{iso-ips} > 1200V$

Step 2 :- $CMTI > 47V/ns$

Step 3 :- $V_{cc} = 20V$
 $V_{EE} = -5V$ } Required voltages

Step 4 :- $P_{out} > P_{iso} + P_{gap} + P_{sw}$
 (Data sheet)
 $P_{sw} = (V_{cc} - V_{EE}) \times Q_g \times f_{sw}$
 $= (20 + 5) \times 49.2 \times 10^{-9} \times 100 \times 10^3 = 123mW$

Step 5- Select isolated power supply
 (MEJI series DC/DC converter)

So, next thing once we have the signal isolator, what we need to consider is the isolated power supply. Now, once we have the signal isolator, then isolated power supply, we can design, so in this also we have to follow different steps, so the first step remains same what is the isolation voltage for isolated power supply? Again it is similar to the previous component so it comes from the breakdown voltage. So this signal isolation, so isolation voltage isolation voltage for isolated power supply It should be more than the breakdown voltage of the device means which is equal to 1200 volts. So, V isolation should be greater than 1200 volts.

$$V_{ISO-IPS} > V_{BD} (= 1200V)$$

$$V_{ISO-IPS} > 1200V$$

Now, step 2. Similarly, we have to see what will be CMTI. CMTI, it is same as the previous component. So CMTI should be more than the maximum value of dv/dt either in ON or the OFF condition. So here we are getting this in off condition that is 47 volts per nanosecond. Okay, you can check this with respect to the device which you are going to consider and you can select suitable CMTI. Okay, now we got two components for this isolated power supply. Now step 3, it is actually same. Basically, we have to consider here, so the isolated power supply we have to consider the required voltages. So this required voltages it will be it will not be same it will be different because you know this voltage will go to the gate drive. And the gate drive will amplify the voltage level of the microcontroller based on the power supply coming from the isolated power supply. So the voltage level of this isolated power supply will come from turn on and turn off voltage levels. So this turn on and turn off voltage levels you have already seen. It is represented in terms of VCC and VEE in the previous discussions. So the VCC here it is given 20 volts and then VEE it is given minus 5 volts. So, then the required voltage which should provide by the isolated power supply, it should be 20 minus minus 5. The total voltage should be 25 volts. So, the total voltage should be 25 volts. Now, step 4, So, these are the required voltages. Now, step 4 should be what should be the power rating of the isolated power supply. We have already calculated this in the previous discussion. So, the power rating of the isolated power supply should be more than the power loss which is happening in the signal isolator, in the gate drive and in the capacitor, during the charging and discharging. So which already we have represented it in terms of isolation power loss, in the isolator power loss in the gate drivers P_{gd} and switch power loss which is required to charge and discharge the gate capacitor or the input capacitor. So, now this isolator both like power loss in the signal isolator and the gate drive that will come from the data sheet. So once we are selecting these components, you can see in the data sheet what are the power losses given with respect to each component. So in the previous slide, we have already selected signal isolator. So in the data sheet of the signal isolator, it will be given what will be the power loss. So you have to select that and you have to put it here. Now switch power loss is something what we need to calculate and you already know how we can calculate the switch power loss. Now switch power loss we can calculate it will be calculated by using the formula VCC minus VEE multiplied by QG.

$$P_{sw} = (V_{CC} - V_{EE}) \times Q_g \times f_{sw}$$

Already I have written QG with respect to this particular device that is given in nano coulomb 49.2 nano coulomb. And then this multiplied by the switching frequency. So this will give power loss. So now VCC equals to 20. This is plus 5. This is 49.2 nano coulomb and this is 100 kilohertz. So if we calculate this loss then we will be getting loss around 123 milliwatts, okay, so remaining losses can be selected from the data sheet. Once we have all the losses then we can actually find out value of P output. So the P output once we have, so based on that we can select now once we have all this value. So, the P out we have. So, the P isolation and gate

drive that we need to select and then once we have these values. So, we have 1200 volts, we have 47 volts per nanosecond and then VCC, VEE and then Pout. Once we have all this value then we can select the isolated power supply which will be suitable for this particular device gate drive. So, the step 5 is the selection. So in this case what they have selected? They have selected this series Meji series DC to DC converter for this isolated power supply and this you can actually see this series DC to DC converter. So whatever will satisfy the rating like whatever the four ratings we have selected here so that you can actually consider for your gate drive.

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Gate Drive-Case Study

Step 1 : $V_{GD} > V_{ce} - V_{EE}$
 $V_{GD} > \underline{25V}$

Step 2 : $I_{g_peak} = \frac{V_{ce} - V_{EE}}{R_g}$
 $I_{g_peak} < \frac{V_{ce} - V_{EE}}{R_{g(internal)}} = \frac{25}{4.6} = \underline{5.4A}$

Step 3 : $f_{sw} = 100kHz$

Step 4 :- $t_{pd} = \underline{100ns}$

Step 5 :- $R_{g(dr)} < R_{g(in)} (= \underline{4.6\Omega})$

Step 6 :- select suitable gate drive IC.
IXYS-IXDN-609 




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Okay, so the next thing is the gate drive. So, we have signal isolator, we have isolated power supply. Now, what we have to do? We have to select the gate drive IC. So, gate drive IC, how we can select? So, there are also different steps. So, step 1, what we have to select? The first thing in the gate drive. So, what is the voltage rating of the gate drive? It should be more than so this is coming around 25 volts. So the gate drive voltage should be more than this. Now step 2 is the peak current. So this is the another important part in the gate drive so the two main important components of the gate drive is the voltage rating and the peak current which it can provide. The peak current which it can provide that we have already seen can be calculated from this divided by R_g . Now R_g is the gate resistance. VCC minus VEE divided by R_g .

$$I_{g_peak} = \frac{V_{ce} - V_{EE}}{R_g}$$

So R_g I have already discussed in the last lecture. So R_g has three different components. So one component will come from the gate drive IC, another component will come from the device. So device will have some internal resistance. Now the third component is the external

resistance. So, in the device data set generally internal resistance of the device will be given. So, other two components will not be given. So, the another component we can actually get once we select the gate drive IC. The third component the external gate resistance that we have to connect and that depending upon the optimum operating condition we generally select that external gate resistance.

So, then we do not have this R_g value, but what we have is that we have internal gate resistance. So, this R_g if we have only internal gate resistance, this peak current should be less. So, basically if we have higher resistance, then what will happen? Then current will be less. If we have lower resistance, then the current will be more, peak current will be more.

So, if we consider only internal resistance. So, here V_{CC} minus V_{EE} and R_g internal component then the peak current which we will be getting so that will be higher than the actual value. So, the rating which we can select here is should be less than this. So this is the kind of worst condition what we can select so basically if we don't have external resistance or in gate drive there is no resistance then this will be the condition. $I_{g\text{peak}}$ is less than V_{CC} minus V_{EE} divided by $R_{g(\text{internal})}$.

$$I_{g\text{peak}} < \frac{V_{CC} - V_{EE}}{R_{g(\text{internal})}} = \frac{25}{4.6} = 5.4A$$

This will be the value of the peak gate current. So now once we have this value so we can actually select any gate drive so there the current rating will be less than this value So here if we put all these values, so then this is 25 and then this is 4.6 ohm, that is given in this particular data sheet. So then we will get the peak current as 5.4 ampere. So now we have to select gate drive IC where the peak current rating will be less than this value. This will be kind of the worst condition. Okay, now similarly in step 3, we have to assume the switching frequency which already we have assumed so that is 100 kilohertz. Now step 4, similarly we have to select the propagation delay for gate drive. So the propagation delay generally we can consider same as the previous case 1% of the switching period. So that if we consider 1% of the switching period it will be same as 100 nanosecond. Okay. Along with all this we have this step 4. Now we have to select suitable pull up or pull down resistance for the gate drive. So that pull up or pull down resistance. So for that what we have to do. So this resistance value should be selected such that that R_g gate drive so, basically resistance of the gate drive should be less than R_g internal. So R_g internal we know that is equals to 4.6 ohm. So, then R_g gate drive should be less than this 4.6 ohm the internal value.

$$R_{g(\text{dr})} < R_{g(\text{in})} (= 4.6 \Omega)$$

So, based on this we can actually select our gate drive. So, gate drive first is the voltage rating then is the peak current then We have to see the propagation delay and then the resistance of the drive IC. So, that is less than the internal resistance. So once we have all the parameter then last step is to select the suitable gate drive IC which will satisfy all the conditions. So then this

is step 6. So this is step 6. So now this is the step for select suitable gate drive IC. So in this particular device, they have selected the gate drive IC IXYS-IXDN609. So this is the gate drive IC which is satisfying all this condition for this particular device. So this is suitable for this particular device. Now we have all the main components.

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Gate Resistor-Case Study

Step 1 : Power rating $P_g = P_{sw} (= 123 \text{ mW})$

Step 2 :- Suitable gate resistor for any device (separate for turn-on & turn-off)

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Now the additional thing which we need for a gate drive design so that is the gate resistor. So what should be the value of the gate resistor? So generally what happens when we consider this gate resistance only two things we need to consider. Basically the power rating. So power rating of the resistor. So whenever we will be connecting any resistor, gate resistor externally, so then we have to consider the power rating. So this power rating of this gate resistor should come from the power loss which is going to happen. That already we have calculated equals to 123 milli-watt. So we have to see the resistance what we are selecting that is having this much power. handling capability or not then, this is the thing we need to consider for the gate resistor. Now, step 2 is that, so now we can actually consider different resistor different value of the external gate resistance and we can see the dynamic characteristics for the device under test. So then then once we have this dynamic characteristics so we can actually select suitable gate resistor for any device. But it is advisable to have two different resistor one for turn ON and another for turn OFF condition. So separate for turn ON and turn OFF. So these are the conditions it should satisfy.

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Decoupling Capacitor-Case Study

Step 1

$$C_1 = \frac{Q_g}{\Delta V_{cc}}$$

$$= \frac{49.2 \times 10^{-9}}{KV_{cc} \times V_{cc}}$$

$$= \frac{49.2 \times 10^{-9}}{0.01 \times 20}$$

$$= 0.25 \mu F$$

$$C_1 > 0.25 \mu F$$

$$C_2 = \frac{Q_g}{\Delta V_{EE}}$$

$$= \frac{49.2 \times 10^{-9}}{KV_{EE} \times |V_{EE}|}$$

$$= \frac{49.2 \times 10^{-9}}{0.01 \times 5}$$

$$= 0.98 \mu F$$

$$C_2 > 0.98 \mu F$$

+

Step 2 Select capacitors (TOK ceramic capacitors)



Now the last component which we need to consider is the decoupling capacitor. So already you know the decoupling capacitor why we need. So then if we have to select the value of the decoupling capacitor. So then what we have to do. So we have to see. So basically we have to select the capacitance value. So the capacitance value, so there are two different capacitances are there. C_1 and C_2 that already I have discussed. So it will come from gate charge divided by ΔV_{CC1} with respect to the positive voltage and if we have negative voltage then another will come from the negative voltage. C_1 is equal to Q_g divided by ΔV_{CC} .

$$C_1 = \frac{Q_g}{\Delta V_{cc}}$$

C_2 is equal to Q_g ΔV_{EE} .

$$C_2 = \frac{Q_g}{\Delta V_{EE}}$$

So if we have two different sources then two different decoupling capacitors will be connecting. So ΔV_{EE} . So now this Q_g already you know. So that is 49.2 nanocoulomb. And ΔV_{CC} it is always advisable to have 1%. So generally what we have? We have KV_{CC} multiplied by V_{CC} . So then KV_{CC} we can consider as 1% of the V_{CC} . Similarly here also, we can consider KV_{EE} as 1% of the V_{EE} . So, then once we have this value, here it is, so basically we have negative voltage here so we can consider only the magnitude. So then we can get the values as, so we have to select these capacitances which should be more than these values. So C_1 should be more than 0.25 microfarad and C_2 should be more than 0.98 microfarad. So these are the values we need to consider in case of decoupling capacitor. So then so this step let's say this is the calculation of capacitor step one, then step two we can once

we are we have with the calculated values based on this then we can select the required capacitor. So then select. So generally ceramic type of capacitors are considered like SMD type of ceramic capacitors are considered for this. So for this particular driver design TDK ceramic capacitor are considered. Okay, so now you have all the parameters, right? So now you have all the parameters, you know the how to design the gate drive. So once you have the gate drive, then dynamic characterization will be possible. So the five components are required and five components are very important. Important for all this so this is the reference so you can see this like all this design from this particular reference. So you can actually see the signal isolator. It is basically known as the steering wheel. Then the isolated power supply it work as the gas tank. If we consider any like car so this work as gas tank or the petrol tank and then gate drive work as the main engine and then your gate resistor, it is actually providing the gas pedal and then decoupling capacitor, it is kind of providing as the fuel injector. So, this is the five different components if you try to relate it with the car. So, this is how these five components are related to the gate driver. So, basically driving means like we can consider a suppose it is like kind of car. So, which is probably driving. So, this is how these five components are related and this is how their work should be. So, if you try to consider with respect to any car. Okay, thank you. So, this is all for today.