

Power Electronics with Wide Bandgap Devices
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Lecture-4
Junction Capacitance characterization of Power Devices

JUNCTION CAPACITANCE CHARACTERIZATION OF POWER DEVICES

Welcome to the course on power electronics with wide band gap devices. Today I am going to discuss about junction capacitance characterization of the power devices. So, when I say junction capacitance, what do you understand by junction capacitance?

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Junction Capacitance

- ❖ Parasitic capacitances form between any two terminals at the die level and in the packaging of the power device.
- ❖ At the die level, capacitances partly represent charge separation creating the depletion region that blocks voltage and later recombines.
- ❖ The capacitance depends on the device's geometry and material properties and may also include additional capacitances from metallizations.
- ❖ Physical structure understanding helps, as it has an impact on these characteristics.



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So, it is basically the capacitance which is present in the device which we are not adding from the outside. So, how this capacitances are coming? So, basically as you can see here written in this slide. So, this parasitic capacitances it actually forms between two terminals at the die level and in the packaging of the power devices. So, basically it is coming from both die level and from the packaging of the power devices. So at die level these capacitances are partly represent charge separation which is creating the depletion region that blocks the voltage and later recombines. So, basically it is present inherently in the device. So, this we are not adding or there is no other reason to form these capacitances. So,

this capacitance creates the depletion region Later actually it recombines So, then this capacitance depends on the device's geometry If the size of the devices increases, voltage level, current level anything changes obviously then this capacitance values will also change and this also include additional capacitances from the metallization.

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Nonlinearity of Capacitance

- ❖ The capacitance representing charge separation is highly nonlinear with respect to voltage.
- ❖ Nonlinearity depends significantly on the geometry and material properties of the device.
- ❖ Example: In a Super Junction MOSFET, capacitance between drain and source changes significantly over the rated voltage range.
- ❖ In comparison, other devices show only slight changes over the rated voltage range.

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This physical understanding of these capacitances will help to impact on the characteristics of the device So, now these capacitances are basically non-linear in nature. So, that is why it is very much important to understand characteristics of these different capacitances So, now this capacitance represent charge separation is highly non-linear with respect to the voltage level That means what? If the voltage level of any particular device So, let us say any device is rated for 1000 volts so if the voltage rating of the device changes with respect to the operation so initially let's say for some loading condition the voltage is 100 volts and for some loading condition this voltage change to 500 volts or some loading condition it changed to 900 volts so the then the this capacitance values will also change And additionally, if the rating of the device changes, so let's say one device which is rated for 100 volts, another device which is rated for 900 volts, then also these capacitance values and their characteristics with respect to different voltage level will change. So, this gives us non-linear type of characteristics. This non-linearity significantly also depends geometry and the material properties Means if we are considering silicon device then the material property will be different than that of the silicon carbide or the Gallium nitride device And also the size, so what is the geometry of any particular device So that gives us different types of capacitance, different value of capacitance So, for an example, in a super

junction MOSFET the capacitance between drain and source changes significantly over the rated voltage change.

In comparison to other devices, so only slight changes over the rated voltage change. So, that is why you can see here, so see super junction MOSFET it is having different type of capacitance characteristics as compared to the other device. So, that is why we need to learn about these capacitances. what are these different capacitances, how this is coming, how we can actually measure this capacitance with respect to the voltage level and what will be the effect of this capacitance in the device operation. So, these are the different factors we need to know.

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Understanding C_{oss}

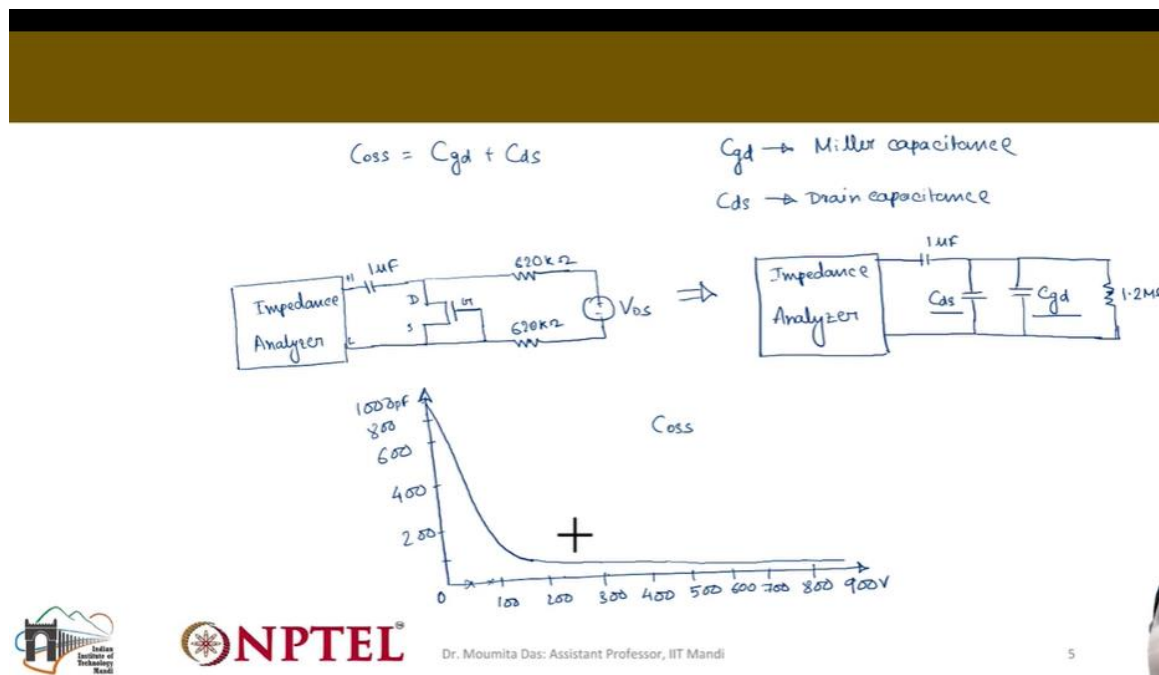
- ❖ C_{oss} is defined as the sum of the capacitance between drain-source (C_{ds}) and gate-drain (C_{gd}).
- ❖ This parameter is crucial in understanding power device performance and behavior.
- ❖ C_{oss} helps in determining the dynamic switching characteristics of the device.
- ❖ The knowledge of C_{oss} is essential for accurate simulation and characterization.

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So, that is why today we will learn about these different capacitances. So, the first thing In these capacitances, so in the data sheet I have already told you So there are three different capacitances One you probably know as the output capacitance So this is what is shown here C_{oss} Which is known as output capacitor So this C_{oss} is basically summation of two different capacitances Which is known as C_{ds} or drain to source capacitance plus C_{gd} which is gate to drain capacitance. So, these two capacitances combines to give this C_{oss} . In data sheet you can get this value of C_{oss} which will have two different capacitance characteristics. So, this Parameter is very important to understanding behavior of the device and the performance of the device.

This helps to determine the dynamic switching characteristics of the device. That is why this knowledge of the C_{oss} is very essential for simulation and characterization. So, now another capacitance which is very important. So, that I will tell you later that is C_{iss} . So, here I will just tell you little bit more about this C_{oss} .

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So, C_{oss} as I told you C_{gd} plus C_{ds} ok.

$$C_{oss} = C_{gd} + C_{ds}$$

So, now There are two different capacitance. Now, in this two capacitance C_{gd} is gate to drain and C_{ds} is drain to source. This capacitance is basically known as drain capacitance. And what is this capacitance? This is known as Miller capacitance.

Now, how to find out this capacitance? So, in order to find out any capacitance, there are two equipment which we can use, any of the two equipments. One is impedance analyzer or another is parametric curve tracer. So, any of the two equipments will be useful to find out these capacitances. Now, since this is having two capacitances which is having drain common, so you can see So, in order to find this capacitance what we need to do? We need to short gate and source terminal and how that is possible? So, if this any device is connected to impedance analyzer. So, which is having high side and low side.

So, then what will happen? This impedance analyzer will be connected to the device let's say drain and low side will be connected to the source terminal of the device. And as I told you this in order to find out this output capacitance we need to short gate and source terminal. So, gate terminal will be shorted here. So, you can see here, so this is drain, this is source and this is gate terminal. So, another important thing here is that in order to find out these different capacitances, we have to connect one input capacitance which is of 0.

1 microfarad. And in this path, there will be one resistance which will be connected 620 kilo ohm and which will be connected to drain to source voltage. And similarly, another resistance will be connected in this path which will be having similar value as 620 kilo ohm. So, this is VDS. So, now if I try to find out equivalent impedance in this particular network, so then this network will look like this is having impedance analyzer, then this is having 0.1 micro, sorry, this is not 0.

1, this is 1 microfarad. This is 1 microfarad. Similarly, here it will be having the value of 1 microfarad. Then this will be connected to two different capacitances in parallel which you already know C_{gd} and C_{ds} which will be connected to the resistance of 1.

2 mega ohm. Because this 620, 620 kilo ohm resistance will add up and this will give 1.2 mega ohm total. So, now in impedance analyzer we will get to see the output capacitance which is having two input, two parasitic capacitances, not input, parasitic capacitances C_{ds} and C_{gd} . So, how the characteristics looks like? So, for any particular device, so different devices having different output capacitance values. So, if we try to draw the characteristics of any particular device so let's say for one silicon carbide device if i try to draw this characteristics which is having rating let's say 0 to 900 volts maximum rating is 900 volts and which is having let's say 100, 200 like this division is there 20, 300 like this so it will go 400, 500 600, 700, 800, 900 now this let's say having maximum value of this parasitic capacitance as 1000 pico farad now again it will be divided in let's say 800 then 600 then 400 then 200 like this it will be divided.

So, now when I try to draw the capacitance, so initially this output capacitance will start from very high value, let us say from 1000 picofarad and it will go to minimum value when the drain to source voltage reaches to certain level and it will remain close to minimum value throughout the voltage level. Now, for any device these characteristics looks little bit about like this so basically characteristics the maximum value of the output capacitance will change for different device so that comes from the material properties and also from the size dimension of the device but the characteristics will look like this So, initially very high value of parasitic capacitance, parasitic output capacitance will come into picture. So, if the device is operating somewhere here or here. So, the output capacitance will be very

high and when the device will reach to certain voltage level. So, after that it will reach to minimum capacitance value and this minimum capacitance value will remain throughout the voltage range.

So, if we are using this particular device, we have to ensure that we are using this device for a voltage level which will give us this minimum capacitance. So, this curve will give us the actual behavior of this capacitor which will not be able to find out from any particular value. So, in the data sheet, I told you different value like single value of these different capacitances. Obviously, by changing the voltage level, these values will remain, we consider it will remain constant, but this is not constant as you can see from this particular characteristics. So, that is why this characteristics is very important.

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Understanding C_{iss}

- ❖ C_{iss} is defined as the sum of the capacitance between gate-source (C_{gs}) and gate-drain (C_{gd}).
- ❖ C_{iss} impacts the input characteristics of the power device significantly.
- ❖ Knowledge of C_{iss} is critical for designing gate driver circuits and other related components.
- ❖ Accurate characterization of C_{iss} helps in optimizing device performance in various applications.

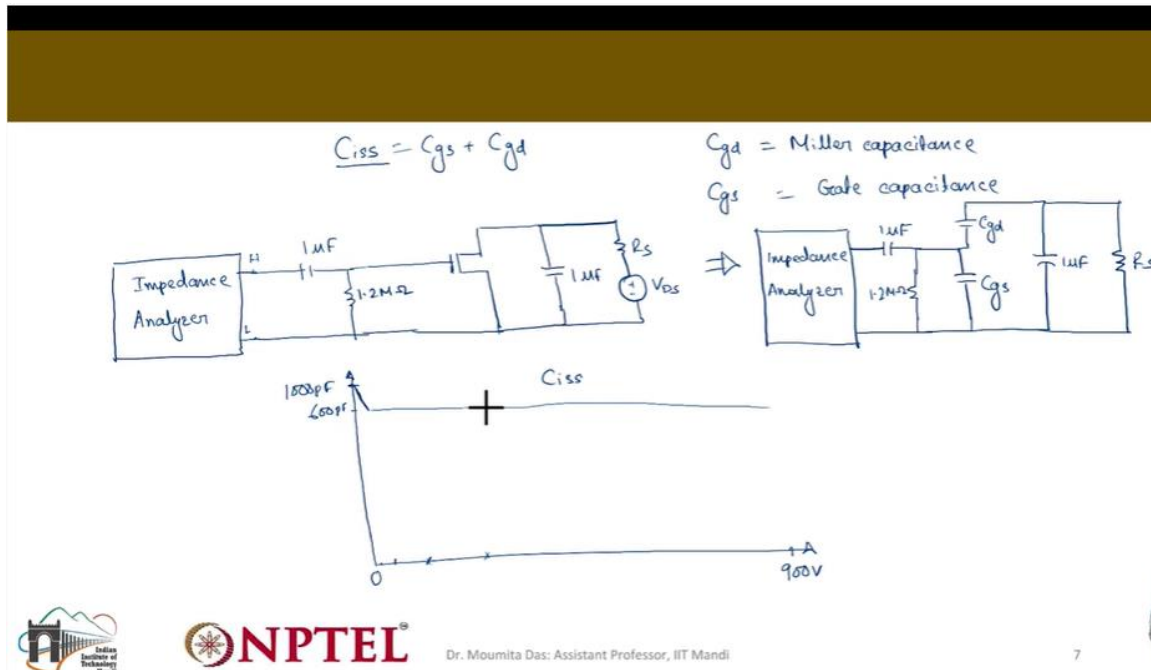
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Now coming to the input capacitance. Similar to output capacitance, this input capacitance is also having two different components as you can see gate to source and gate to drain component. So, basically this C_{iss} is summation of C_{gs} which is gate to source capacitance and C_{gd} which is gate to drain capacitance. This C_{iss} basically impacts the input characteristics of the power devices. So, this knowledge of this C_{iss} is very important for designing the gate driver.

So, this gate driver when we will be discussing in detail. So, then I will be telling you more about how this capacitance are related to design of the gate driver. So, at this moment I will be telling about how we can get this Ciss. So, this accurate characterization of the Ciss helps in optimizing the device performance in various applications. So, similar to the previous case, so Ciss as you know, so basically it is combination of Cgs plus Cgd.

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$$C_{iss} = C_{gs} + C_{gd}$$

Now, you already know C_{gd} , it is basically known as Miller capacitance as I told you in the previous slide. and C_{gs} it is known as gate capacitance. So, in order to find out this input capacitance what we have to do? We have to actually short this drain and source terminal. How we can short this drain and source terminal? So, the device will be connected to impedance analyzer similar to the previous case. So, it is having high and low point and similar to the previous case there will be one capacitance which is of 1 micro farad will be connected here and then there will be one high value of resistance equivalent to the previous case which is 1.

2 mega ohm will be connected here in parallel now this will be connected to the device gate so now device drain will be connected so gate will be connected here and then source will be connected here now drain basically will be connected to 1 microfarad capacitance,

which will be connected to 1 resistance R_s and that will be connected to VDS. Diagram with respect to different impedances will look like, which will be having similar capacitance as the previous case 1 microfarad. Then there will be this resistance which is connected. So, 1.2 mega ohm and then this will be connect this is having the value having the capacitance C_{gs} .

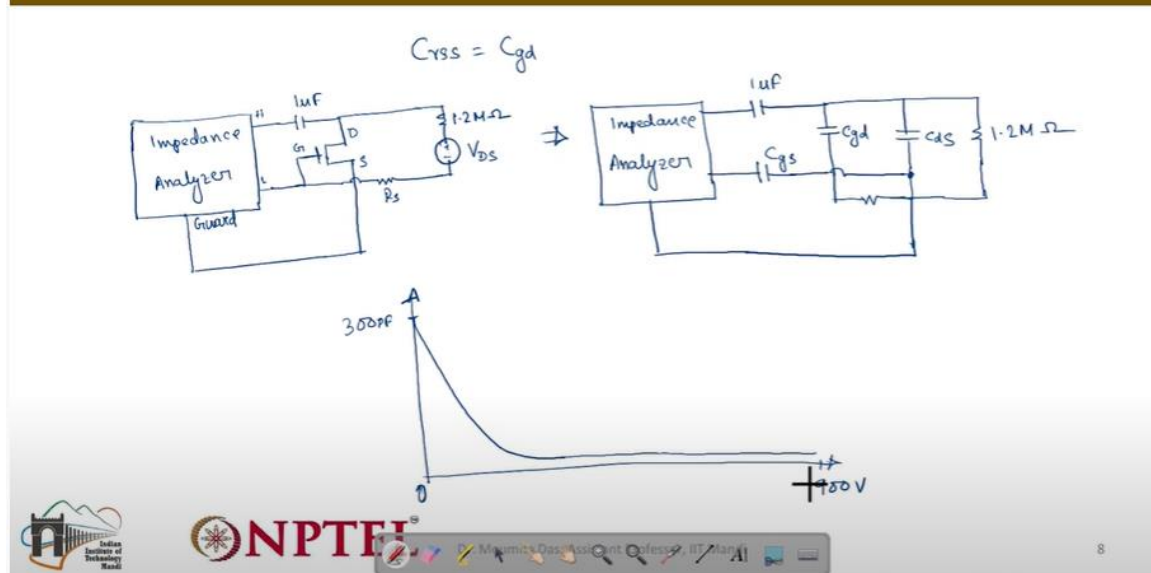
This is having capacitance of C_{gd} and this is connected to the capacitance 1 microfarad and this is connected to R_s . So, this is the equivalent diagram to get the characteristics for input capacitance. Now, how this characteristics looks like? So, if I take the similar device as the previous case to find out the characteristics of the input capacitance. So, in impedance analyzer what we will get? We will get this C_{iss} . So, how this characteristics looks like? So, similar to the previous case if I take the voltage level from 0 to 900 volts.

volts and the capacitances input capacitances in pico farad let's say it is having maximum value of 1000 pico farad so 0 to 1000 pico farad so then what will happen the input capacitance will be it will slightly decrease as the voltage will increase then it will settle down to the steady state voltage level. So, as you can see here if the maximum value is 1000 picofarad, so then by decreasing this value it will be either 600 or 700 picofarad, let us say 600 picofarad. So, from here you can understand that this C_{iss} is having quite significant value. and this is playing very important role for turning on and turning off of the device because you know it is having it is input capacitance in order to turn on or turn off the device gate it is coming in the gate so gate will either charge or discharge so it is not having minimum value so that means like significant charge and discharge will be there in this capacitance and it will give a significant rise and fall time so that is why this characteristics is very important so as i told you in the previous case so if we are very close to zero then this capacitance value will be very high And after some point, when we are reaching some voltage level, then this capacitance will settle down to the steady state value. So, this, then we can use this steady state value to actually design our gate drive.

But we have to always keep in mind that drain to source voltage is actually beyond this minimum capacitance value. Means we are either operating here, here, so that this capacitance is reaching to steady state value. So, this is very important for designing gate drive as I told you in the previous slide. Now, these are the two different capacitances with respect to input and output.

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Understanding C_{rss}



Now, there is another capacitance, the reverse capacitance. So, what is this reverse capacitance? So, it is actually having only one capacitance which you know as Miller capacitance. So, in order to find this capacitance value, what we have to do? We have to keep this source in the floating condition. And how that is possible?

So, in impedance analyzer, if I try to draw the equivalent network, so similar to the previous case, so this device will be connected to the impedance analyzer. Now this high point will be there and the low point will be there. Now this device again will be having 1 microfarad capacitance at the input.

Then the device drain will be connected and then gate. This gate will be connected to the lower terminal. and as I told you source will be in floating condition. So, there will be one point where this can be connected to the Guard of the impedance analyzer. So, there this source point will be connected.

So, in the previous two cases you have seen either we are shorting gate to drain or probably we are basically shorting drain to source. So, different two terminals we are shorting, but in this case we are not shorting any two terminal because it is having only one capacitance. So, that is why we are keeping the other one, so like source terminal in the floating condition. So, that is why this characteristics is going to be bit different. So, then this will be connected to the output through one resistance and it is having VDS connected to VDS.

So, this is the source terminal, this is the gate terminal. Now, how the equivalent diagram will look like? So, this let us say this is R_s . So, the equivalent diagram it will be having

similar type of diagram. So, input will be having impedance analyzer. This will be connected to 1 microfarad capacitor.

Now this is connected to, so there are three different capacitances will be coming. So gate to drain capacitance, so gate to drain capacitance it will be connected to and then there will be another drain to source capacitance. And now this gate to drain capacitance and drain to source capacitance will be having resistance in between. And this source terminal will be connected to the guard.

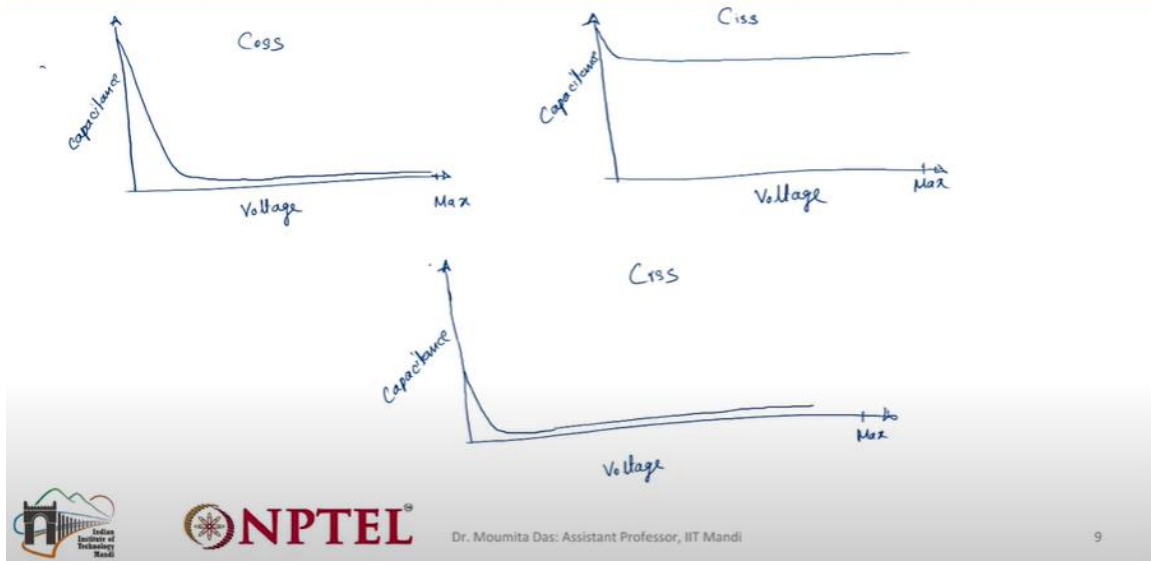
and here it will be having 1.2 mega ohm and now this is having this is the value C_{gd} , C_{ds} . So, now this is having the value of C_{gs} . So, this is how the equivalent diagram will look like. So, ultimately it will give us the value of C_{gd} . So, this is how the equivalent diagram will look like for this reverse capacitance. So, how the characteristics looks like for this reverse capacitance? So, if I try to keep similar the characteristics for the similar device means it is having the voltage level 0 to 900 volts.

So, now this reverse capacitance it is having only one capacitance. So, the value of this capacitance will be much lower. Means it will be starting from let's say maximum of 300 volts.

Not 300 volts, 300 picofarad. So, 300 picofarad. So, eventually with respect to the voltage level this will also reduce and then remain to the minimum level. So the input, so initial value of this reverse capacitance is lower than that of the output capacitance but the characteristics will remain similar to that of the output capacitance. So these are the three different capacitances which you get to see in the data sheet and this actually you need in order to understand the basically different parasitic capacitances of the device.

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Characteristics



so now you know different characteristics so you can so if i try to draw different characteristics here so you can see here with respect to C_{oss} so voltage level will be minimum to maximum this is pico farad so voltage level here it will be maximum so then it will go to minimum level like this then C_{iss} so it will be having the maximum voltage here so this is in this side voltage and then this side it will be having capacitance similarly voltage and capacitance is maximum and this will be having like it will reduce little bit from the initial value, but it will try to settle down to some significant value. Now, C_{rss} which is having only one component of the capacitance that is Miller capacitance.

So, the maximum voltage this is capacitance Now it will also reduce. So this is having comparatively lower value. So maybe I can start from the lower point. So in order to keep the scale in the similar level. So it is having much more lower value and then it will reduce to minimum value.

Same as the C_{oss} . So, these are the three different capacitances which we need from the device characterization.

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Impact on Device Selection

- ❖ Capacitance characteristics are invaluable for selecting appropriate devices for specific applications.
- ❖ These characteristics ensure that the device meets the necessary performance criteria under different operating conditions.
- ❖ Designers can better match devices to their intended applications by understanding these parameters.
- ❖ Selection impacts both the efficiency and reliability of the final application.



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So, now how these capacitances are going to impact? So, basically these capacitance characteristics are invaluable for selecting appropriate device for specific applications. Specific applications will have specific frequency and then also we have to probably limit the value of the capacitance for certain application. May be some devices with respect to the material let us say silicon and silicon carbide and GaN, they all are available similar voltage level. So, for particular application probably we have to limit this parasitic capacitances, then we have to choose the devices which is having lower value of this parasitic capacitances.

So, that is why this specific application is very important for this. Now, these characteristics ensure device meets necessary performance criteria under different operating conditions. so designer can also better match these devices to their application and by understanding different parameters so this selection will impact both efficiency and the reliability for any applications.

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Simulation Model Accuracy

* suitable switching & driving losses

- ❖ Knowledge of junction capacitances is crucial for developing accurate simulation models.
- ❖ Accurate models lead to better predictions of device behavior under various conditions.
- ❖ Improved simulation models enhance the design process, saving time and resources.
- ❖ It ensures that the final product meets the desired specifications and performance criteria.



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Now there are actually various advantages we will have if we try to characterize these different devices. Now what are the different advantages? So basically these are these capacitances first thing is the required for suitable. So the first point is the suitable switching and driving devices.

And driving operation. So, in order to find out suitable switching order driving losses, we need these capacitance values. So, this is the first advantage for characterizing these capacitances. Second is the simulation model accuracy. So, simulation model accuracy means, so if we are modeling any device, if we do not have information of these capacitances or the behavior of the capacitances we cannot model the device properly and if we can't model the device properly then the simulation also will not be possible properly so that is why this knowledge of the junction sorry capacitance is very important in order to develop accurate simulation model. So, this accurate model will give us better prediction of the device behavior under various operating condition.

So, this improved simulation model enhance the design process, save the time and the resources. It ensures the final product meet the desired specification and the performance criteria. So, that is why This is very important to model any particular device for the simulation purpose or for getting the actual behavior characteristics from the model of the device.

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Dynamic Characterization Data

- ❖ Junction capacitance characteristics are vital for interpreting dynamic characterization data.
- ❖ They help in understanding the transient behavior of devices under real operating conditions.
- ❖ Accurate characterization leads to better insights and more reliable data interpretation.
- ❖ This understanding is crucial for improving device performance and reliability in practical applications.



And the important point is that last or the important very important point is that dynamic characterization of the device. So, dynamic characterization of the device will be possible by knowing this characteristics.

parasitic capacitances. So, this junction capacitance is very important for getting dynamic characterization data. They help understanding the transient behavior of the device. As I told you, so this input capacitance generally comes into picture during turning on and turning off condition. So, the turning on and the turning off condition of the device is having the information of the dynamic operation. So, this is very, this time is very crucial for any device and this gives us the transient behavior of the device.

So, until and unless we have actual information of this capacitances, we cannot characterize the device for dynamic time. So, accurate characterization leads to better insight and more reliable data interpretation. So, this understanding is very critical for improving device performance reliability for practical operation. So, there are three major advantages for characterizing these parasitic capacitances.

One is to find out the losses during the switching or driving. Second is the modeling of the device. Third is the getting dynamic characterization for device operation. So, these three factors we will get after characterizing these parasitic capacitances. So, this is the reference which you can refer for this particular lecture. Thank you.