Power Electronics with Wide Bandgap Devices
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Lecture-30
Power Density

Welcome to the course on power electronics with wide band gap devices. Today I am going to discuss about the power density considering the wide band gap devices. I need to tell you what is the power density. So what generally we consider when we say power density because you know like in the entire course sometime probably I have mentioned that whenever we consider this wide band gap devices the power density of the system it will be higher. And that is desirable for any power electronic system. So, that is why I mean people are going towards this wide band gap devices so that they can go for high power density system.

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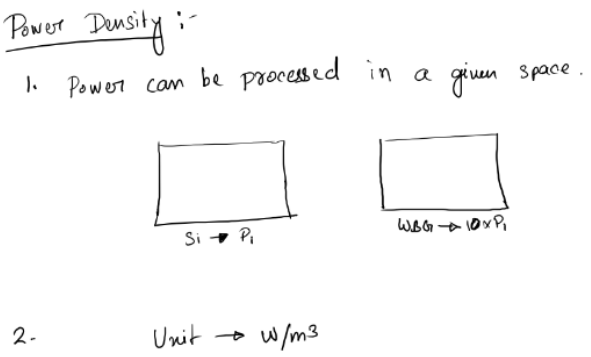

So, let us see what is power density. So definition of power density. So definition of the power density when I say so that time so that power how much power is processed in given space. So that is known as the power density.

If power process that measurement is less in a given space then we can say low power

density and if it is more in a given space then we can say high power density system. So, basically the definition for this is that power can be processed in a given space so generally what happens for silicon devices you know like considering low frequency operation we need the component which is having higher value component means the inductor capacitor and heat sink for the silicon based system so then The same space like if we consider for silicon so like amount of power it will be processed for silicon based system. So power P1 let's say it is processed in this particular space. And for this wide band gap devices this can be processed in the same space 10 times P1. this is just an example.

So, then what will happen? If in silicon P1 power is processed and in wide band gap devices it is 10 times P1 is processed in that space, then we can say this is high power density system and that is what is desirable, right. Now, unit of this is that watt per meter cube. watt per meter cube so meter cube tells like the space where one watt power is processed this is this can be also expressed in terms of watt per inch cube or watt per centimeter cube so whatever inch meter or centimeter that gives dimension of the particular space and what is obviously the unit of the power so like if it is like high power density system so maybe it can go towards kilowatt in that kind of level okay so this is known as the power density and as you know like now everything is going towards like compact kind of system, the size of the system is reducing. So, then power electronic converter size should also reduce. So, then if we want to reduce the size, we have to process high power in a smaller space, right.

So, then we have to go for high power density system. So, as we are going to use wide band gap devices in future power electronic system, then this can be easily achieved using wide band gap devices. But there are problems or challenges which we need to face if we go for high power density system.

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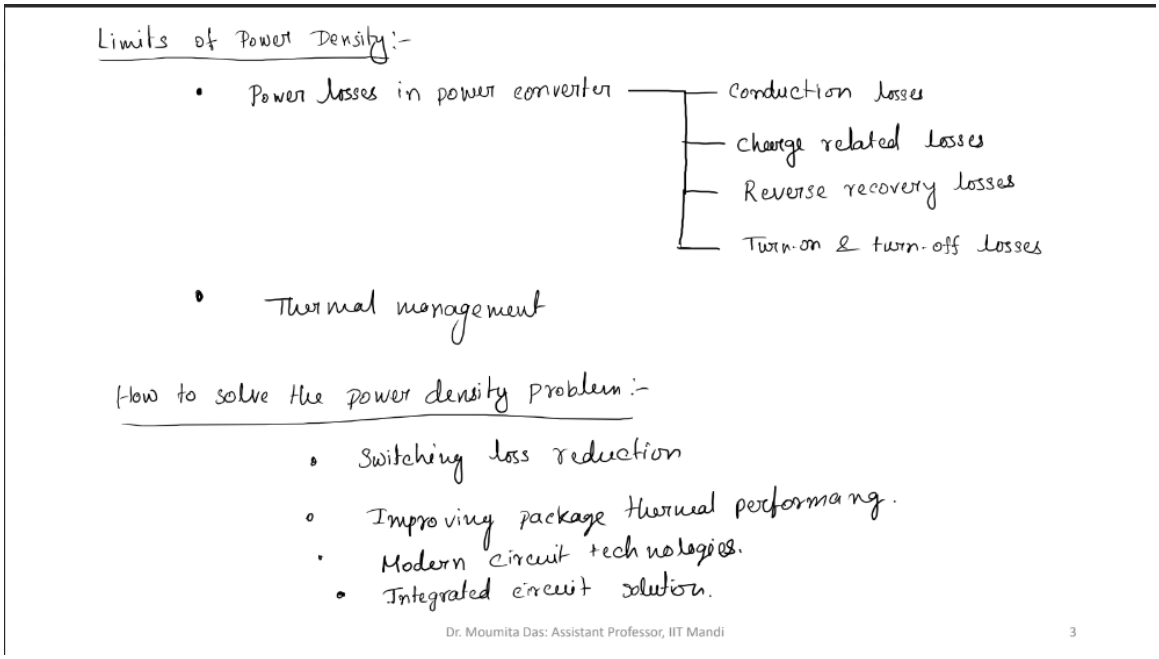

Okay, so then what limits the power density? First we have to know that see in silicon also we can go for high power density system. But there must be some limitation of silicon based devices which doesn't allow us to go for high power density system.

Now for wide band gap devices with this limitation can be solved. Let's see what are these limits. Limits of So, what limits the power density? So, basically there are different limiting factor of this power density operation. So, one is that power losses. So this power losses in the power converter which happens this comes in the way of achieving high power density system.

Now what are these losses? So these losses can be classified conduction, charge related losses, Reverse recovery losses Turn on and turn off losses okay right so these are the different losses which causes this power density problem okay now what are the other problems so this losses will generate heat in the system in order to reduce that heat we need to use heat sink or we have to use method or maybe like we can increase the size of the system so that I mean like the surface of the size surface of that particular system will be much wider so that it can dissipate heat easily so the heat generation in the system will be less and you know the problem of thermal related issues. So if heat generation is more obviously the property of the devices will change and again it will generate more heat and eventually system breakdown will happen. So that is why we have to manage this losses generated heat properly so that it will not affect the system. And then second thing is the thermal management. This is also related to the losses basically we have to manage all the heat generated in the system by using proper method and that causes increase in the size of the system.

So, in order to reduce the problem probably the first thing we should be considering is the reduction in all the losses or probably better thermal management of the system or combination of both. Now how to break through this problem? So how to solve this problem? as you know like switching loss we can probably reduce reduction second is that improving package thermal performance, modern circuit technologies using wide band gap devices. All this I will discuss in details. and then go towards integrated kind of solution, integrated circuit solution. So these are the problems and this is how we can solve.

So let's see how this power density is trending starting from the beginning. Means when this semiconductor devices first came and then power electronic system developed due to that. From that time to now where we are exactly in the power density point of view.

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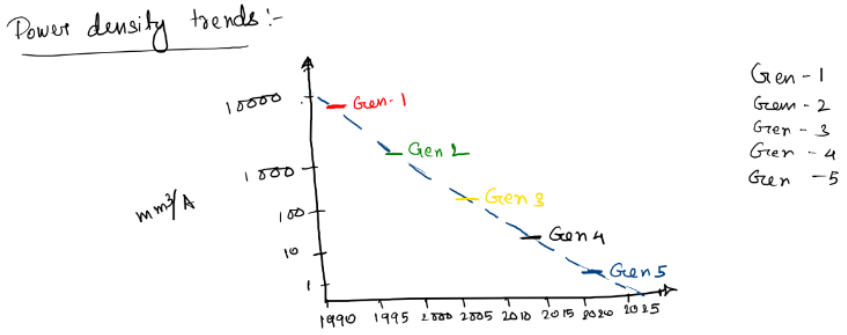

So, if you see power density trends means how basically this system size changed, right. So, system size if I write down, so starting from 1, so this scale will be like different scale you can just consider, log scale you can consider 1000, then it is 10000.

So, this is millimeter cube per ampere. Okay, so this is the magnitude in this y-axis and the x-axis gives the year starting from 1990, then 1995, 2000, then 2005. 2010 2015 2020 right now we are in 2025 now it is to 24 is ending so we are in 2025 and then it will go further 2030 right so now this curve looks like so basically it is going from 10,000 so if I draw a dotted line so then it will look like Something like this. Okay. So now in this so if we so just let me draw it Okay, so now We are starting from 1990.

So, there are like different generation semiconductor devices like we started using from 1990 right now 2025. So, then we can write down the semiconductor devices with respect to generation 1, generation 2, generation 3, generation 4. four generation five okay now let me just use different color so here this line is with respect to generation one now this is the first semiconductor device when started using then modified device when it arised so then what happens so then we are in generation two Right, now after that there is like here around generation 3, now generation 4, and then we are going towards generation 5 here okay so this is how this power density trend is now recently we are using generation 5 semiconductor device and that allow us to have very small size 1 mm cube per ampere. Earlier it was close to 10,000 mm cube per ampere. So that much space is used for that much current process.

Okay. So 1 ampere current is processed in 10,000 mm cube space. And now here it is 1 ampere current in 1 mm cube space. So this is how this power density trend is evolving ok now probably in future it will be further less so that is that prediction only we have until and unless there is like proof we cannot comment on it but trend is going towards it ok now this let's see how we can actually analyze this different power density limits ok.

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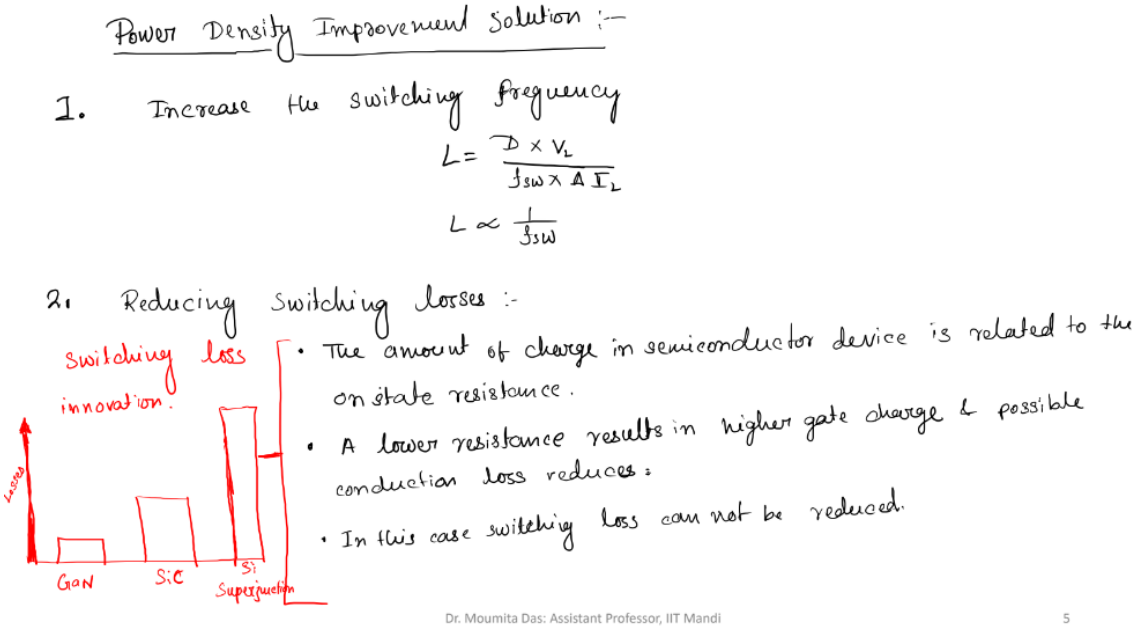

So, if we have to consider power density improvement solution if we have to provide so then how that can be provided. So, let us see the power density So first thing, so there are point wise, let us see how it can be done, 0.

1 is that increase the switching frequency. So this is the first step can be taken. So if we increase the switching frequency then what will happen? Passive component size will

reduced out. So passive component among passive component which one is directly related to the frequency? That is magnetics or the inductor. If the system is isolated if there is a transformer so then it will consider the transformer.

So, then inductor how it is related?

$$L = \frac{D \times V_L}{F_{sw} \times \Delta I_L}$$

L equals to duty cycle of that particular converter multiplied by voltage across the inductor divided by switching frequency multiplied by the current ripple of the inductor. So, this is the basic formula which you can refer in any power electronics book you can get it very easily. So, basically VL equals to L di/dt. So, from there this can be derived. So, now you can see here.

So, this L it is basically inversely proportional to the switching frequency. So, if switching frequency increases, then the L size will reduce down. If L reduces, then what will happen? The requirement of magnetic size will reduce down and that will increase the power density of the system, ok. This is one of the ways. Now, second thing what we can do? Second thing we can consider is the reduce, by reducing the switching losses.

So, this switching losses if we can reduce down then what will happen? Heat generation will be less. heat generation is less then the heat sink requirement will reduce down and if heat sink requirement is less then it will improve the power density of the system so now there are different losses you know that turn on and turn off losses conduction losses charge related losses all these different parameters are there if there is a possibility to reduce down that we can do one of the ways is that the amount of charge in semiconductor device is related to the on state resistance. Now, somehow if we can reduce this on state resistance then that can be reduced down. So, a lower resistance results in higher gate charge. Right and possible capacitances or possible conduction loss can be reduced.

Loss reduces okay and then switching losses can also be reduced down but there is a problem so basically loss due to conduction can be reduced down but in this case switching loss cannot be ok so in the previous basically if it is possible to reduce the on state resistance then what will happen then the loss in the switches due to conduction can be reduced down Now switching loss if we consider like higher gate charge then the switching loss cannot be reduced down. If resistance reduces then conduction loss will reduce but the charge related loss will increase. And charge related loss if it is increasing then the

switching loss will increase. Then reduction in the switching loss is not possible but conduction loss in the switch is possible in this way. So, then what we have to do? We have to consider reduction in charge related losses.

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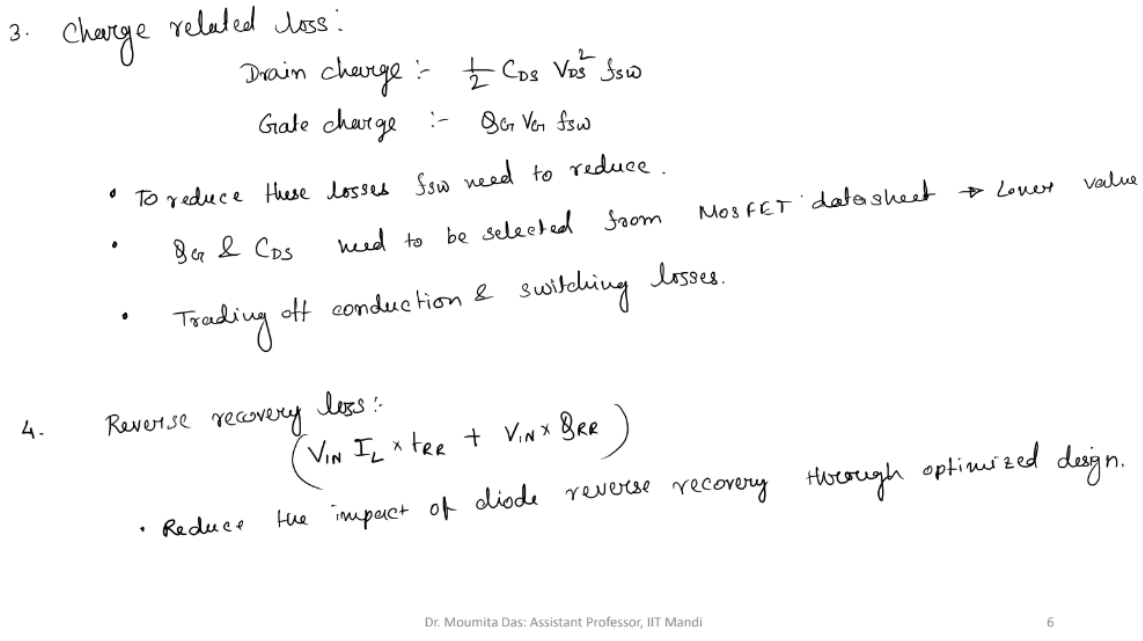

so what do you understand by charge related loss so charge when i am saying so basically it is related to some capacitance so how this charge related loss comes so basically drain charge if i write down charge in charge related losses so then that can be write down as So,

$$\frac{1}{2} C_{DS} V_{DS}^2 f_s$$

whatever voltage is appearing across drain to source in the devices. So, this is with respect to the MOSFET. In IGBT, it will be like with respect to collector to emitter. okay so collected to emitter the capacitance and then with respect to the voltage across it and then that multiplied by the switching frequency so this Cds if it is increasing then the charge related loss will increase so this is with respect to the drain charge so there are actually two different charge related losses one is with respect to drain charge another with respect to gate charge for mosfet So that is equal to

$$Q_G V_G f_s$$

VG is the voltage which is coming across the gate to source and QG is the charge required for that. gate to source basically the capacitor switch is connected at the input of the device which is known as the gate capacitance okay in order to reduce the losses we have to consider this parameter which is less in the devices so then what we need to do to reduce this losses this charge related basically losses drain charge and gate charge related losses Primarily this QG, primarily the switching frequency need to reduce down. Now if we reduce this switching frequency then that will increase the passive component size. So this is not desirable. So there are actually two components input voltage, output voltage and the gate voltage they are fixed.

So other things are the gate charges or CDS and the switching frequency. Switching frequency we can reduce down but that is not possible for high power density system because we are going for high frequency operation. Now then remains QG and CDS need to be selected from MOSFET data sheet. which will be of lower value.

So this we need to check. That will help us in improving charge related problem or loss problem. There are actually two things. Either we can reduce the conduction losses or we can reduce the switching losses. Both cannot be reduced at the same time. So then what we need to do? We have to optimize these values.

Trading off means if we optimize we have to see like which parameter is causing more losses if charge related loss is more with respect to the on state resistance loss then probably we have to go for the this QG and CDS with lower value if on state resistance related loss is more that is the conduction loss then we have to consider lower resistance so that we can reduce the conduction losses so that is why this trade-off between the switching loss and conduction loss we have to do so that we can select like which parameter we want to optimize right so accordingly we can reduce the losses right fourth is the reverse recovery losses so the reverse recovery loss how we can analyse So, basically this can be analyzed as the input voltage multiplied by the inductor current multiplied by the reverse recovery time of the diode plus input voltage multiplied by reverse recovery charge of the capacitor. So, these parameters tell us how much will be the reverse recovery loss in particular system, particular converter if the diode is conducting. If the diode is not conducting then we do not have to consider this reverse recovery loss. But most of the cases what happens forward and the reverse operation is there. So, that is why the diode will come into picture even if there is no diode corrected separately.

But let's say boost converter or buck converter, they have diode connected separately. Then we have to consider this reverse recovery loss also, how much it is going to be. There is no switching frequency parameter. So, that is one thing we can see in this particular expression. So, switching frequency will not come into picture in this, but like the reverse

recovery time and the reverse recovery charge that will come from the selection of the particular device, right.

And device will be selected according to the switching frequency. So, that I mean like all the parameters related to the device will not have effect in that switching frequency. So, accordingly we can select the device and from there we can check what will be the reverse recovery time and the reverse recovery charge and then we can calculate the reverse recovery loss. So, then this reduce the impact of diode reverse recovery through optimized design. Now this is with respect to reverse recovery losses.

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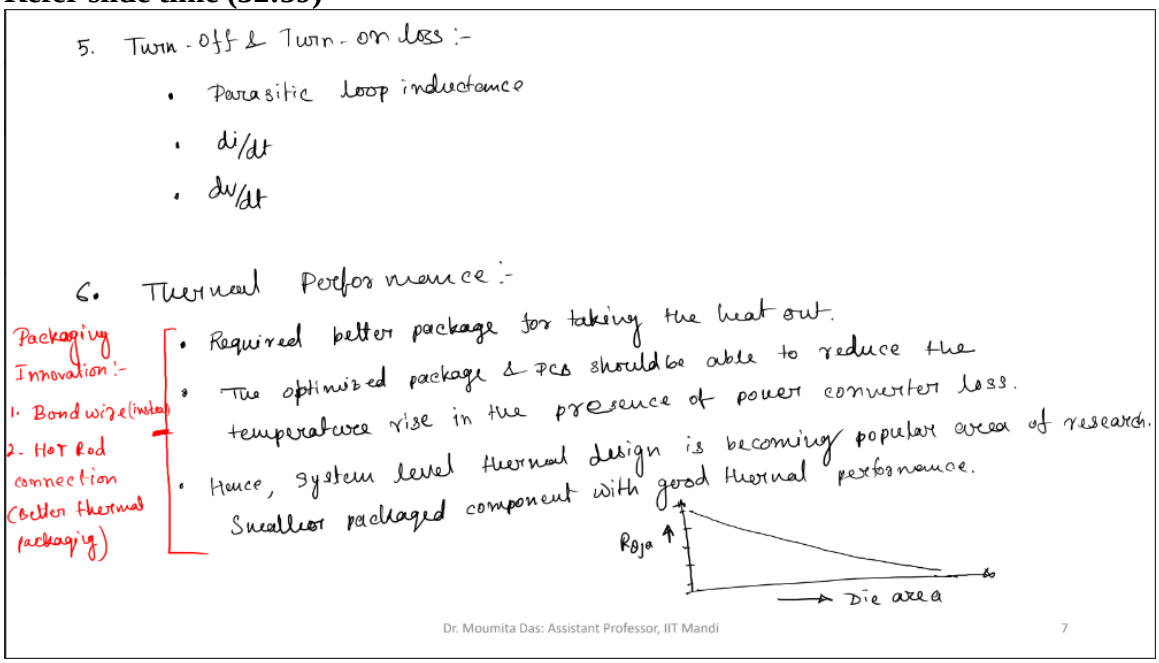

Another thing important thing is that turn on and turn off loss. Although like it comes under switching losses but this turn on and turn off which causes problem due to the presence of parasitic element means parasitic loop inductance. This parasitic loop inductance will cause transient current to be present. So, this di/dt problem and dv/dt problem so basically during turn on and turn off time if there is like parasitic element so there will be definitely parasitic element present in the system and that will cause di/dt and dv/dt so basically current and voltage spike will be there and due to this current and voltage spike obviously then the system size will increase because you know like if there is a spike in the system so then we have to select the device as per the consideration of the spike rating. So, based on that the device size and all the size of the components will increase and that will causes increase in the system size and reduces power density.

So, then these losses need to be considered properly. So, basically design has to be done

properly so that this parasitic element can be reduced down which causes the problem of di/dt and dv/dt. or di/dt or dv/dt problem should be taken care of so that optimized system design will be possible. Now, the thermal performance. So, when I say thermal performance, so system heat dissipation I am talking about.

So, generally what happens as I have discussed earlier so heat generation in the system should be such that it will be able to dissipate through heat sink or the through PCB layout or through the devices. So, it should be able to take off the heat which is generated in the system. So, thermal performance of the system should be improved. So, how that is possible? One of the ways is that so required better packaging. Better packaging with respect to the device or any other component or whatever will be placed in the system.

So required better package for taking the heat out of the system. Now this also requires the optimized package and PCB should be able to reduce the temperature rise in the presence of power converter loss. So, hence system level Thermal design is becoming popular area of research. So the main component where people are focusing is smaller package component. with good thermal performance so probably people can look for the material or the connection how it is done so that this can be taken care of generally the thermal performance is like kind can be characterized as with respect to the thermal resistance.

So, you can see resistance thermal resistance if it is like junction to ambient thermal resistance of any system like device or anything it is increasing. So, it is increasing like this. So, then die area is increasing in this direction let us say. So, as the thermal resistance is more so, then what will happen die area it is basically less.

So it is like this. It can be, sorry, you can actually, so it will not go to 0 because you know like then the system will not be practical. So it is having characteristics something like this. okay so you can see if the dye area is less the thermal resistance is actually more so then heat generation of the system it will be more and then it will be difficult to dissipate if the die area is more so then the thermal resistance is less so the heat generation in the system will be less and it will be easy to dissipate also so this is how the thermal performance of the system can be characterized so i mean both are complementary in nature so we have to select the optimized design again so everything we have to consider like something we will be losing and something we will be gaining so we have to choose the optimum point which will give us the required performance okay so for anything this is like how it is done so okay just let me just tell you the final thing so now these are the problems so what are the problems I have just listed down so basically power density improvement solution is that first is the switching frequency we can increase so switching frequency we can increase so that is like that will again cause that will reduce the magnetics but increasing switching

frequency will cause some other problem anyway like that will not go here. So, we can increase the switching frequency to improve the power density. One thing reduce the conduction loss, reduce the switching loss, reduce the losses due to charge related losses so that comes under switching losses so basically reducing switching conduction losses all the losses reverse recovery losses and the parasitic element present in the system and then improve the thermal performance of the system so this will go this will allow us to go towards high power density system so now So, then if we go for this high power density system, so then what are the things we have to consider? So, these are the things, these are the properties which we have to consider.

Now, what we have to do? We have to consider this reduction in the switching losses. How that will be possible? Let me just write down here. Switching losses, we are saying that we can reduce the switching losses. Then, we have to consider here this is possible by using switching loss innovation so in this particular course we are discussing about wide bandgap devices you know like how this switching losses changes in the wide bandgap devices so if i consider so this is the energy losses that if I consider then what will happen if I just I am not giving any values I am just comparing GaN with respect to silicon and silicon carbide.

So this is how the losses are actually varying. So generally this is like with respect to GaN the losses will be very small for silicon it will be higher than the GaN sorry for silicon carbide and this is silicon super junction devices. So you can see here so So, loss in case of GaN device it is much smaller than that of the silicon carbide than that of the silicon super junction devices. So, switching loss innovation if we have to consider for reducing switching losses. So, then probably we can select the suitable device.

We can go for the wide band gap devices. We can use the GaN device in order to have very less switching losses. So, this is where the innovation can come. next comes so this switching losses it will cover all the losses means reverse recovery loss and charge related loss conduction loss everything okay now next is the thermal performance when we say thermal performance so basically i can just give you one example we have to select like better packaging so better packaging means so better packaging so we have to consider packaging part packaging thermal innovation How that can be done? One example I can give you in the packaging innovation in devices instead of using bond wire some of the devices if they are having bond wire right instead of using that we can go for this hot rod connection. So instead of this this will have less thermal problem or I can just give you better thermal innovation.

So, this is with respect to the device. Devices generally have bond wire. If instead of bond wire, if we can go for hot rod kind of technology, then it is having better thermal packaging.

So, this is hot rod interconnection. This comes under the device part. So, we can actually select those kind of devices which have those connection, which does not have bond wire that will give us better thermal performance.

Right now this all this thing along with advanced circuit topologies. So these all are the solutions that is fine we can choose different devices we can reduce this package related problem by selecting proper packaging. Now if we have advanced circuit technologies which probably will help us increasing power density. that we can also choose. So, all this thing will give us the high power density system using wide band gap devices.

That is what is desirable for wide band gap device applications. More about this I will be discussing in the next class. Thank you.