Power Electronics with Wide Bandgap Devices
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Lecture-16
LAYOUT DESIGN AND PARASITIC MANAGEMENT – Continue

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Welcome to the course on power electronics with wide band gap devices. In the last lecture I have started discussion about parasitic effect in the converter. So how different parasitic components comes from the device so and how that is going to affect the operation of the converter or the DPT board that discussion I have started in the last class. now the effect of parasitics which comes from packaging and the PCB layout that is what i am going to discuss today.

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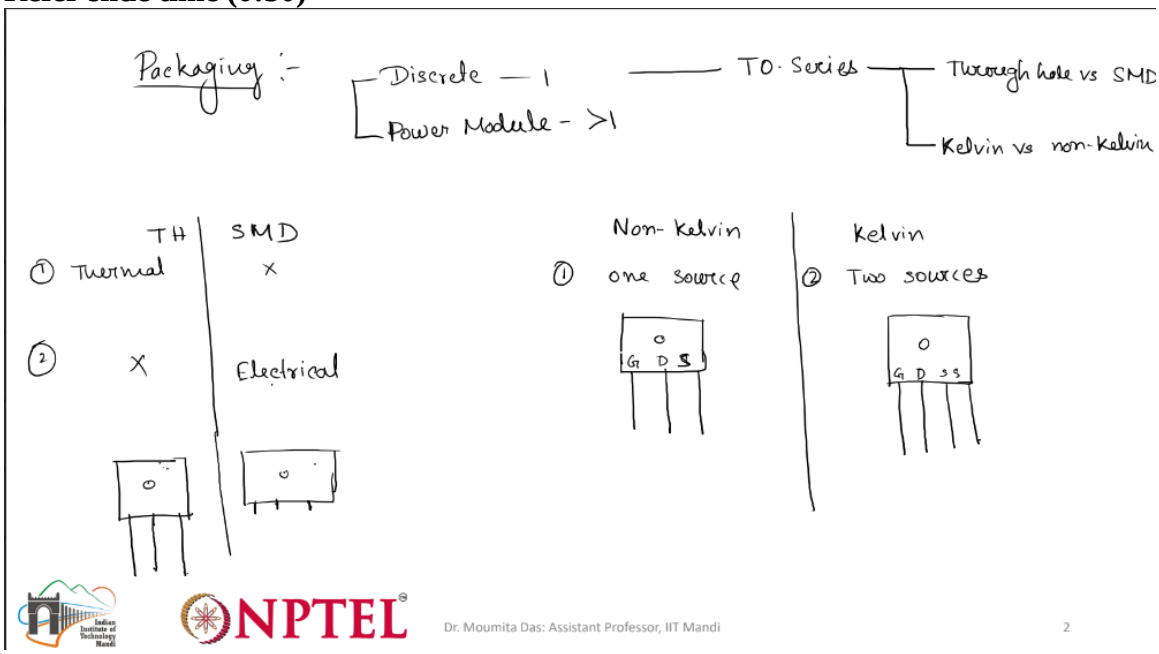

So when i say packaging so basically WBG devices or any devices they can have different types of packaging so how this packaging looks like Generally you have probably heard of discrete component or power module component. So, discrete component means only one device will be present and then power module or the module there will be more than one

device be present. in the particular package.

So, how these devices are available whether you are buying a discrete manner means separately or whether you are buying more than one device in module form and then this you can use in your particular application. If it is discrete device, so let's say for particular inverter application you need six different switches. Okay so it is like conventional inverter which has six different switches. So now the power module there also you need six different switches instead of this using six different switches which you need to use in discrete manner you can use power module which probably has six different switches connected in that particular module.

both are available in the market and this power module since it is having six different switches connected so it is like much more compact kind of design and they are suitable for high power application if it is discrete then you have to place all the components PCB properly and connection and everything should be proper in order to use it as inverter for particular application so that is why for high power application people prefer to use power module rather than the discrete module because discrete module you need to handle all the different devices but the advantage of discrete module is that if there is problem in any particular device you can easily replace that device in the PCB but in power module if there is any problem then the entire module you have to replace So that is the disadvantage of power module. So everything has advantage and disadvantage There will not be any single solution without any disadvantage. Okay, so we have to choose based on our application so now these are like two different types of Module like packaging with respect to the number of devices now there are also like types of packaging under discrete component. So, under discrete component if I try to see, so most frequently used or the popular one is the TO series packaging. So, in this TO series packaging also there are two different types.

So, two different types are classified with respect to through hole versus surface mount versus SMD or surface mount devices and another is Kelvin versus non Kelvin devices. When I say through hole versus surface mount So this is actually one of the another important area or the selection criteria for designing PCB So like both are having some advantage some disadvantage So whenever you see any GaN devices they generally are available in SMD types of packaging in order to reduce different parasitic component okay so now through hole means their leads are like much longer than that of the SMD devices so they are also having some advantage some disadvantage now if I try to tell you about through hole through hole versus SMD so then They can be, so there are actually two different properties which will classify these two different devices. One is electrical characteristics, another is thermal characteristics. In case of through hole kind of devices, thermal management is much better. okay so this is better in case of SMD devices this thermal management is a big problem in case of SMD devices electrical management is

much better and that may not be that good in case of through hole device because you know because of the number of leads So basically if I try to show you so generally what happens the through hole devices they are probably having this kind of big leads and in case of SMD devices so they are probably will have this small small leads.

or maybe they can be much smaller than that. So, then what will happen because this leads are there. So, this through hole kind of devices it has proper place for connecting the heat sink. But in case of SMD devices what happens they are connected to the PCB track So basically back of this device it is having the connection so that can be connected to the PCB layers So now PCB layout if it is connected so that is the only place so PCB layout it actually extract the heat from the device and it dissipate So the dissipation capability of the SMD devices is much lesser than that of the through-hole devices So that is why thermal management in case of SMD devices is much more difficult than that of the through-hole devices Because it has proper access or proper place where you can actually connect the heatsink which can take off the heat from the device Now with respect to electrical characteristics since the leads in case of through hole they are much longer so they will cause inclusion of additional inductance which you know as the parasitic inductance in the power loop. So, again if the parasitic inductance is more you have already seen in the last lecture how it is going to affect the switching performance.

So, this is why this electrical characteristics in case of through-hole devices will be worse than that of the SMD devices. So, there can be much more ringing, di-dittivity effect due to this additional parasitic element. okay now this is with respect to through hole and SMD now what is with respect to non Kelvin and Kelvin so non Kelvin when I say so like so this non Kelvin and Kelvin both are available in SMD as well as through hole devices so through hole can have Kelvin and non Kelvin type similarly SMD can also have Kelvin and non Kelvin type Now Kelvin and non-Kelvin it is actually depending upon number of leads present. So here only one source is present. One source.

So it is similar to that of the. So if I try to tell you with respect to through hole. So it will be having three different legs. Now Kelvin type there will be. two different sources so if I try to draw it for similar through hole kind of component so it will be having four legs instead of three legs now two different sources so basically two different sources let's say gate drain and two different sources here it is gate drain and one source okay Now, these two different sources one for the gate loop another for the power loop and this is actually quite helpful for elimination of the common mode related problem.

So, that is why for most of the application people try to use this Kelvin type of application. devices or packaging where two different sources are there although the sources means kind of we consider as the circuit ground so that is same but due to the connection it will

reduce problems between the gate and the power loop. You have already seen that there can be one common inductance which can be present between the source terminal of the device and the negative terminal of the gate loop. So that inductance we can minimize and that will affect the common mode problem. Okay, so this is where the Kelvin and non Kelvin types of connection comes and this is also available in SMD devices also.

Now it is up to you which kind of packaging you want to choose. so that depending upon your application and also like which parameter you want to optimize for some cases probably you need to optimize thermal parameter so then if through whole component will be better so based on that you can choose particular packaging okay.

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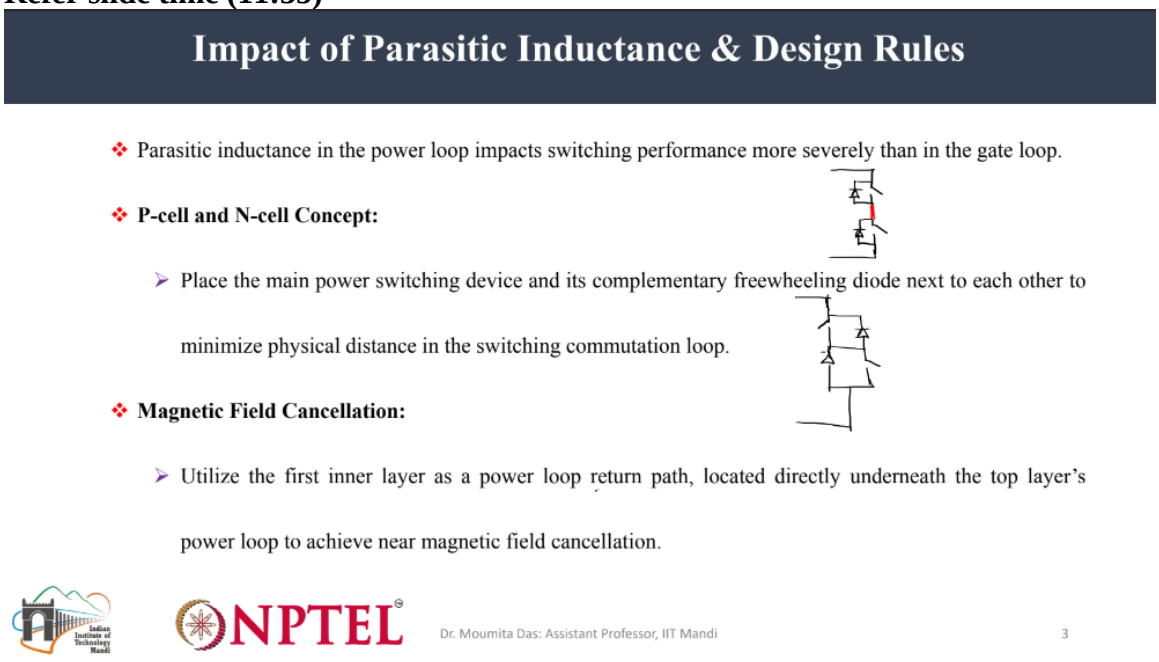

now this is with respect to the device packaging now there are effects which comes due to the PCB layout design. Now, how these effects are coming? So, this parasitic inductance in the power loop which impacts both switching performance that actually is much greater than that of the gate loop because power loop where the length and the thickness and width of the line basically PCB track it is actually much more than that of the gate loop. So, the parasitic inductance effect will be much more in the power loop than that of the gate loop ok. Now, one way to minimize this different parasitic effect is the by using p-cell and n-cell concept so p-cell and n-cell concept is that whenever we connect two switches generally what happens each switch is having their body diode and they are connected through one wire or the PCB track line for any particular leg right So the placing of this main power switch device and the complimentary freewheeling device if we can keep it

next to each other Then it will minimize the physical distance in the switching commutation loop.

So that is known as P cell N cell concept. Means what happens generally whenever we have any switch. So these two switches it is generally connected this way. So the body diode if I try to draw like this. the connection will be like this, right.

So, this is this can be connected to anything. So, and this in between length here, this length will cause some parasitic inductance to be present between two different switches. So instead of if we can have this P cell N cell concept so then how this connection will be so then the connection will be so basically the switch which we have and this diode and then similarly here there will be diode and then there can be switch. So, instead of first connection, if we can have the second connection, then the in between this red line we can actually minimize and that will help us in deduction of the some inductance, parasitic inductance in the path, ok. So, this is the first solution.

Second is that magnetic field cancellation. so, If we can utilize first inner layer as a power loop return path which will be located directly underneath of the top layers power loop to achieve near magnetic field cancellation the positive power loop means top so basically return path means it is having current in the opposite direction and top loop so it is having current in the positive direction so the magnetic effect should be opposite so that it can be like connected such a way so which is given here so then it will cancel the magnetic effect so that will again cause reduction of the magnetics present or the parasitic inductance present in the path.

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Surface-Mount WBG Device

- **Minimization of Effective Lead Length:**
  - Short or leadless packages make minimizing effective lead length in the switching loop insignificant.
  - Focus shifts to minimizing PCB layout resultant parasitics.
- **PCB Layout Schemes:**
  - *Lateral Loop Layout Design:*
    - ✓ Power loop travels only on the top layer, highly dependent on the footprint of DC capacitor and transistors.

Then third is the minimization of the effective lead length so that comes from the device packaging so basically instead of through hole you can you can use SMD short or leadless packaging makes minimizing effective lead length in the switching loop insignificant Okay, so that obviously you have to see the thermal and electrical characteristics and which one you want to choose. And the focus shifts to minimizing PCB layout resultant parasitics. Okay. Now fourth is the PCB layout scheme.

So PCB how we are designing. So there are two different ways. One is lateral loop and another one is vertical loop. so in lateral loop layout design what we need to do power loop travels only on the top layer okay highly dependent on the footprint of the dc capacitor and transistor so in this lateral loop kind of connection.

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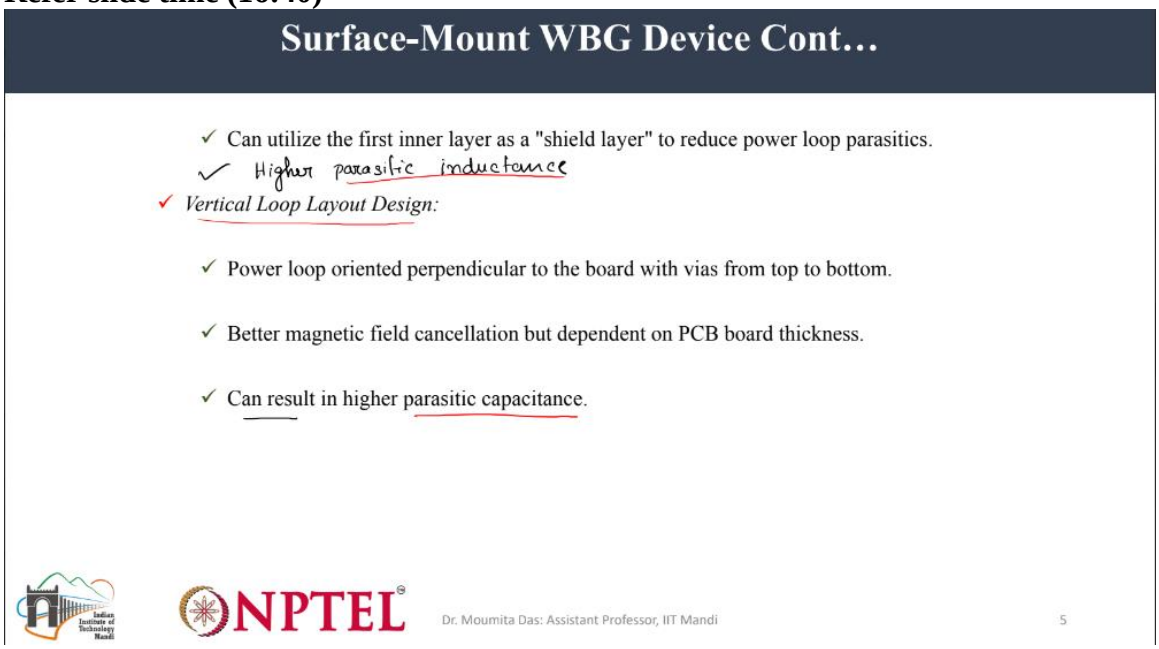

it can utilize first inner layer as a shield layer to reduce the power loop parasitics so this is with respect to the lateral loop structure and the vertical loop layout what it does power loop oriented perpendicular to the board with bias from top to bottom and this is having better magnetic field cancellation but depending on the PCB board thickness so here the PCB board comes into picture and this vertical loop it can result in higher parasitic capacitance And in case of this lateral loop, so here this is having higher parasitic inductance. So, you can see here, so there are actually two different parasitic components present in the converter or the DPT board one comes from the parasitic capacitance some capacitances which are inherent to the device that we cannot minimize but some comes

from the PCB layout design so this you can see if we have vertical loop layout design there are some advantages but the disadvantage is that it is the one which increase the parasitic capacitance now for the lateral one so here it is having also some advantages but the disadvantage is that it is having high inductance now no matter whatever you will choose either you will end up with increasing the inductance or the capacitance now you have to see which effect is going to be more prominent in your application based on that you can design the PCB okay.

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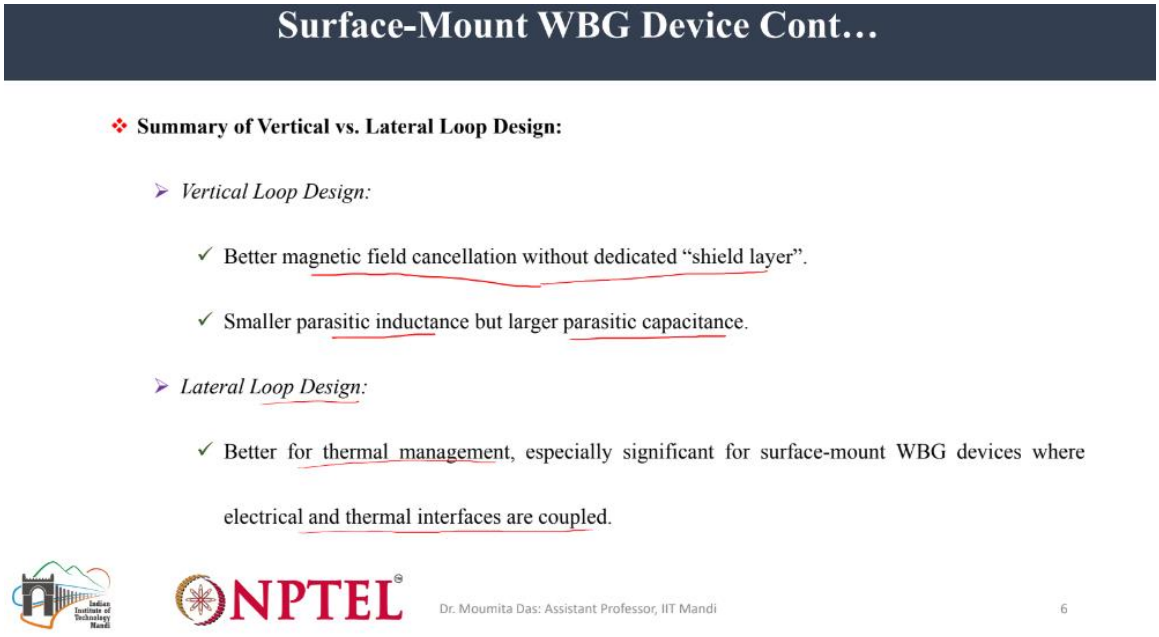

Now if we try to summarize this vertical loop and the lateral loop so you can see here this vertical loop it is having better magnetic field cancellation without dedicated shield layer whereas in case of vertical loop you can see In case of vertical loop the parasitic capacitance is more but inductance is small So, capacitance is the problem in vertical loop But in lateral loop better for thermal management So, especially significant for the surface mount WBG devices where electrical and thermal interfaces are coupled So, this is one of the important thing for WBG applications So, as you have seen for GaN devices their packaging of the GaN devices such that we have to consider proper thermal management technique for those kind of devices.

Now if this lateral loop design it helps us in thermal management then this is like more suitable for this surface mount kind of device where the packaging is very small and where the thermal management is the biggest problem. So then we can Consider for like such let's say GaN devices where packaging is very thin and also thermal management is

challenging. So there this kind of layout is much more helpful. and in case of like the basically package where thermal management is not a problem let's say through whole kind of devices so they are actually we can consider vertical loop since it is having better magnetic field cancellation okay.

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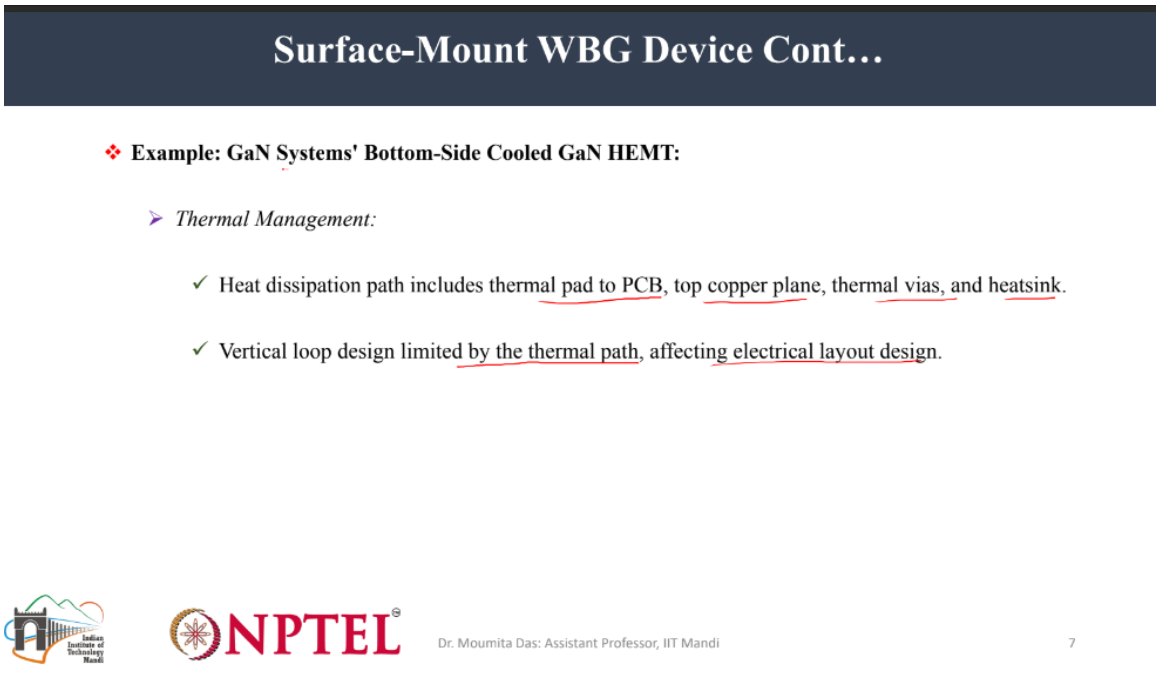

So that is what i told for GaN systems bottom side cooled GaN MOSFET so their thermal management is a big challenge so where thermal management heat dissipation path includes thermal pad to PCB top copper plane thermal vias and heat sink so these are the heat dissipation path generally used for any devices for vertical loop design it is limited by the thermal path affecting electrical layout design okay.

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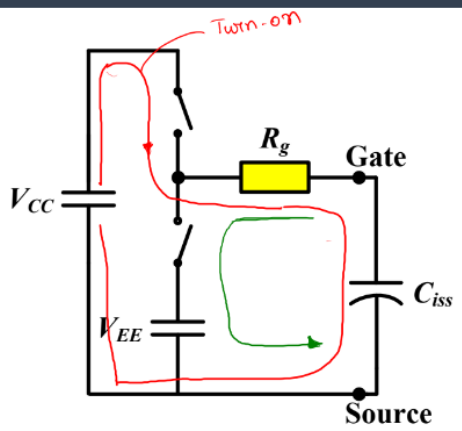
Gate Loop Layout for Gate Parasitic Inductance Minimization



now you can see here gate loop layout for the gate parasitic inductance minimization so here this gate loop it is having the turn on and turn off two different path so if you try to see the turn on current path so generally what happens so this is the gate to source capacitance right now whenever the device is turning on the capacitance will be charging so the current path will be through this so you can see here so this is the Loop for the current to flow during turn on condition. Now during the turn off condition it is actually capacitance input capacitance should discharge.

So then it is having current path in this direction. So based on this current path, this parasitic element in the gate loop can be optimized. There are different solutions I have already discussed. Okay, so those can be considered for this parasitic optimization.

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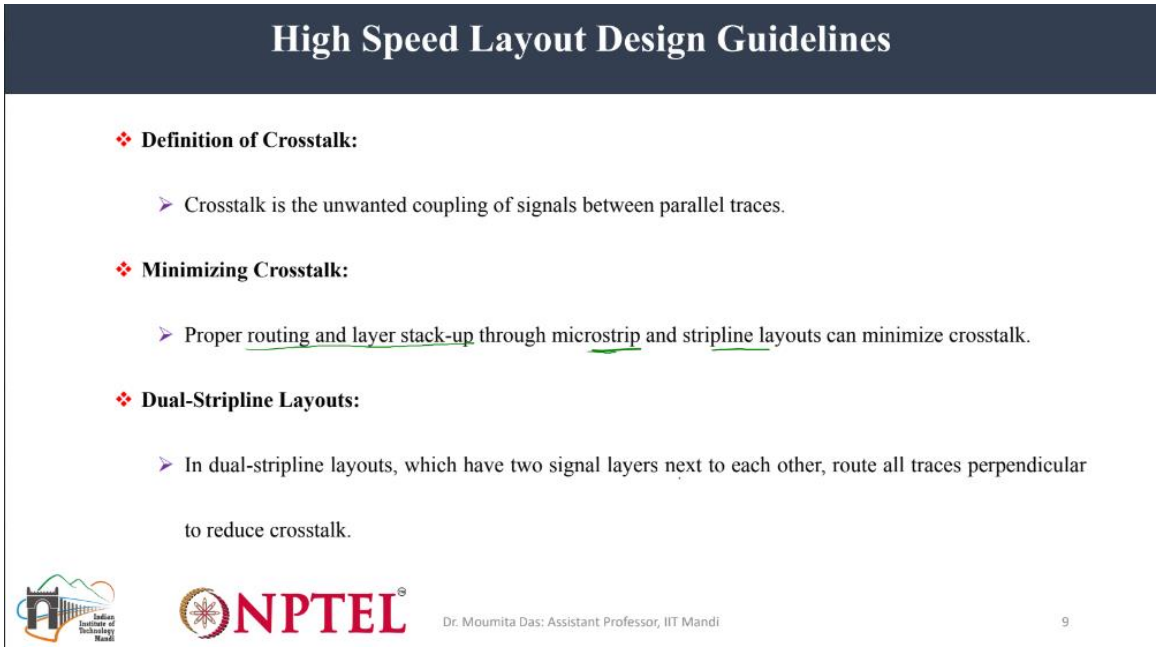

So now if we have to design the PCBs for high speed application means high frequency application.

So, then there can be different problems and how this design should be. So, one of the problem comes from crosstalk. So, that already I have discussed earlier. So, this crosstalk is the unwanted coupling of signals between the parallel traces. so then this parallel traces if it is creating this kind of crosstalk so then we have to minimize this crosstalk related effect how we can minimize this proper routing and layer stack up through microstrip and stripline layouts So crosstalk you have seen what I have discussed with respect to the device so that is different than the crosstalk which comes from the PCB tracks so the meaning remains same but earlier I have discussed about with respect to the devices here it comes with respect to the lines so one line can affect the other line so that is how it is working so then proper routing technique and also the layout how you are going to use so there are two different layout technique micro strip and strip line layout so they can minimize the crosstalk we'll see this how this strip line and micro strip layouts are so in dual strip line strip line layouts which has two signal layer next to each other route all trace perpendicular to reduce crosstalk.

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High Speed Layout Design Guidelines Cont…

- Increase the distance between the two signal layers.
- Minimize the distance between the signal layer and adjacent plane.

❖ **Microstrip and Stripline Layouts:**

- Microstrip layouts involve a circuit trace routed on an outside layer of the PCB with a reference plane (GND or Vcc) below it.
- Stripline layouts involve a circuit trace routed on an inside layer of the PCB with two low-voltage reference planes (such as power and/or GND).


Now this increase the distance between two signal layers and minimize the distance between signal layer and adjacent plane Now microstrip and strip layout, so their microstrip layout involve a circuit trace routed on an outside layer of the PCB with a reference plane below it.Okay. So now you can see in the next it is there.

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High Speed Layout Design Guidelines Cont…

Microstrip Transmission Line Layout.

Stripline Transmission Line Layout.

Transmission Line Layout.

So this microstrip reference line below it and then you can see here this is the reference line which is below it and then this is where the PCB track is presented. Okay. So this is what is written So it involves circuit trace routed on an outside layer So you can see this is the outside top one is the outside layer And then This PCB with a reference plane below it. So reference plane which is at the bottom.

Okay. Now strip line layout it involves a circuit trace routed on an inside layer. So it is present inside and then the micro strip it is present outside. So then this inside layer with two low voltage reference planes above and below. Okay. So, that you can see here So, this is the strip line So, where the PCB trace is presented in between two low voltage reference plane So, this can be either power or the ground anything can be present So, this trace will be in between So, in multilayer PCB it can be created this way so in microstrip here it is the bottom one you can consider as the ground and top one is the PCB trace so these are the two different types of layout designing technique which can reduce the crosstalk related effect now that was with respect to the designing of the layout how the layout should be so that parallel lines should not affect each other okay

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High Speed Layout Design Guidelines Cont…

- **Dielectric Material:**
  - The dielectric constant (ε_r) affects the impedance of a transmission line.
  - Signals can propagate faster in materials with a lower ε_r.
  - FR-4 is a widely used dielectric material for PCBs, with an ε_r between 4.1 and 4.5.
  - GETEK, composed of epoxy and resin (polyphenylene oxide), has an ε_r between 3.6 and 4.2.

Now there is another important point with respect to this layout design that is the dielectric constant affects the impedance of a transmission line So how this dielectric constant is affecting? Let's see that So basically whenever this signal is propagating from one particular point to another so then signals can propagate faster in materials with a lower dielectric constant So now this material part is coming into the picture.

So if you see here, so FR-4 is a widely used dielectric material for PCBs with an that within epsilon r between 4.1 to 4.5. So, what will be the material for PCB that also affects the signal basically how fast it will be transmitted from one particular point to the another point. So, this GETEK composed of epoxy and resin polyphenylene oxide has an epsilon r between 3.

6 to 4.2. So, these are the dielectric constant which are generally used for the PCBs. So, this is like between 4.1 and 4.5 and the material that is generally used that is having the epsilon r between 3.

6 to 4.2. So now you can see here this transmission line. Now you know about this dielectric constant which is coming from the material part. Okay. So the PCB when you will be building.

So how this material is going to be.

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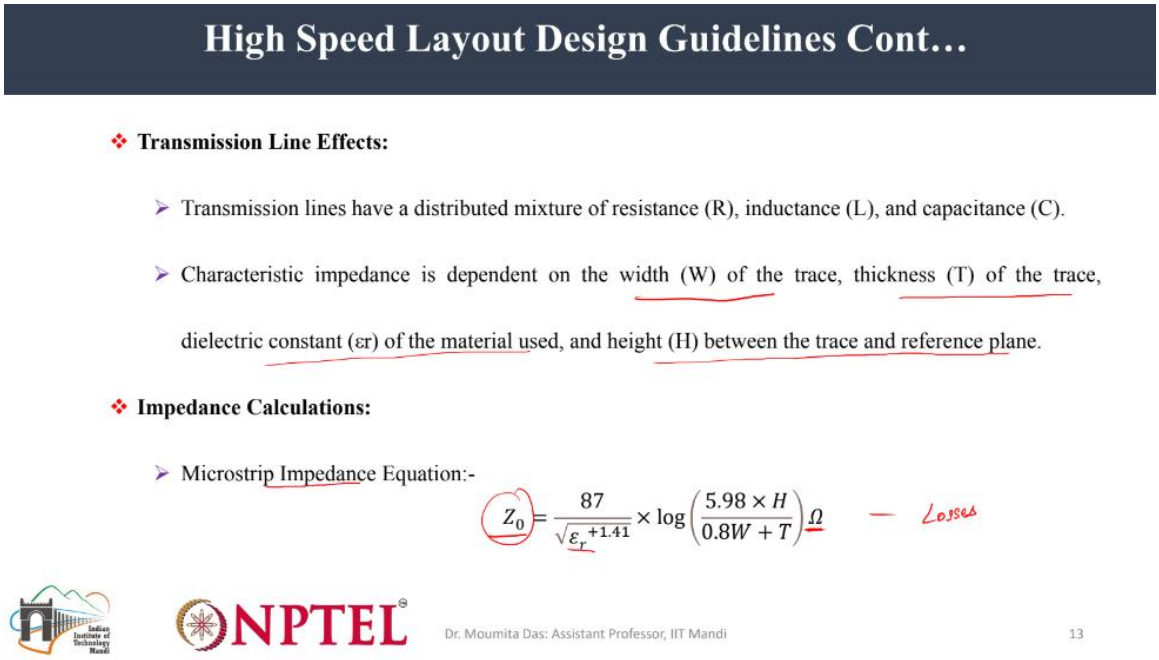

So, now this transmission line have distributed mixture of resistance, inductance, capacitance and the characteristic impedance it is dependent upon the width of the trace, thickness of the trace, dielectric constant of the material used and height between the trace and the reference plane so these are the factors which is going to affect the impedance and this impedance is going to affect the signal so this impedance can be calculated so this you can see if for microstrip impedance equation is so this is

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \times \log\left(\frac{5.98 \times H}{0.8W + T}\right) \Omega$$ — Losses

this much impedance you can achieve for microstrip kind of layout so the layout material so which gives the permittivity so that you can choose so based on the reference values which are given or the material whatever you are going to use so how much this permitivity this dielectric constant is going to be so that you can choose and then height width and thickness of the trace you can actually select so based on that this impedance you can achieve now this impedance will tell you how fast or the slow this signal will travel from one particular place to the another place.

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High Speed Layout Design Guidelines Cont…

- Stripline Impedance Equation:

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \times \log\left(\frac{4 \times H}{0.67\pi(T + 0.8W)}\right) \Omega$$

→ Losses

❖ **Propagation Delay:**

- Propagation delay is the time required for a signal to travel from one point to another.
- It is a function of the dielectric constant of the material.
- Microstrip Layout Propagation Delay:

$$T_{PD} = 85 \times \sqrt{0.475\varepsilon_r + 0.67} \text{ Sec}$$

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so now let's see this with respect to the strip line similarly like it is having different formula because of the different structure so this is

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \times \log\left(\frac{4 \times H}{0.67\pi(T + 0.8W)}\right) \Omega$$

→ Losses

okay so two different impedances you will get for microstrip and strip line so now you can select the you can actually calculate the impedance based on the selection Now this will tell you what will be the propagation delay. Now propagation delay is the time required for a signal to travel from one point to another point. So generally we assume if there is a connection in no time signal will travel from one particular point to another particular point. But this is not the thing which is going to happen. this is also having relationship with respect to how this PCB tracks are and what kind of material is used so this is going to tell us what will be the propagation delay and propagation delay is going to affect the ultimate like delay which is Generally, you can see in the circuit, okay.

Now, it is a function of the dielectric constant of the material. So, this propagation delay you can see here. So, this impedance anyway it is going to give you the losses. Whatever impedance you got from these equations, it will give you the losses and also it will also tell you this like how much delay is going to be present. Delay mainly depends on the dielectric constant, okay.

so now this microstrip layout design the propagation delay it is having this formula

$$T_{PD} = 85 \times \sqrt{0.475\varepsilon_r + 0.67} \text{ Sec}$$

okay This is second. So now this much is the propagation delay. So propagation delay basically is coming from the dielectric constant.

And whatever impedance you got from this micro strip and strip line. So you can see here it is having unit in ohm. So basically this impedance will tell you how much losses is going to happen. This will tell you the losses. And then this is the one which tells you how fast the signal can travel, how fast or the how slow.

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High Speed Layout Design Guidelines Cont…

- Stripline Layout Propagation Delay:

$$T_{PD} = 85 \times \sqrt{\varepsilon_r} \text{ Sec}$$


Similarly for strip line layout you can see the propagation delay it is also coming from this particular equation.

$$T_{PD} = 85 \times \sqrt{\varepsilon_r} \text{ Sec}$$

So, this completely depends upon what kind of material you are using. So, this material will tell you how fast and slow the signal will be traveling. And the trace, thickness, height and width, it will tell you what will be the impedance. And that impedance ultimately will

give you the losses and the heat generation in the PCB track.

Okay. Okay, this is all about today and this is the reference. And also for this formulas, you can... refer the NXP application note high frequency layout design Thank you.

This is all for today. More about this I will be discussing in the next class.