Power Electronics with Wide Bandgap Devices
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Lecture-14
CROSS TALK CONSIDERATION

LAYOUT DESIGN AND PARASITIC MANAGEMENT

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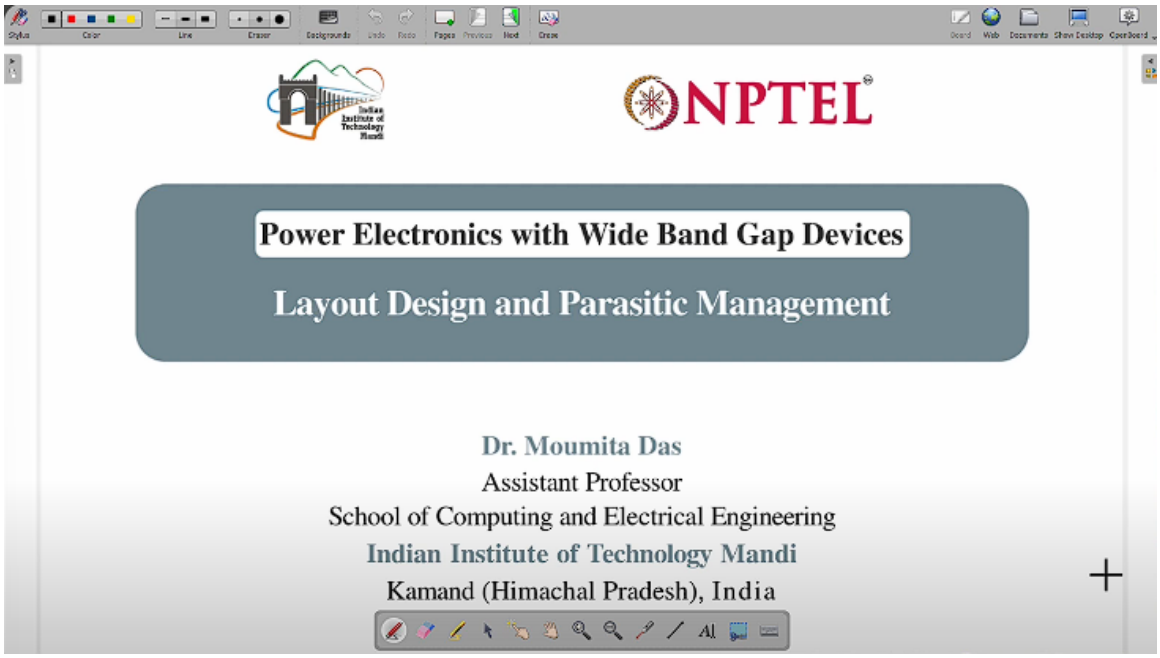

Welcome back to the course on Power Electronics with wide band gap devices. Today I am going to discuss about circuit parasitics and their effect on the switching characteristics. So in the last lecture I have already discussed about different switching issues and how we can mitigate them using passive and active solutions. So, today I am going to include other components in the circuit means parasitics which was not included earlier. So, earlier whatever switching related issues I have discussed so that considering without the parasitic element of the circuit. But now I am going to consider the parasitic element that they are basically included in the circuit either in the form of capacitance of the switches or in the form of parasitic inductances. So, how they are going to affect the switching characteristics, so, that I am going to discuss today.

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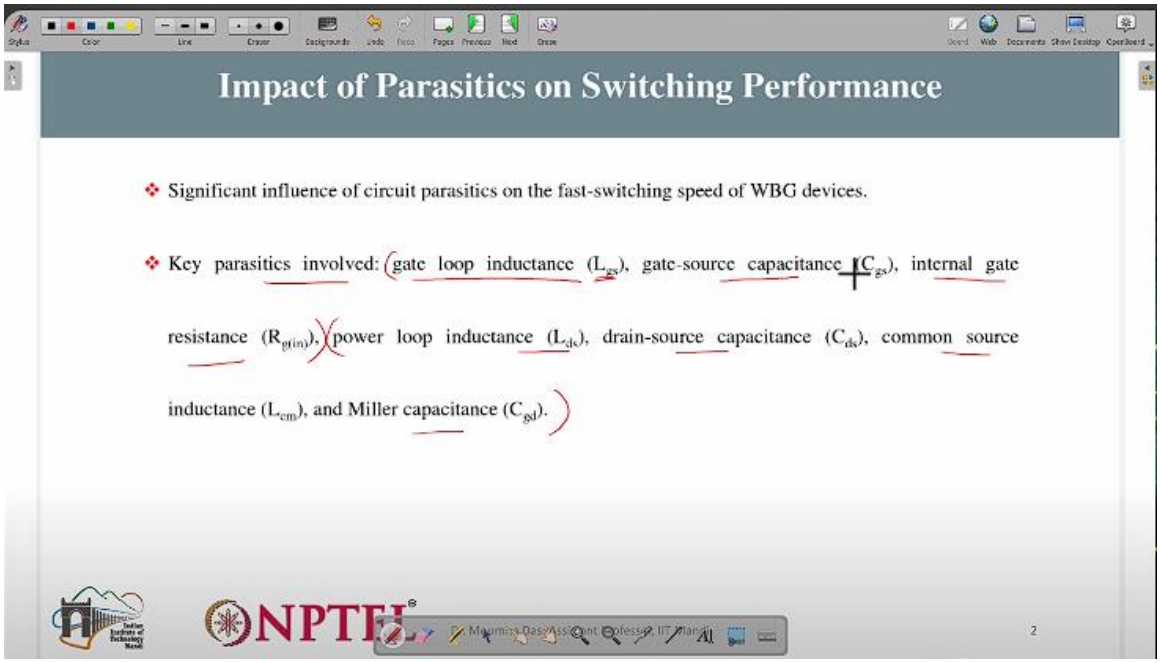

So, as you know the switching parasitics means there are basically either parasitic capacitances or parasitic inductances. So, how this parasitic capacitance or inductances are coming into picture? And also there are two different parasitics involved. One with respect to the gate loop and one another with respect to the power loop. The one which is with respect to the gate loop so that generally affects the switching characteristics during the turn on and turn off time and the other one which is mainly related to the power loop that will affect switching characteristics along with the signal it gives at the output. So let's see what are those components that we need to consider while analyzing any circuit. Okay. So basically, this significant influence of the circuit parasitics on the first switching speed of the WBG devices. As you know, like these devices operate at higher frequency than that of the silicon devices. So, these parasitic components, they become quite significant at that frequency. So, that is why we have to consider those parasitics specially for the wide band gap devices. Now, the key parasitics they are involved as I told you gate loop inductance. So, I will show you in the circuit in the next slide. So, I will just tell you about the different components in this particular slide. So, gate loop inductance, gate source capacitance so which is basically input capacitance of the particular device. So, it will be connected between gate to source terminal. Right? And the internal gate resistance. So this internal gate resistance it is inherent to the switch and also there will be external gate resistance generally that we connect. But internal gate resistance that is already present in the switch network. Basically it is part of the switch so that we cannot separate out. So now these three components are with respect to the gate loop. Now with respect to power loop so there are power loop inductance. So whatever inductance will be coming in the power loop basically in the switching path. So, how this is coming? So, basically whenever we are connecting the switch with respect to the track, PCB track or anywhere we are connecting. So, that actually cause including this kind of parasitic inductances in the circuit path. Okay. And then another is the drain to source capacitance. So, this already you know which is basically known as the output capacitance of the switch or output parasitic capacitance. So this drain to source capacitance it is also inherent to the switch.

And then common source inductance. So this is another inductance which is also coming in the circuit path. And then miller capacitance. So miller capacitance it is generally connected between gate to drain. So it is not connected it is part of the switch. So this will be related to the power load. So, there are two different parasitic related effects. So, first one as I have shown here it is with respect to the gate loop and the second one with respect to power loop and these are the different components which will be coming in the circuit that will cause the effect in the switching characteristics or in the output signal.

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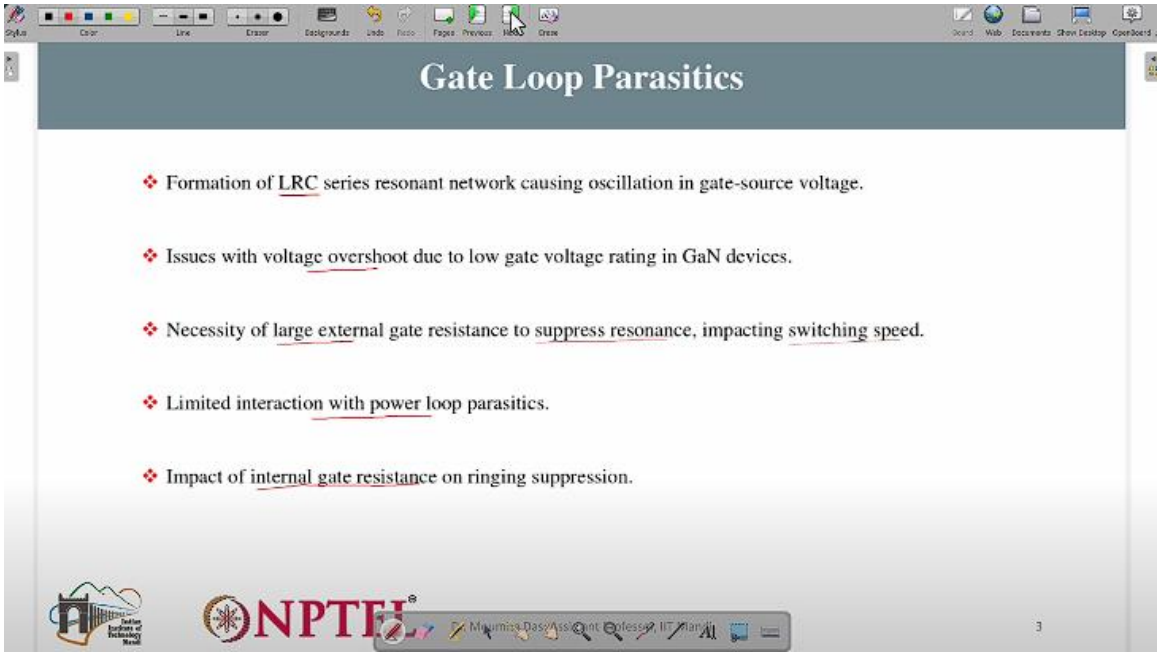

So, basically the gate loop parasitics how it is forming? So, first I will start discussing about this gate loop parasitics. So, you can see this formation of this LRC series resonant network it causes oscillation. So, how this LRC network is forming? So, you can see here. So, already there is a loop inductance L then gate capacitor C and the internal resistance R. So, these three component it is forming LRC or LCR. And this will work as series resonant network. Means if these three component comes so then what will happen that will cause oscillation. Because you know inductance and capacitance that are coming in series. And the resistance we assume it is to be very small. So if the resistance is high then the oscillation will be less. If the resistance is small then the oscillation will be more. So generally for silicon carbide device this internal resistance is higher as compared to silicon or the GaN device. So then in the silicon carbide device the problem related to oscillation will be lesser. But in case of gallium nitride device this resistance value is very small. So if we try to operate at higher frequency now this small resistance will cause huge oscillation in this particular gate loop. So, that is why we have to optimize the value of resistance so that we do not affect the switching turn on or off. In other way, we also will try to reduce the oscillation due to this resonant network. First is this and second is issues with the voltage overshoot due to low gate voltage rating in the gallium nitride device. So that already I have discussed. So how this voltage overshoot is coming in any device.

So if the voltage gate voltage level is less so then the overshoot kind of incident will happen quite frequently. So that also we need to take care. And I have also given different solutions with respect to passive and active components, how we can reduce that impact, okay? Now how this different parasitic component will cause this overshoot so that we will see in the next slide. A necessity of large external gate resistance to suppress the resonance impacting switching speed as I told you so we cannot increase this resistance to very high value then that will affect the switching frequency. Now limited interaction with the power loop parasitics. So now power loop parasitics as you can see, so that is separate with respect to gate loop parasitics. So if there is like more interaction with respect to gate loop parasitics so this effect will be more. Now impact of internal gate resistance on ringing suppression. So this internal gate resistance also can help to suppress this kind of ringing, so that also kind of beneficial for silicon carbide device, it is more so it is beneficial for the network.

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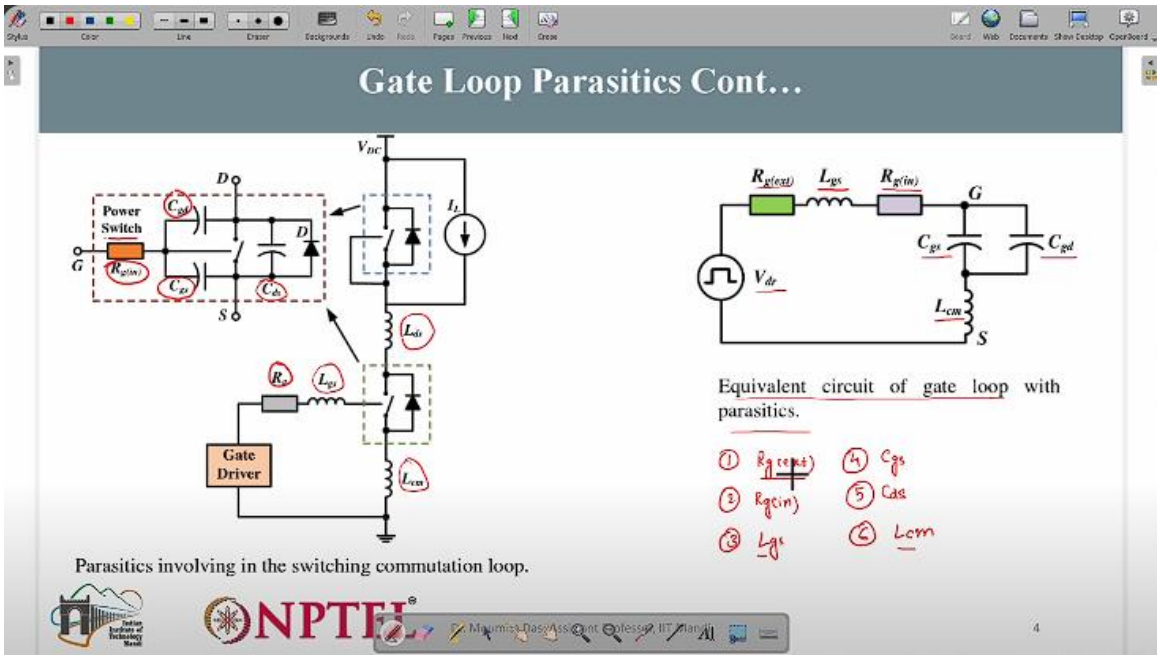

Now you can see this this is the diagram of the gate loop parasitic, so you can see here so this switch so in this particular block so the power switch is shown, so which is shown here in the dotted line, so power switch is having these three different parasitic component inherent to it. Any power switch if you take these four different parasitic components will be there. So here four components are three different capacitances. They are Cgd, Cgs, Cds and internal resistance of the switch. Right? Now this will come in any device, okay? In addition to this particular device you can see here with respect to gate driver so there is one external resistance. This Rg it is external resistance and Lgs it is arising due to connection of this external resistance with the gate terminal, so whenever we are connecting anything so that will cause some inductance to form in that particular branch loop or any where with whatever you are connecting that will cause inclusion of this kind of parasitic inductance. If the length of the wire or PCB track is small so this inductance will be smaller. So now we can optimize this value depending upon the circuit layout and how we are connecting the driver with respect to

the gate. So that can actually give us optimized value of this particular inductance. Okay? Now another inductances which are coming so you can see here between two switches there is a inductance which is coming Lds. So basically drain of one particular switch or the lower switch connected to source of the upper switch. So that connection gives parasitic inductance Lds and source of the lower switch connected to the common terminal or the ground terminal, so that gives parasitic inductance Lcm. So these are different parasitic components which are due to the presence or which can be present in any network. No matter whatever the situation, so, these values may change, but this parasitic components will be there. So, it is important to include these parasitic components while analyzing any circuit, right? So, now you can see the equivalent circuit of the gate loop parasitic. So, you can see here, So, here the input, so whatever voltage is coming from gate driver, it is connected to the external resistance, Rg external, it is shown here, which is shown in terms of Rg in the left diagram and then there will be Lgs, this parasitic inductance between gate terminal gate terminal so basically resistance at the gate terminal and then there will be internal resistance of the switch comes in series with that and this will be connected with the two the different capacitances one is Cgs another is Cgd, these two capacitances will be connected in parallel. So whenever there is a signal going to the circuit it will see from the basically gate drive perspective, it will see all these different parameters and then this particular inductance will be coming. So you can see here with respect to gate loop so basically there are So six different parasitic components. So you can see here Rg external then Rg internal. Rg external we can vary and that we can increase in order to reduce the oscillation but again we have to see that what is the optimum value we can use so that we don't affect the switching speed. Then Lgs, Lgs it comes from the layout. So we have to see how we can actually optimize the layout so that this Lgs will be small. Now fourth, it is Cgs and five is Cds. So 4 and 5 they comes in the device. So basically we have to select a device that can give us these values very small or we can see the switch which will be suitable for the particular application and also having smaller parasitic capacitances. So that we can just choose but we cannot change these values and this 6th is the Lcm and this also comes from the circuit part. So basically circuit layout layout how we are designing so that will give us this Lcm. Okay? So this inductances both the inductances depend upon the layout designing part. So there we can actually see the optimize optimization in the layout design, how we can do so that these values we can reduce down. Rg external we can connect based on the device information given in the data sheet and also how much we can connect so that we don't affect the switching speed and other three parameter that comes with the switch so we have to select the switch to have suitable this parasitic parameter for the particular application. Okay?

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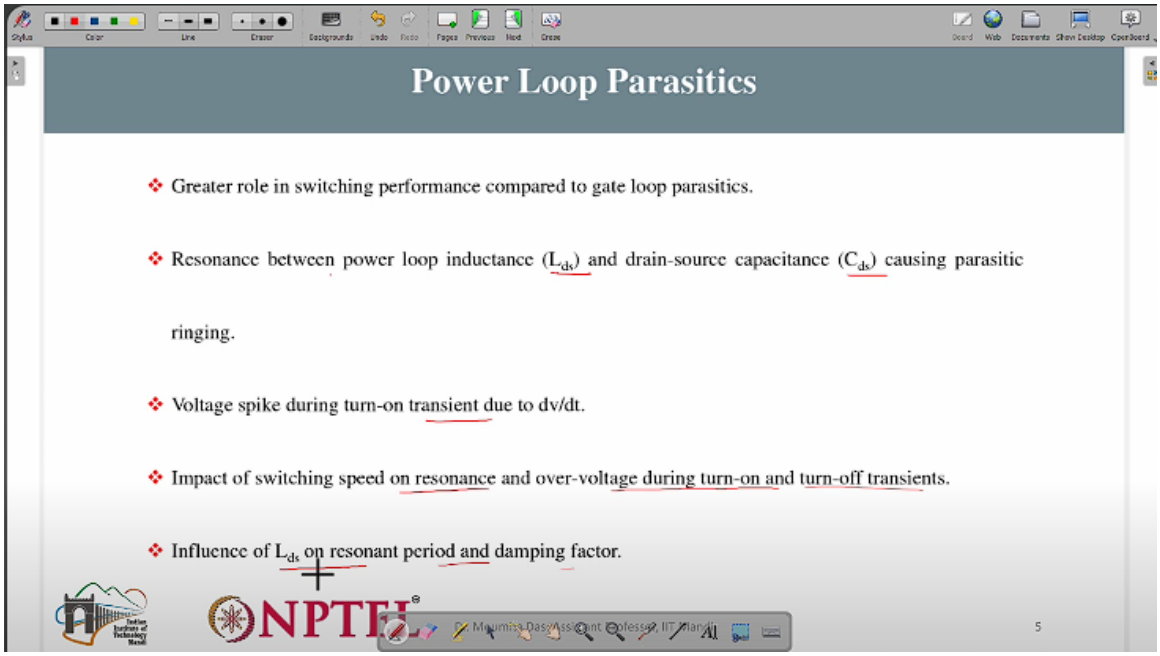

Now comes to power loop parasitics. So how this power loop parasitics are coming? So basically greater role in switching performance compared to the gate loop parasitics. So basically this is having more or direct role while operating the switches. Because gate loop parasitics it is affecting the gate signal. Maximum it can actually affect the gate signal by increasing turn on or turn off time, right? But the oscillation part in the power loop parameter, so that will come from the power loop parasitics, okay? And the resonance between the power loop inductance drain to source capacitance causing parasitic ringing and there will be, so the you can see here this L and C is there so here R component is not there because you know, so in ideal circuit, so if we consider any layout, so there we are considering only inductance but whenever we have any PCB track or the any wire connected between any component, so that will give both inductance and the resistance. So that resistance is known as the stray resistance. So that will give again the RLC series network, where the R value will be very small. So this L and C they will be dominating. So that will cause parasitic ringing or the oscillation in the power signal. Okay? and the voltage spike during turn on transient is due to dv/dt and impact of switching speed on resonance and over voltage during turn on and turn off transients. These are the effects due to this power loop parasitics and influence of Lds on the resonant period and the damping factor so this Lds not only impact the signal by including the oscillation or the ringing but it will actually cause the resonant period to vary so how much time this oscillation will sustain so that will come from this Lds value and it will also affect the damping factor. So how fast this will oscillation will die out so that will come from this Lds value.

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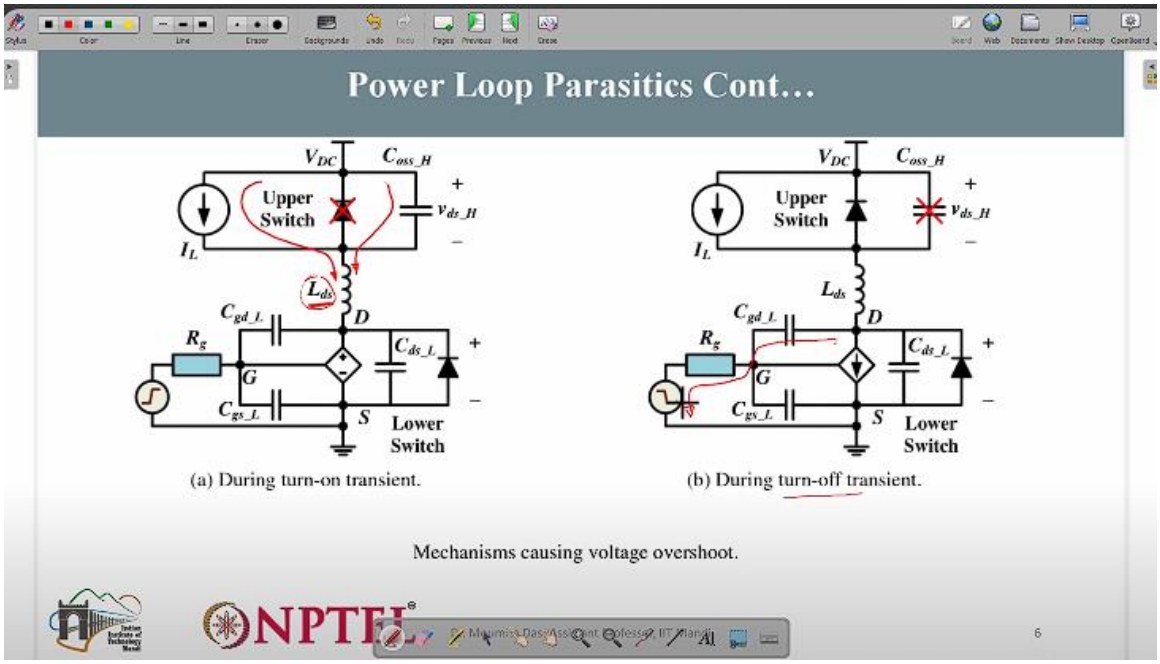

So this you can see the circuit diagram of power loop parasitic. So you can see here so already you have seen what are the components can be present with respect to power loop parasitics. So let me just tell you how this will be operating. So you can see here so whenever this lower switch during the turn on transient so whatever is happening? So the voltage overshoot how it is coming so that I will just tell you. So during the turn on of the lower switch so then what is happening? So this lower switch is turning on and due to which there will be current which will be coming from the Miller capacitance of the upper switch. And this current path will be through this. Okay? And the lower switch it is represented in terms of the voltage source this you can see this voltage source here and it is having all the different parasitic capacitances associated to it and this voltage source is acting here in the lower switch and then this will cause this current whatever is coming from the upper switch to increase and due to this Lds so Lds component it will cause so, basically so it will cause the current to flow whether it depends on basically the inductance value. So, whether the current will be high or low. So, depending upon these parasitics, this current component will vary or the magnitude of the current component will vary. So, that is why we have to make sure that this parasitic component is as low as possible. And during turn off time how it is affecting? So, basically during turn off time, so when the lower switch it is actually shown here in terms of the current source. So, basically this particular switch it is turning off and the current it is flowing, how it is flowing? So, basically current through the miller capacitance to the Rg it is flowing through the gate signal. right? So in this case what is happening this will again cause voltage overshoot to happen okay so now for GaN devices as I have discussed all this problem so I am not going in details of this. So already you know how this current path and everything will be so this is with respect to the parasitic path. Okay? Now you can see this power loop parasitics how it is coming,

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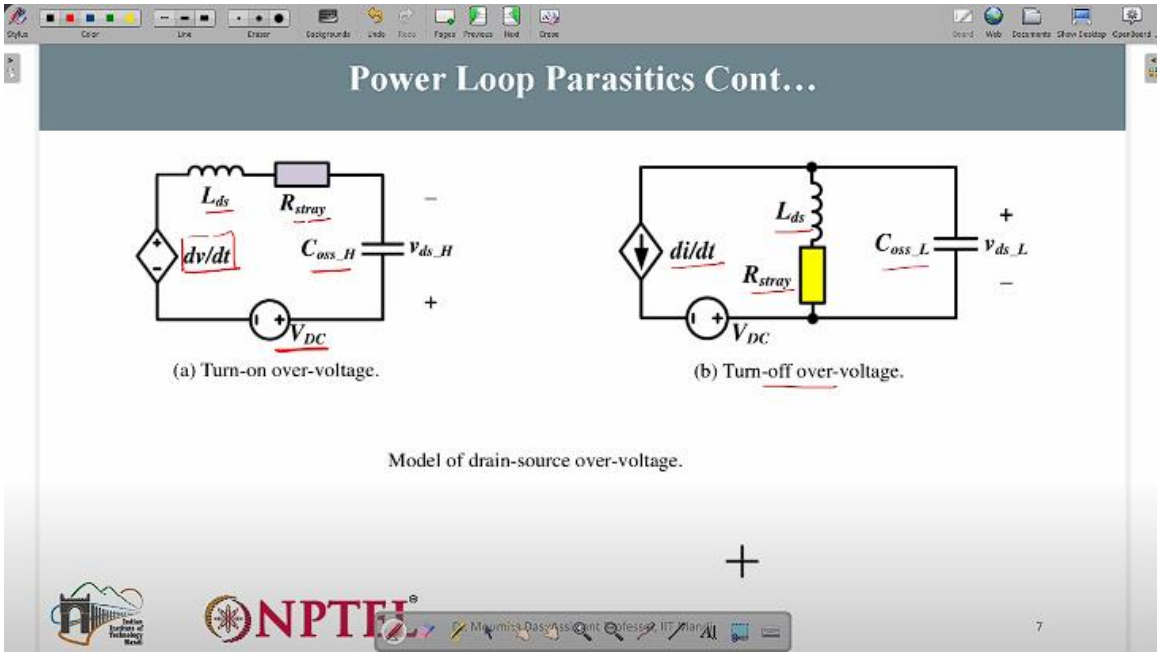

So the basically resonant component how it is coming so you can see here so this is represented in terms of dv/dt which is shown in voltage source during the turn on time and the Lds Rstray which i told you generally from any track there are two different component comes one is inductance and one is resistance this is represented as Rstray and the output capacitance or the capacitance which is coming connected between the drain and source, this is coming in series and this will cause and this will be connected to the vdc input voltage source, so this will cause the oscillation to present in the circuit and during the turn of over voltage how it is happening, so it is represented as current source so this is coming as di/dt so di dt how it will be connected so it will be connected in parallel with the inductance L and the stray resistance which will be coming connected in parallel with the capacitance so this will work as the parallel kind of resonance during the turn of time, okay?

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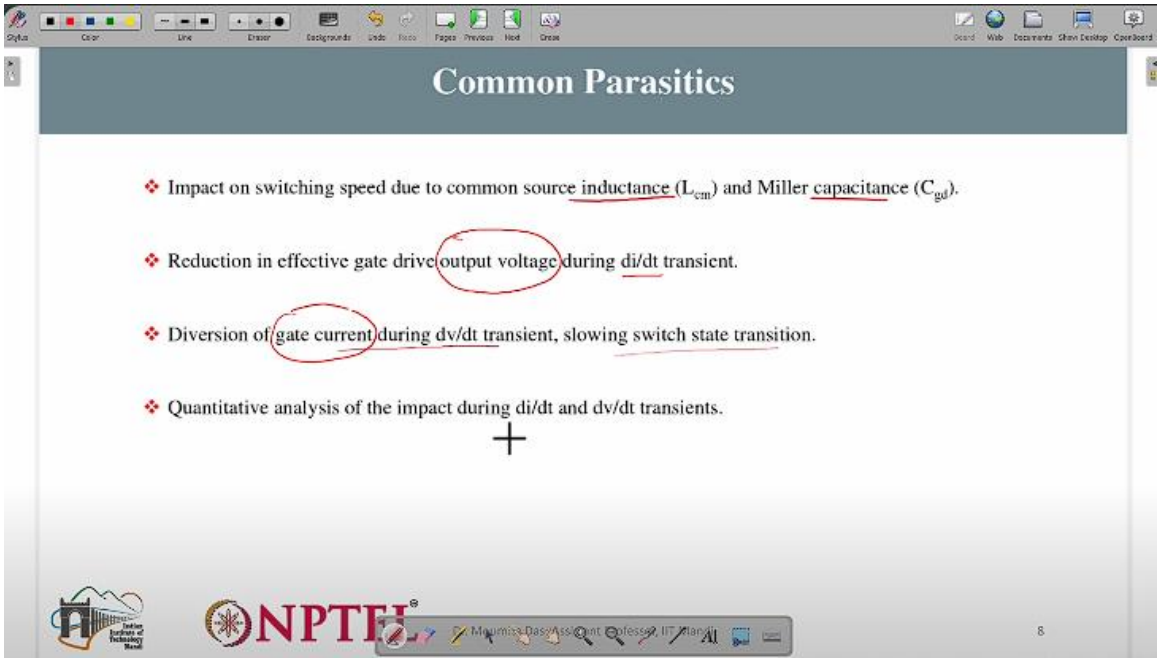

Now these are with respect to separate parasitics which are present in gate loop and the power loop. And then there will be also some common parasitics which will be present between the gate loop and the power loop. So what are those common parasitics? So, impact of the switching speed is due to the common source inductance and the Miller capacitance. This common source inductance which you have seen it is basically connected between the source terminal of the device and the ground terminal of the gate. Means we assume that gate ground is connected to the source terminal. But there will be some track between the gate ground and the source terminal. So, this will cause presence of this particular inductance. So, whatever will be the path exist between the source terminal and the ground of the gate, so, there this inductance will come. This is known as Lcm and the Miller capacitor, this already you know so I don't have to explain again, so this is present between the gate and the drain terminal of the device. So anyway like this two component it is connecting gate with the power loop, so that is why this is known these two component are known as the common parasitics, so this will affect both the gate loop and the power loop, okay? So, now reduction in the effect what will be there due to this common parasitics? This reduction in the effective gate drive output voltage during di/dt transient. So, di/dt transient when it is coming? During the turn off time. So, during this time the gate drive output voltage can reduce effectively. Okay? Now diversion of the gate current during the dv/dt transient. So dv/dt transient is coming during the turn on time. And if it is coming, so then what will happen? So whatever current we need to provide to turn on the device, that current will reduce down because of the diversion. And what will happen because of that? That will slowing slow down the switch state transition. So, it will if the current is not enough. So, the current which is supposed to come from the driver circuit to the gate terminal. So, what will happen that will increase the turn on time. So, ultimately your rise time and the delay time associated with the rise time that will increase and eventually it will affect the switching speed. So, that is why we have to make sure that there is there will not be any effect in the gate current and the gate drive gate voltage basically gate drive output voltage means gate voltage during the turn on and turn off transient. But if this parasitics are

present that will affect so how it is affecting that is written here. Now this quantitative analysis of this parameter is required in order to make sure the switching operation is proper during the turn on and turn off time due to presence of different parasitic parameters, so that is why we have to include all these parasitic parameters in the dynamic analysis so in dynamic analysis what we do generally we consider DPT, so DPT whenever we are considering previously i have already discussed about DPT's so there we don't consider any parasitic parameter neither with the gate loop nor with the power loop we consider just the two switches and the inductance, if you are connecting two switches or one switch one diode connected with the inductance in ideal connection, so there will be no effect from the parasitic side, so for basic understanding of the circuit operation that is fine but if we have to analyze the circuit properly then we need to have information about this parasitic parameters or we need to at least include this in the analysis then we have to see how it is actually impacting the gate signal and the power signal. So, this is why this common parasitic we need to consider during the di/dt transient and the dv/dt transient.

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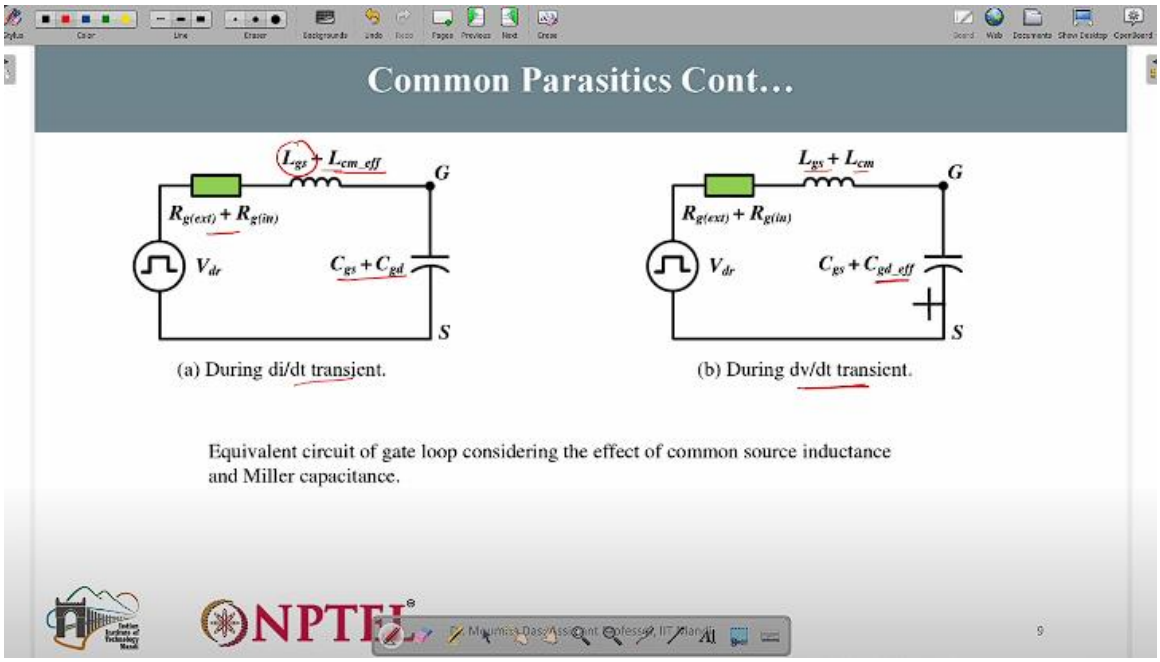

So, whenever we are analyzing the gate signal, so we have to consider this resistances. So, you can see here. So, here earlier for the gate drive part, so gate loop whenever I have discussed in the earlier slides. So, there only Lgs was connected. So, you can I can just go back to show. So you can see here only Lgs is connected and then Rgs in is connected. Here Lcm is connected here. So now net we have to consider. So here you can see two inductances are connected here and Lcm effective is connected here and Cgs and Cgd, these two are constant. We can actually get it from the data sheet if we have the information or you know how to actually derive this capacitance values from the device or capacitance testing you can do to get these values and now during dv/dt transients this cgd effective is coming here these two parameters are fixed. Okay, so this is where the difference is coming while analyzing the circuit. Although you have all the parameters connected to it and the which parameter will vary during the turn on and turn

off time that information we need to include in the analysis part. So, basically equivalent circuit of the gate loop considering the effect of the common source inductance and the Miller capacitance they are connected, they are shown here.

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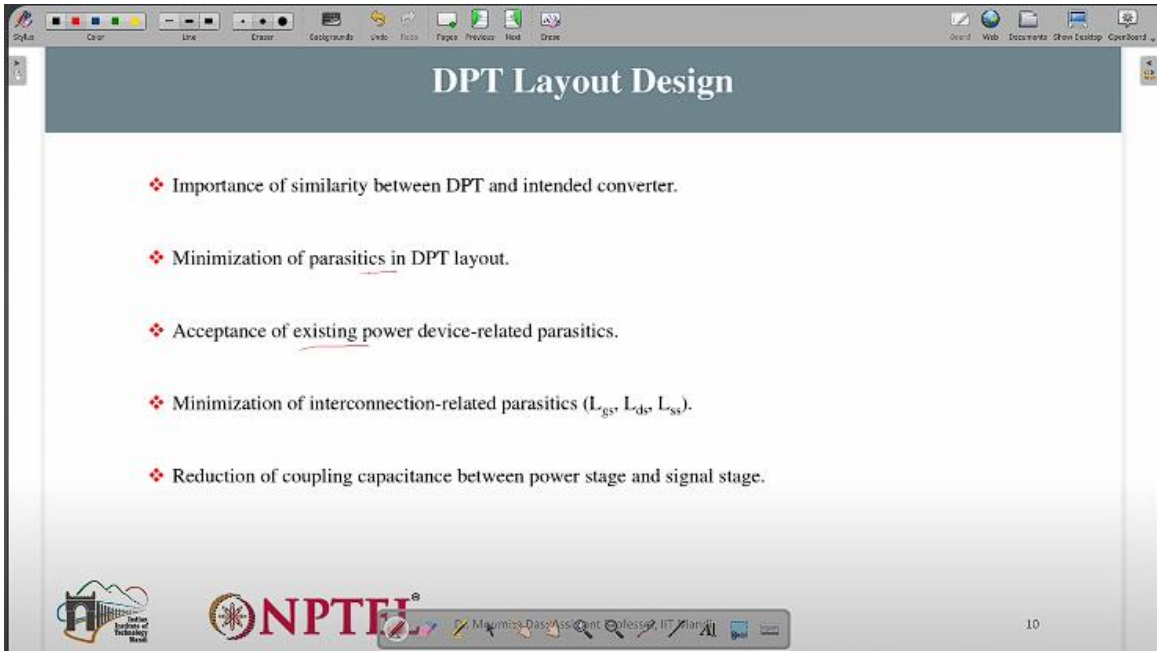

Now, as I told you, so this is what we are going to include in the DPT analysis, DPTs for the analyzing of dynamic dynamics of the converter. So, basically dynamic analysis can be done by including these parasitic parameters. So, this minimization of the parasitics in the DPT layout accepting the existence power device related parasitics and minimization of the interconnected related parasitics and detection of the coupling capacitance between power stage and single stage. So, these are considered while analyzing the DPT circuit. So, you can see this.

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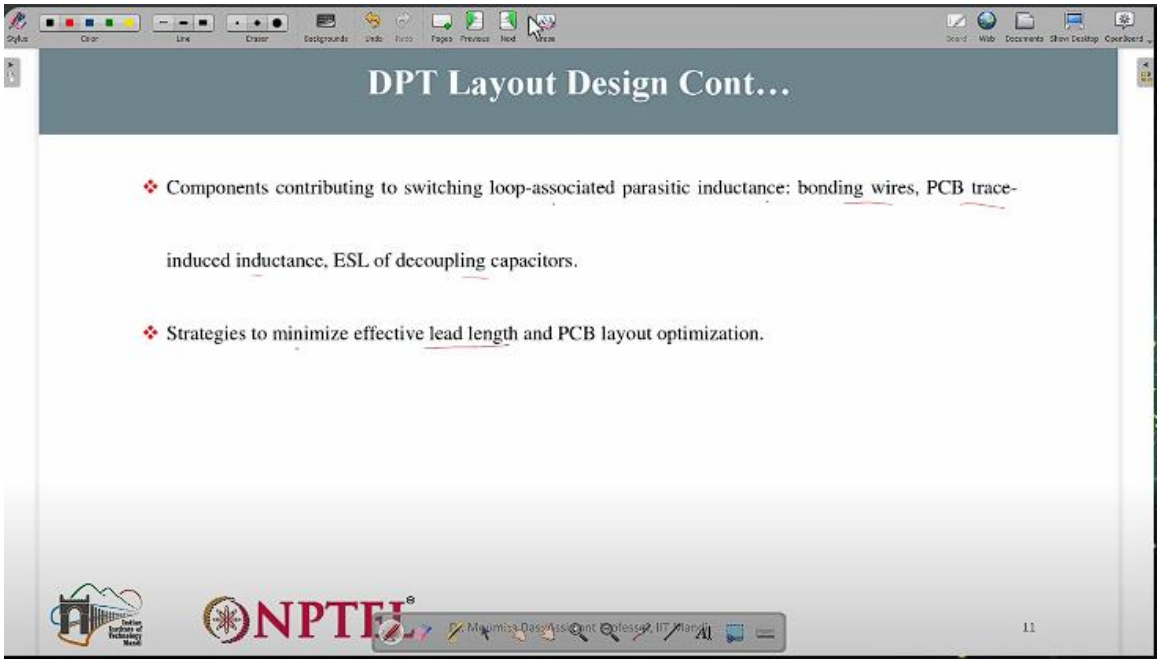

So, and also this components contribution to switching loop associated with transiting inductance, this bonding wire, PCB trays, all these things are considered. Okay? So, this will, this strategy is to minimize the effect lead, effect lead length and the PCB layout optimization.

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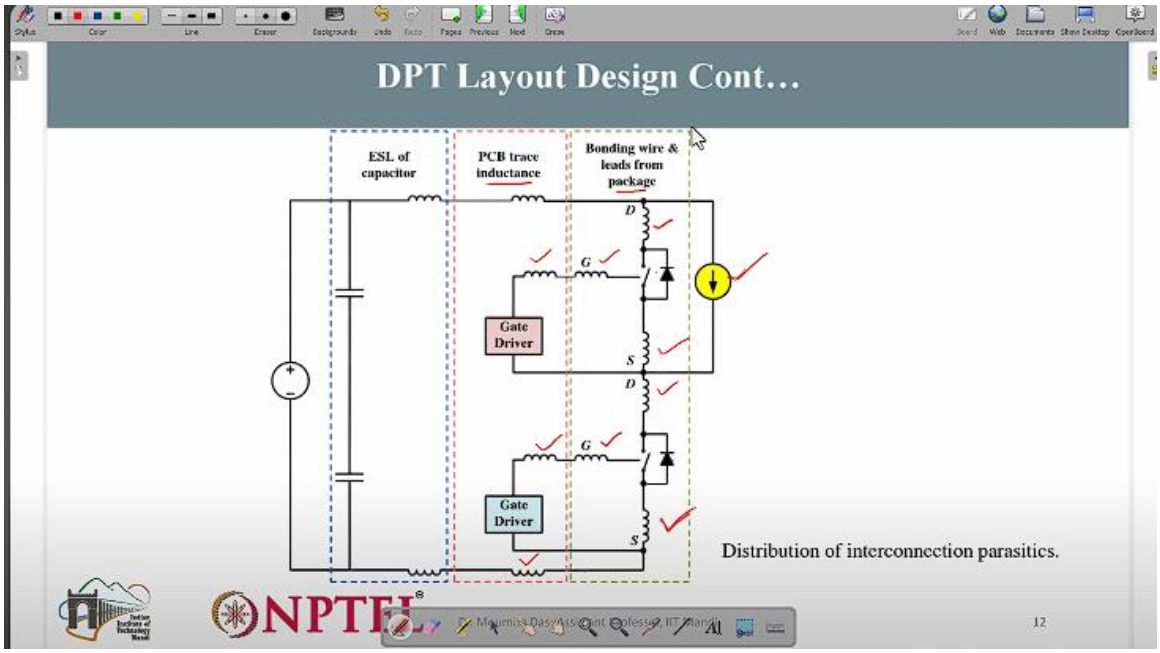

So now this is the DPT layout. So here you can see. So there are actually three different dotted lines are shown. So three different dotted lines gives three different types of parasitic elements. So basically three different parasitic elements how it is coming? The first one it is coming from the gate loop power loop separately. Second one it is coming from the interconnection. Means whenever you are trying to connect switches like two switches together or the gate right part with the switches. So there the interconnection part is coming. So from there second part is

coming. and the third one it is coming from the basically if there is any effect in the signal isolator with the isolated supply, so due to the effect of one particular component with respect to the other component whatever is coming so that also is included, so due to these three different parameters so this these three different dotted blocks are coming. So these three different dotted blocks are shown here so the first one with respect to the switches and how the different parasitic components in the switches are coming? So first is the bonding wear and leads from the packages, so whatever leads you can see for GaN device, so this leads of the GaN device if you have seen the GaN device then you will see these are basically SMD kind of devices. So the lead length will be much smaller than that of the silicon carbide or the silicon device. So this length will cause increase in the parasitic inductance. So these inductances are shown here. So, these are basically coming partly it is coming from the bonding wire and partly leads from the package. So, how the packaging is done? So, if you try to find out any device generally the device data sheet will keep what kind of package it is. So basically SMD package or the packaging type, so based on the packaging type some devices you will see the lead length will be more than that of the some other devices. Even though it is not SMD devices and SMD devices it will be like much smaller, so based on this lead length, so this inductance will vary and bonding wire it is already there inside the device, so that also we cannot do anything but what we can do based on any particular application we can actually choose a package which will give us lower value of this parasitic inductance. So same device may have different packaging. So this different packaging will have different inductances. For some application it is mandatory to have like low inductance packaging but for some application it is up to us which one to select. Some may be easily accessible or easily we can connect for testing and all these things. So then based on that this inductance value will vary. Okay? So this is with respect to the device part, now the second which comes from the PCB trace inductance, PCB trace means that whenever you are connecting the gate driver either you can connect let's say like there can be upper layer lower layer so multi-layer PCBs you can have in one layer you can have gate driver in one layer you can have power component or you can actually connect in the same layer so there can be some like wire length or the track length which can be connected between this gate driver and the device. So this will give us the inductance. So how you are going to design the PCB? How you can optimize the length of the PCB track so that this inductance can be optimized. So this gives us these three different inductances. Mostly the inductance will come between the gate driver and the point where it is connected to the device and some part will be between the gate driver ground and the device ground basically device source and then again some part will be coming between the gate driver ground or the point where it will be connected to the input DC source. Right? Or in this particular case the input capacitor and the third one is the ESL of the capacitor. So ESL of the capacitor, so basically capacitor generally we consider ideal kind of component. So then whenever, we are connecting this capacitor, so there will be again some track length between the gate driver point and the capacitor point. This will give us this ESL of the capacitor. Again this can be reduced down if we try to connect multiple capacitances in parallel. So that again like we have to see how we can select this optimization of this capacitance. So these are the different parasitic distribution in the DPT layout. So now if you try to read recall the DPT circuit which I have discussed earlier, so, there only these switches were there. This current basically here it is shown as the current flowing here through the inductance is the current source. So, the inductance will be

here and the input voltage source. So, all the parasitic components were missing and again these parasitic components considering only the inductance effect the other effect due to parasitic capacitance and everything that are not included here, so which i have already discussed in this particular slide so what are the components are not included so these components also you can include in order to analyze the circuit properly and in order to get the proper or the actual characteristics of the device. So that whenever generally what happens whenever you are testing any device in the DPT so the characteristics whatever you will be getting that may be different than the characteristics which you will be getting whenever it will be connected to the power circuit or any power converter. Because we do not include all these parasitic components. If we include then what will happen the characteristics whatever you will be getting that will be very similar to the characteristics we will be getting from the converter part. So that is why it is important to include these different parasitic components. Okay?

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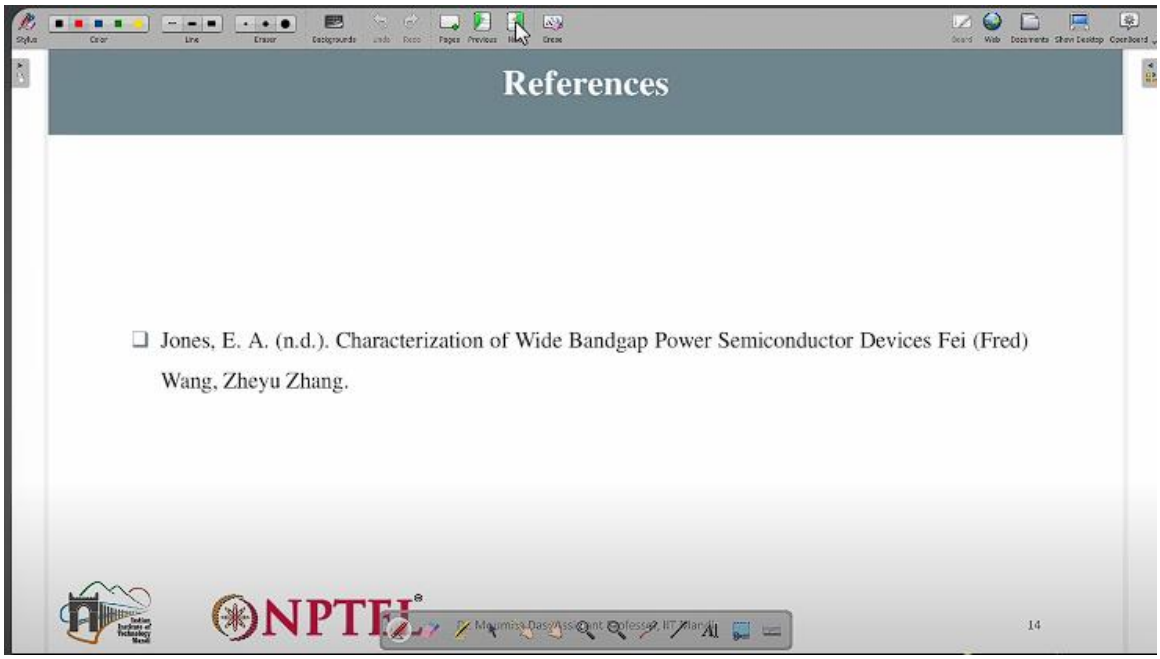

More about this I will be discussing in the next class. So this is the reference for this particular discussion. Thank you.