# Power Electronics with Wide Bandgap Devices Dr. Moumita das School of Computing and Electrical Engineering Indian Institute of Technology, Mandi

# Lecture-14 CROSS TALK CONSIDERATION

# **CROSS TALK CONSIDERATION**

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Hello welcome to the course on power electronics with wide band gap devices. In the last class I have started discussion about the crosstalk related consideration. So how the problem during the turn on and turn off time of the switch is happening and how we can mitigate them. So in the last lecture I have discussed mostly about the passive type of consideration. So what kind of solution exists if we use the passive components and also I have started discussion about the active related solutions. So, as you have seen in the passive related solutions we can either connect capacitance or the voltage negative voltage we can supply. So, basically there are two different mechanism. First is that we can provide impedance requirement of the impedance depends on the capacitance that we can connect. And the second is that how we can change the voltage level, so that it can provide the required path. So, this type of solutions mainly we have focused. Now, in passive solutions this kind of component they are fixed in nature means if the voltage or anything vary with respect to the load condition, input condition or the output condition then we cannot change all this parameter. So that is why we started looking for a solution which can provide required voltage or the impedance level based on the output characteristics or the change in the load and also it can provide us a solution so where we can

actually control all the parameters. Okay, so that is where the active component comes into picture.

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|---|---|
| Key Elements Affecting Switching Charac   | teristics                                 |
| ✤ Gate drive.   |   |
| Parasitic. /  |   |
| Cross-talk between switches.  |   |
| Additional elements in a three-phase system: other phase-legs, heatsink, and moto   | or/cable load.                            |
| Dr. Moumita Das: Assistant Professor, IIT Mandi   | 2   |

So let's see how this is working. So as I have told in the last class, so there are like different types of like a problem which can affect the switching characteristics. So, the problem can come from gate drive, parasitic, crosstalk and additional element. So, they may not create that much problem, but those can also be part of this switching characteristics effect. So, they are phase lag, heat sink and motor or cable load. So, now we are discussing about this crosstalk. So, let us see the active solution which are existing in nature or which can be a possible solution for wide band gap devices for this crosstalk mitigation.

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So, you have already seen this kind of diagram in the last class. So, the circuit which I am showing you, so I am considering the same network. So, one of the legs of the three phases. So, let us say this is phase A. So, where two switches are connected. So, one upper switch. one upper switch and another is lower switch, right? So, now upper switch and lower switch if they are connected in series, so it we have to consider that both are not in turn on condition at the same time. ok?. So, for that we have to provide a sufficient dead gap, so that one switch when it turns off then the other switch will turn on. So those things are taken care of. Now when one switch is turning off or other switch is turning on so during that time the transient due to turn on and turn off can affect the switch which may not be in the working condition or the complementary switch. Okay? So now you have seen that like one solution I have already provided so there the capacitance was connected right? So now here all the components remain same means this Rg H, so Rg H, Rg L, they are the external gate resistances. So, as you can see from this, so this Rg\_L Rg\_L and Rg\_H, so they are external gate resistance, they are connected to the gate drive circuit, external resistance. Now, the capacitance which we are using for this active solution, so they are given as Ca\_H and Ca\_L. So, they are let us say auxiliary capacitance, they are helping for this crosstalk mitigation. Now, these capacitances you have already seen in the passive kind of solution. We are also using this here, but the difference is that we are using two different switches means like with respect to each capacitance there one switch is connected in series with this. As you can see for the upper switch it is Sa\_H, for lower switch it is Sa\_L. So, these two switches Sa\_H and Sa\_L. These are also you can call it as auxiliary switches. So, these switches, helps this capacitor to charge with respect to different voltage level or it can actually charge in the different polarity. So basically what is happening, so when we are connecting these switches based on the switching turn on and turn off condition we can actually regulate this impedance. So, that is why this kind of technique which I am discussing in this particular slide, this is known as gate impedance regulation. So, you can refer this as GIR or gate impedance regulation, right?. So the idea is that, we can regulate the impedance here by using the switches. So the switch which coming into picture are Sa\_H and Sa\_L. Now you can see these switches are connected to the capacitance but there are other switches which are connected to the gate driver network. So you can see so this there are like two switches with respect to upper uh network so that is S1 H and S2\_H and two switches with respect to the lower network S1\_H and s sorry, S1\_L and S2\_L. So, these two switches are connected to the gate driver network and it is having two different voltages. So, one is the positive voltage for upper switch let's say S1\_H and another is the negative voltage S2 H. So, here we have two different potential voltages. So, V1 H and V1\_L, they are positive voltages, right? And then similarly V2\_H and V2\_L, they are negative voltages. So, in this particular solution two different potential voltages are used ok. Now, this switches you can see the normal switches S1\_H, S2\_H, S1\_L and S2\_L. So, they are basically gate driver switches connected to the gate driver network. So, these switches so you can see here S1\_H, S2\_H, then S1\_L, then S2\_L. So now these switches are connected to the gate driver network, in order to provide charging of the capacitor and charging of the input capacitor of the switch. So there are two different capacitor auxiliary capacitor and the input capacitance of the switch. So in different time we may need different switches to charge with respect to required capacitances, means if the switch is on so then if we have to provide positive voltage then S1\_H or S1\_L switches will be ON and then the positive voltage will find the path with respect to that particular switch, let's say S1\_H then external resistance Rg\_H and internal resistance Rg(in) and then through the input capacitance of the gate and that is how the switch will turn on. Right? and then in that time what will happen the capacitance which is connected in the path where basically we are providing turn on and turn off transient path so that is auxiliary capacitance SA\_H or the SA\_L any of the capacitances if you see, so they are connected in series with the switch auxiliary switch and that is actually helping during the turn on time the total capacitance or the net capacitance in that path that will be negligible. Means if we connect only capacitance then whatever capacitance will come, let's say 1 microfarad. So that capacitance will add up with the gate capacitance and that will increase the net capacitance at the input of the switch. And that may affect turn on and turn off duration. But if we are connecting this capacitance in series with any switch or the diode then what will happen the parasitic capacitance of the switch or the diode will be very less so it will be in the pico-farad range so the net capacitance in that part will be in picofarad or less than that. So, that anyway will not affect the gate input impedance. So, that is why this path like for active solution is not creating any problem during the turn on condition. Okay? So, generally this I have already discussed in the passive solution where this capacitance if we connect, although we may have the solution for the problem of high current or the turn off during turn off duration, this can find the path through the capacitance, but it can increase the turn on and turn off duration, but here this problem will not come. So, let us see how the working principle is. So, I will just, so I have divided in different times. it

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So, you can see here. So, this is let us say for there are different subinterval for this active operation. So, let us consider the first subinterval. So, subinterval here it is given as t0 to t1. So, what is happening in this t0 to t1 duration? So in this duration, so the current will, so basically this V2H or the V2L, it will charge the auxiliary capacitances and what will be the charging path? So the charging path will be like this. So, you can see here, so this auxiliary capacitances Ca\_H and Ca\_L are pre-charged through body diodes of the switches, body diodes so this body diodes body Sa\_H and Sa\_L, Okay? So these capacitances are pre-charged now you can see from the direction of the current this pre-charge voltage will be negative means it is charging from v to h and through this body diode of the Sa\_H and the internal resistance and then switch Sa sorry S2\_H, so this is the loop which is helping to charge this capacitances Ca\_H and Ca\_L will be negative. And it will complete the precharging at the end of this particular subinterval. Okay. So, now this is with respect to the main main function of this particular subinterval to charge these capacitances. Now, if we consider subinterval 2, then in the subinterval 2 what is happening? So, basically this is for t1 to t2 duration.

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So, you can see here. So, this is given here. So here in this particular duration, so what is happening initialization is complete. So, now the lower switch we are considering lower switch turning on of the lower switch. Lower switch at the end of this particular sub interval means at t2 the lower switch starts to turn on. Okay? So, now this switch will be turning on at the end of sub interval. So, we have given some, this particular sub interval it actually completes this initialization. So, like in the first interval, first sub interval, so their initialization started and it should complete by this sub interval. Okay?

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Now, next is that, so here the lower switch is turning ON. So, this turning on signal provided here, so you can see here, this is the signal which is given to the gate of the lower switch. So, this particular signal you can actually see here. Now, upper switch is not on in this condition.

Now, what will happen? In this case, lower switch, now this lower switch how it will be turning on? As I told you earlier, so basically the current from V1 L, so this current from let's say V1\_L, it will flow through this S1\_L through the gate resistance and the internal resistance of the switch. Yes so the current path you can see here for the lower switch, in this case and in this case what will happen as the switch is turning on, the same turn on transient will affect the upper switch, so then what will happen due to the voltage high voltage in the upper switch or whatever voltage will come across the upper switch that will cause current to flow through the miller capacitance of the upper switch. So, what is the current path? So, basically the current path as you know, so this generally flows through the miller capacitance. So, let me just use the thicker line so that it will be highlighted properly. So, this through this capacitance then it will find the path through this internal resistance of the switch. and then through this capacitance, aH, so the auxiliary capacitance it will flow okay? Now this auxiliary capacitance as you can see, here so in this case, in this case this auxiliary capacitance it will provide the low impedance path and the current will flow through the auxiliary capacitance to the device and then it will not because you know it is not flowing through the gate driver part so that is why it will not turn on the upper switch. So upper switch is protected during this crosstalk turn on condition. Now the lower switch if you see here. So this is with respect to the upper switch. Now the lower switch current path already I have shown, I hope it is visible to you. So this is the current path, so I am just highlighting it again using the thicker line, so this is the current path for the lower switch. Now you can see this Cgs\_L. So basically this Cgs So this is connected across this Ca\_L and the switch. But as I told you earlier, this particular branch will have net capacitance in picofarad, so this particular branch, this particular branch is in picofarad, right? It will be much much smaller so this Cgs\_L, here it will be much much larger than that of the net capacitance coming Ca L. That will be coming in parallel with the either switch or the diode capacitance and that will be very small. So that will be coming in parallel with the, so it will be having capacitance of Sa L So, that is why this Cgs L will be much much higher. So, this line will not impact the turn ON condition. So, the turn on condition, then in this case crosstalk is eliminated. So, the net, so basically the main outcome from this particular subinterval is that crosstalk of turn on. is suppressed. So, basically there are two problem comes during the turn on condition. First is that the upper switch can turn on if we don't have the protection, protection can be anything that can. So, here we are using the impedance kind of protection. So, but we are regulating the impedance. So, now this and another thing is that it can increase the turn on time. So, turn on time we are not increasing by considering that switch capacitance which will be much much lesser value, the net effect will be less and also we are providing the capacitance path which is helping the upper switch to remain in the off condition during the turn on of the lower switch. So, this is the conclusion of this particular sub interval.

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Now, next move to the sub interval t3 to t4. So, now this switch is on. So, basically lower switch the on condition we have seen. So, now let's consider what happens in the turn off condition. So, during turn off condition, so what we have to consider? Here is that so basically this capacitance, so you have seen here the previously this capacitance initially it was charged to the negative voltage, but now the current was flowing in this particular sub interval, the previous sub interval in the positive direction. So the net effect will cancel each other. So basically whatever voltage negative voltage was there in the capacitance it will cancel out with respect to the positive charge in the capacitance. Now what we have to do in this particular sub interval, we have to charge this capacitance again so basically, this particular sub interval, it is helping the capacitance to charge. It is same as the previous step where we have actually used this particular loop for charging, okay so now same loop we are using for charging, okay? Now here another thing is that in this case the current is flowing through the gate capacitance also. So, the gate capacitance it is also charging in the negative polarity, okay? So, this step here the all the switching condition it remains this step same as the previous sub intervals. remain same. So, this is same for the lower switch as previous subinterval was subinterval 3, here it is subinterval 4 as subinterval 3. Now, so this negative power supply as you as I have shown in the upper switch, so the negative the supply V2\_H which is basically negative supply here. So, as you have seen in the previous case, so there was some positive voltage will be appearing across Ca\_H and Cgs\_H. Although we have pre-charged this capacitance to negative value. So, due to this current, because you know we are considering this current may be very high due to CEdv/dt. This Cgd\_H, it will be very low. and this dv/dt it will be very high because you know this is turning off so the voltage should go from 0 to Vds. Vds if it is let's say 1000 volts so then this current will be very high and it may cause the voltage across these two capacitances this Ca\_h and Cgs\_H to become positive means like although it will balance out the negative voltage which was there in the capacitance and still there will be some voltage which will be appearing across the capacitance. So it will cause positive voltage to appear across this capacitance now what we have seen in the sub interval one, we have precharged this auxiliary capacitance to negative voltage. Now in this particular step what is happening so this V2\_H is

helping this Ca\_H auxiliary capacitance to go back to pre-charged value. So, one thing is that if it is having zero voltage then immediately it will charge to pre-charged value which will be equal to V2H. So, basically in normal condition this VCa\_H should be equal to V2\_H. Now, because the current in this particular capacitance was in the opposite direction, so the voltage will be less than V2H. It can be either 0 or positive any value. So, in this step what is happening? Lower switch will be operating as the same condition in subinterval 3, but this upper switch capacitance it will go back to the pre-charged condition. And similarly, the gate capacitance Cgsh, it will also have some voltage due to the current flowing through it. So, it will also go back to the previous condition. So, that it will be ready for the next cycle. Okay? So, that is why in this particular step, the switch S2\_H is on and through this switch, internal resistance either these capacitances are discharging or it is probably the auxiliary capacitor is charging. So, this is the thing is happening in this particular subinterval. Now, at the end of this particular subinterval means at t4 the lower switch starts to turn off. So, turn on transient you have seen how it is mitigated.

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Now we will see what is happening during the turn off condition. So basically turn off, so, how it is happening? So, when this lower switch is turning off as you can see the signal which is given here. So, this is now it is in off it is going to the off from on. So, then in this case in the upper switch Sa\_H will be in on condition. okay. Now Sa\_H is on then how the current will flow so as you have seen if the device turns off the negative voltage generally appears across the upper switch. Right? So the problem was that if the negative voltage go beyond the negative voltage rating of the upper switch then it will destroy the device and the reliability. So that is why in this case what is happening the Turn off path is provided through these capacitances and the capacitance current path will be equal to this. So you can see here so there is a current path through this switch and the capacitance and then it will go also through the capacitances here.

Okay. So now this capacitance polarity is negative and then basically the current Sa\_H is on so the current it is flowing through this capacitance in this particular direction. So to due to this what is happening, so basically, so, that is why, so this path, this particular path current direction will be restricted. So, the current in the gate driver, so basically C2\_H will not be impacted. So, only the low impedance path, through the low impedance path the current will flow and then it will not affect the lower voltage level of the upper switch. So, then it will also be protected during the turn off condition. So, at the end of this sub interval, turn off. Okay? Now turn off of the switches complete in this particular subinterval. So, now next is that turn off part is done. Now, what we have to do? We have to make sure that all the condition remain same as the first subinterval. So, that the switch will be ready again to turn on.

So, you can see here.

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So, basically in this particular subinterval full turn off of lower switch completes. Sa\_H is OFF and Ca\_H is disconnected. okay now C2H starts CAH starts to charge. So, in this case what is happening? The current is flowing through, so, basically this S2\_H Rg\_H through the gate capacitance. So, basically Cgs\_H will be charged from this switch, so body diode and then V2\_H. Let me just write down. that Cgs\_H discharges. So, then it will be discharges through this internal resistance Rg\_H. So you can see so basically what happened in the previous step, so this capacitance was charged in the opposite direction means the voltage across this gate capacitance of the upper switch it was negative, right? so basically, you can see here with respect to this capacitance current the voltage polarity will be negative now this capacitance should discharge in order to make this circuit equivalent to the sub interval 1. So, in the sub interval 1, what was the case? In the sub interval 1, so this capacitance were in the pre-

charged condition. Now due to turn off the some current was flowing through this capacitance gate capacitance of the upper switch. Now we have to make sure that this capacitance is completely in the previous condition or the capacitance voltage or the charge in the capacitance will become zero at the end of the complete interval. So, this is what is happening in this sub interval 6. So, at the end of this sub interval, so this gate impedance regulation based crosstalk mitigation completes. So, we can as you can see, we can regulate the impedance based on our requirement or based on the turn on and turn off transient in this particular method. So this method is very useful and also it provides active kind of solution. So now another method with respect to this active solution is gate voltage control or the GVC. So I will be discussing about that GVC in the next lecture. Thank you.