Power Electronics with Wide Bandgap Devices
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Lecture-13
CROSS TALK CONSIDERATION

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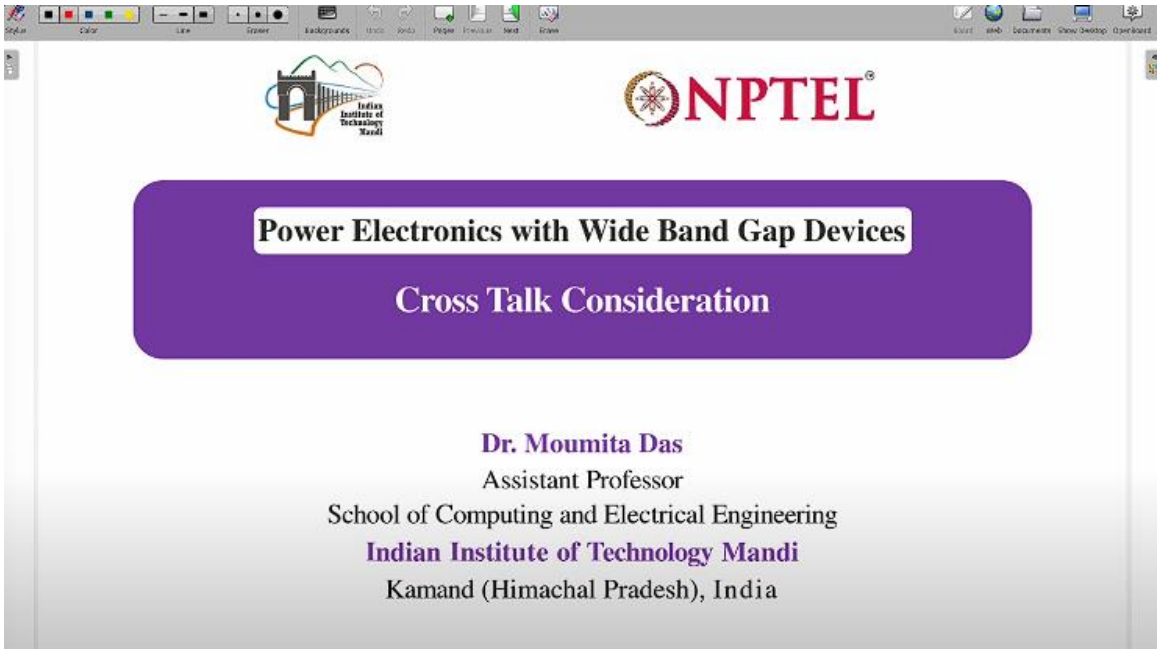

Welcome to the course on power electronics with wide band gap devices. In the last lecture, I have discussed about different protection techniques for DUTs and DPTs. So the protection techniques which are available for the devices which may be new or may not be new that already I have discussed. Now those discussion was based on the DPT configuration where we have considered it is an ideal network. So if we have to consider practical circuit, so there are different other factors we need to consider. So what are those factors and how those factors are going to affect the operation of the circuit that I am going to discuss today.

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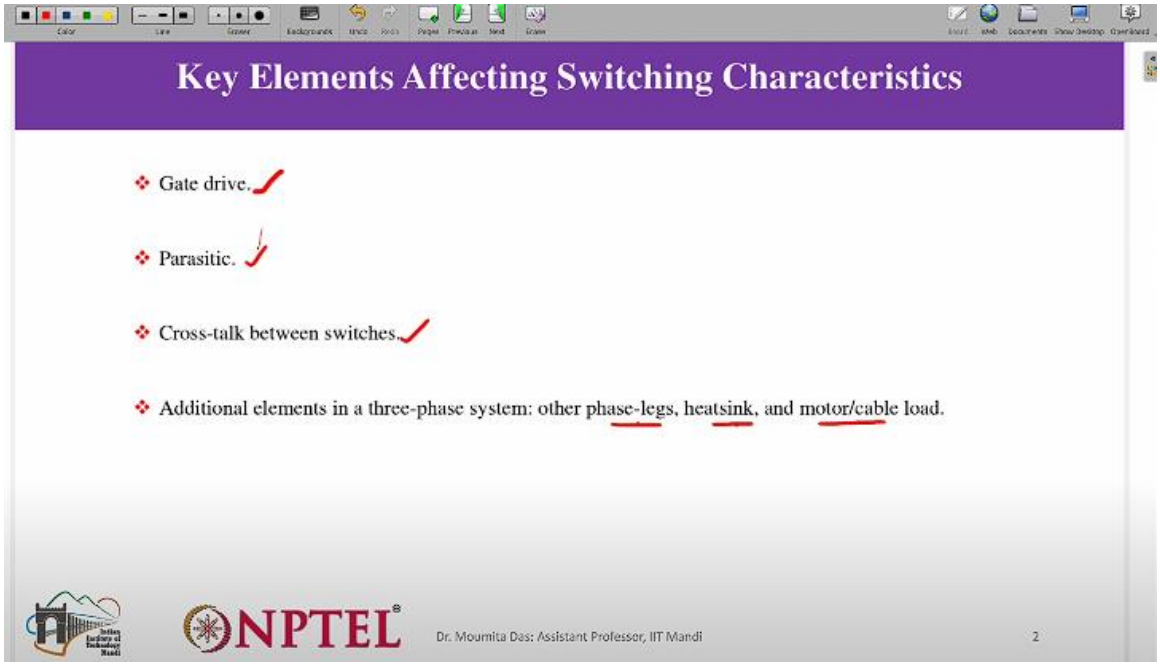

So whenever we consider any switching network, so let's consider DPT. So generally there will be either two switches or one diode and one switch. So if there are two different switches, so then what will happen? Switching of one particular switch either upper switch or the lower switch will affect the another switch. So this effect generally comes due to different factors. So, the different factors here I have listed. So, first is the gate drive. So, first parameter of the gate drive. So, the gate drive related parameter basically can affect the switching of the network or any circuit. So, second is the parasitics. So, parasitics whatever will come in the path of switch or in the path of gate drive that will also affect the operation. So, third is the cross talk between the switches. Cross talk means if one switches is switching on or off that will affect the other switches. So, that is known as the cross talk of between the two switches. So, that will also affect the operation. And the fourth is that additional element in the three phase system other phase legs, then heat sink, motor or cable load. So, this phase legs, heat sink, motor or cable load, these are also the parameter which will affect the operation. But these parameters effect is not that significant as the effect comes from the gate drive parasitics and crosstalks. So, today I am going to discuss in details about the crosstalk related problem. So, the other parameters I will be discussing in the next lectures.

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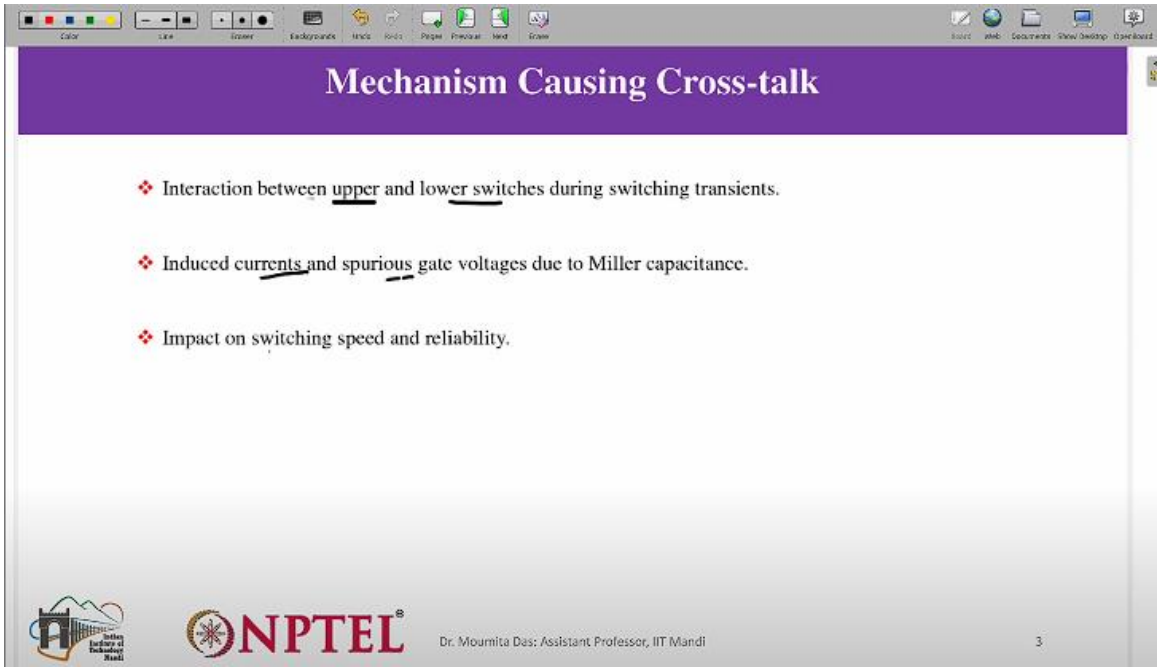

So, you can see, so what is the basically cause of this crosstalk? So, whenever there is a interaction between the upper and the lower switches during switching transient, so that will affect the operation of the converter. Operation means either it can increase the losses, it can increase the transient current, voltage and also it can actually cause the turn on of the switch during the turn off condition. So basically false turn on of the switches. So those can comes from the crosstalk. So interaction between the upper and the lower switches during the switching transient causes crosstalk, and induced current and spurious gate voltages due to Miller capacitance that will cause crosstalk problem and this will impact switching speed and the reliability.

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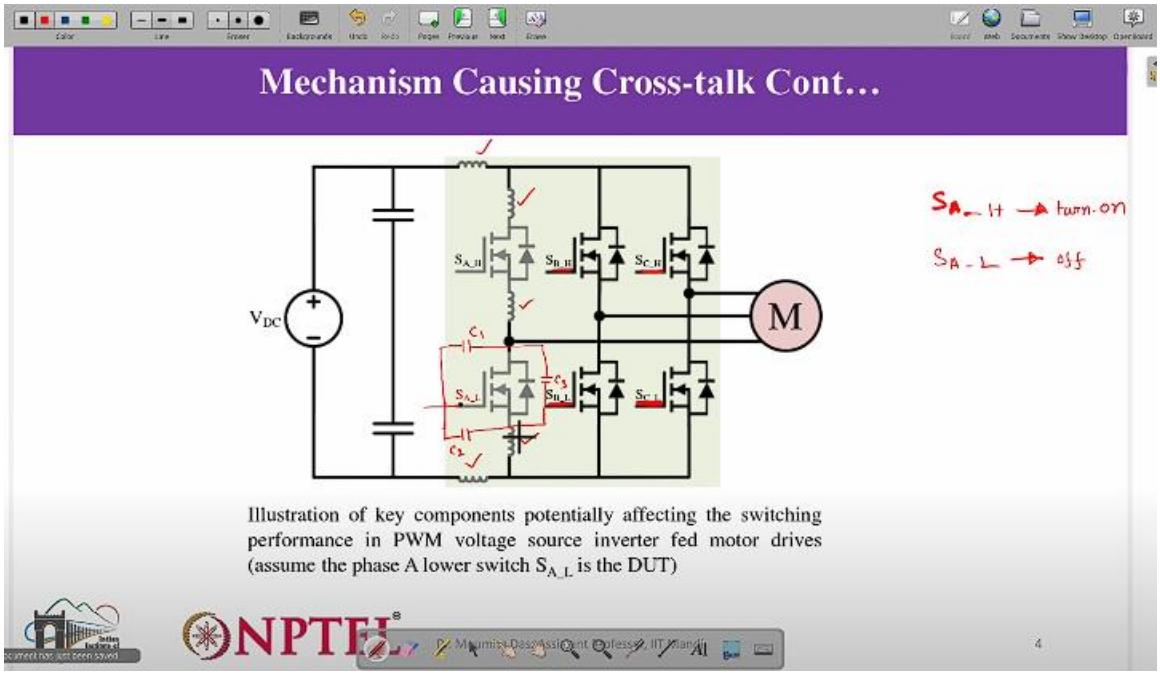

So let's see in details how this is coming into picture. So you can see this particular network, so in this particular network, so this is basically three-phase inverter is shown in this diagram, so this circuit diagram you can see so two switches in one leg are connected. So, we will just consider any particular any leg or any DPT network where two switches are connected in one leg and then we will try to analyze the problem due to the crosstalk. So, you can see here so the switches connected in this particular leg is so basically, phase A it is denoted as SA high and and SA low. Similarly with respect to phase B, SB high and then SB low. Similarly, with respect to C phase, SC high and SC low. It is connected to the motor terminal. So, now the switching of any leg due to either upper switch or the lower switch, it will affect the complementary switch connected to it. Means, if we consider phase A, so then there are two different switches. SA SA high and SA low. Now when switch high is turning ON, so then what is happening? SAL will either be in turned off condition or it is turning off. So generally there will be some dead time. So let let's say this switch is in off condition. So, due to this turn on, so then what will happen? Then the transient whatever will come in that particular path. So, one of the transients is shown here which is inductance which is coming in series of that particular switch. So, you can see here in series of these switches there are different inductances are coming. So, these inductances will come in series with the parasitic capacitances. What are the parasitic capacitances? So, that already you know. So, three different capacitances will be there with respect to any particular switch. First is a Miller capacitance which will be connected between the gate terminal and the drain terminal of the MOSFET. Second is the gate capacitance which will be connected between gate terminal and the source terminal of the MOSFET and the third one is the output capacitance that will be connected between the drain terminal and the source terminal. Now you can see so there are three different capacitances will be there with respect to each switch. So, means with respect to upper switch also this parasitic components will also be there and same will come for the lower switch as I have shown in this particular diagram. So, now this will come in series with different parasitic inductances and this inductance and capacitance combination will cause the problem during the turn on or turn

off condition. So, what are the problems are coming? So, let us analyze that in details.

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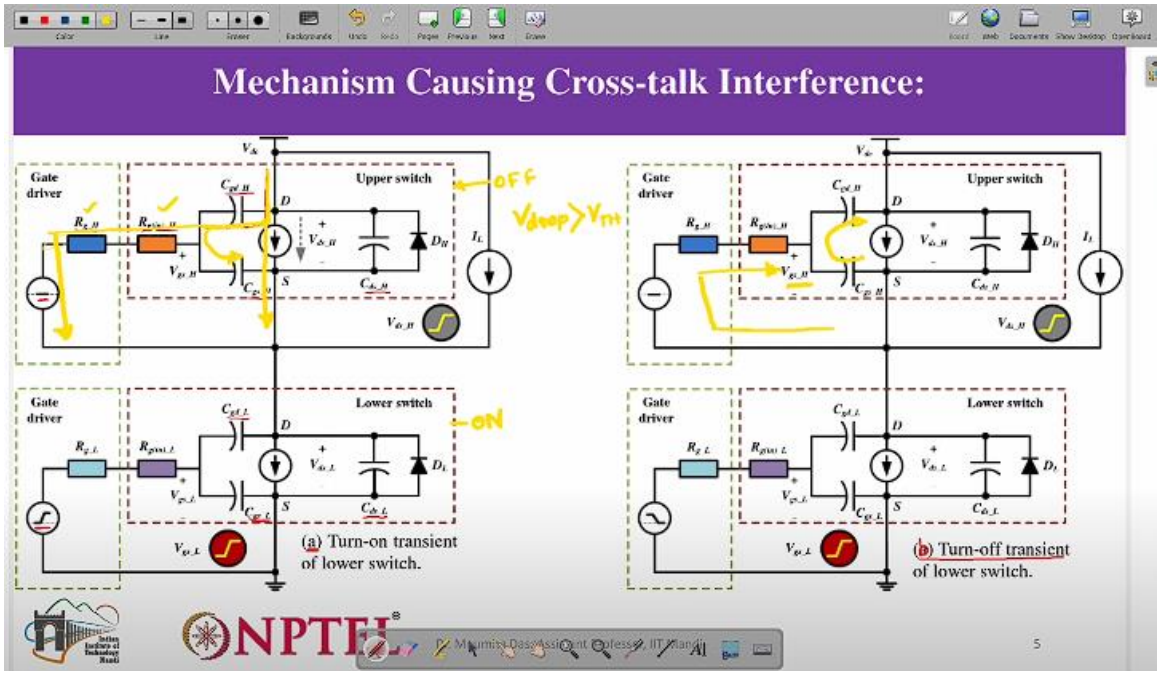

So, you can see here, so two different diagrams are shown. So, one I will just discuss with respect to either turn on or turn off condition. So, let us say, the first one, so this one, the first one figure A here, it is with respect to turn on of the lower switch. You can see here, so the lower switch is shown in the dotted line. So you can see in this particular network, so gate driver is shown here in the green dotted block and the remaining this brown dotted block, it is showing lower switch. And there are different parasitic capacitances are shown with respect to the lower switch. So you can see here with respect to gate driver, so only two components are shown. So gate drive voltage and the gate resistance. So you can see here RGL is the gate resistance which is connected externally. And now there is another gate resistance which is internal to the device. It is shown within the dotted block of the device. So RGNL, L for the lower switch. So, now this VGSL it is coming across the gate to source terminal of the device and then CGDL is the miller capacitance of the lower switch, CGSL is the gate capacitance of the lower switch and CDSL is the output capacitance of the lower switch. So, these three capacitance already I have discussed in the previous slide. So, similar capacitance you can also see for the upper switches. So, you can see different components of the upper switches. It is similar to the lower switch, so gate driver signal it is having input which is coming from the gate driver so either it can be zero negative or positive, depending upon the polarity which you are giving for the particular switch. So if it is silicon, silicon carbide, then generally positive voltages are given but also it is advisable to give negative voltage during the turn off condition to silicon carbide and GaN devices. So, depending on that during turn on or off condition either it will be positive, negative or zero. So here in this particular network, so in this A figure, we are discussing turn on of the lower switch. Means we are providing positive gate voltage, here it is shown positive gate voltage to the lower switch and upper switch it is in off condition that

means 0. So here it is 0 voltage is given to the upper switch. So, similarly all the resistances similar to lower switch is connected. So, external gate resistance is shown here with respect to Rg high and then internal resistance with respect to device it is shown Rg in H and similarly the different parasitic capacitances with respect to miller and gate and output capacitances are shown here. Now the device is in off condition. So the lower switch is turning on, so if the lower switch is turning on, so then what will happen, the upper switch it should be off. If it is off then the voltage across the upper switch it will be equal to Vds or the voltage maximum voltage which the device supposed to handle during the turn off condition. So due to that voltage what will happen since this miller capacitance is connected, so there will be a current path, so how this current path looks like? So this current will come from input DC to this miller capacitance, so let me draw it in different color so then it will be easily visible. Hopefully it is visible to you. So, let me increase the thickness. So this current is going to the gate terminal. So, one is going to the gate terminal. So, now upper switch is off. So, basically this particular switch in this condition it is it is off. But there is a current which is flowing through the gate resistance to the gate. This is due to the miller capacitance and this will come during the turn off condition. Now, due to this particular current path, so there will be voltage drop across the resistances. Gate resistances. So you can see here two different resistances, due to the current there will be voltage drop. Now if this voltage drop is more than the threshold voltage of the device, then the device will turn on. So the voltage drop during this condition, if it is more than Vth, So then the device will turn on. So as you know for silicon carbide and GaN, so the threshold voltage levels especially for GaN, it is very low. So then if this voltage is very high it will immediately turn on the device and the device is if it is on so basically it is false turn on condition, this is not something which we desire. So then there will be a current path through the device And it will go from upper switch to the lower switch. So this current will be very high. So these two you know the lower switch it is already on, but upper switch it is turned on due to this parasitics. And this will cause very high current flowing through this particular leg. So if we consider this leg is equivalent to the leg of phase A. So then very high current will be flowing through that leg. So, this is known as crosstalk. Because of the lower switch and upper switch interaction, this kind of problem is happening. So, that is why it is known as crosstalk problem. So, this is during the turn on transient, ok. Now, turn on transient you can understand, ok fine there is a problem due to miller capacitance during the turn on transient. Now, what will happen during the turn off condition? So, the next one, so here this is figure B. So, this is not A, this is B. So, this shows the turn off transient. So, now turn off transient means the device of the lower switch, it is off, turning off. So, then if the device is turning off, so then okay fine, so there will be no problem then. But what is happening, due to the lower switch turning off in that case very high voltage will be appearing across lower switch. Right? So this will again cause the current to flow through the through actually in the opposite direction, means in this case the current was in this particular direction. Now, here it will be exactly opposite, it will be like this and this will go like this, Ok? during the turn off of the lower switch. Now, if this kind of situation is happening, then anyway, since the current is in the negative direction opposite direction, so obviously the voltage drop across the gate it will be in the negative voltage. so if it is negative, so probably there will be no problem generally there will be no problem of short circuit current or very high current. But there will be a problem of negative voltage means the silicon carbide, GaN or silicon each is having some negative

voltage handling capability. Means the negative voltage for GaN as you have seen probably minus 4 or minus 6 volts maximum you can give. Or for during transient condition it will be much higher. Let's say minus 10 or minus 20 volts. For silicon carbide also there is a limit of minus 6 volts around. For silicon also there is a limit. So, if the voltage drop across the gate, this gate terminal if it is lower than the minimum voltage minimum negative voltage which we can provide in the gate during the transient condition then it will actually destroy the device. So, it will cause the reliability problem of the device. So, during both the condition turn on and turn off. Whatever you are seeing it is due to the switching effect. So switching of one particular switch will affect other switch in that particular link. So, DPT is also having same type of configuration. If you are considering diode in place of switch for DPT operation then there is no problem. But if you are considering two different switches then you have to modify the circuit operation in order to avoid this kind of problem. Ok? So, these two problems comes under crosstalk interference. So, interference of two different switches causes this kind of problem. Okay?

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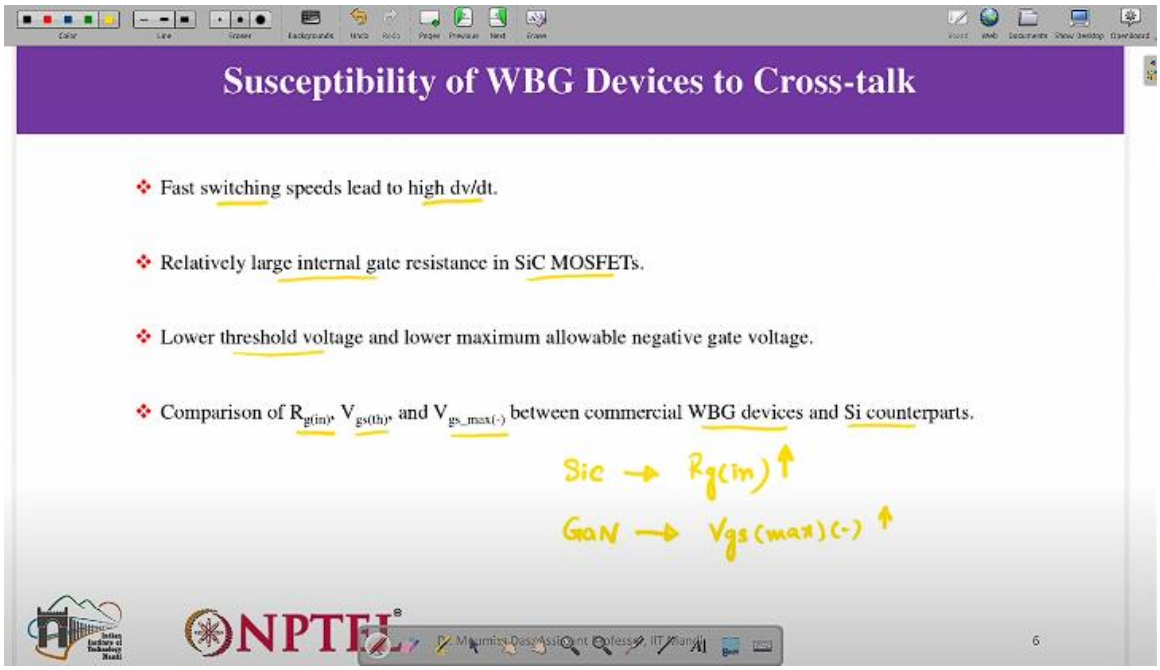

Now, these problems, why we need to bother about? Because these problems are always there. For silicon devices also this kind of problems are there for long time. But why we have to bother now for wide band gap devices? Now for wide band gap devices, this problem will be much higher due to fast switching speed. So, first switching speed then what will be the problem? If the switching speed is very high, so the problem related to high dv/dt will be there. So, means the dv/dt problem in wire band cap devices will be much higher than that of the silicon device which is operating at much lower speed. Okay? So, now the second thing is that relatively large internal gate resistance in silicon carbide MOSFET. So there are two different resistances you can see here, so one with respect to the device which is known as internal resistance, we cannot do anything to that particular resistance that will always be there, whatever we can vary So, that is coming that is actually connected externally right. So, if the

device internal resistance is very high. So, that will increase the impedance of that particular gate loop. So, then that will cause problem with respect to crosstalk. If you know like if the resistance is very high then what will happen the voltage drop with respect to particular current that will also be higher. Again like that will cause like higher voltage across the gate during the turn on transient. So, that is why this problem will be higher in such devices where gate resistance internal gate resistance is high. So, that in case of silicon or carbide MOSFET, it is higher than that of the silicon. So, that is why this problem will be higher. Then the third problem comes with respect to the lower threshold voltage. As I told you for GaN devices threshold voltage is much lower than that of the silicon or silicon carbide. So it is around 1.5 volts. So if the threshold voltage is low again there will be high chance for transient voltage gate voltage to reach that level. So, that is why it is always advisable to keep the turn off voltage across the switch terminal during the turn off condition it is negative for GaN devices. So, that at least there will be some gap between the threshold voltage and the turn off voltage. If it is 0 then gap will be much less. So, that is why this lower threshold voltage causes another increasing problem for this crosstalk. So now, you can see you can actually see if you try to go through the data sheet of this Rg(in) Rg(in) threshold Vgs maximum for commercial wide bandgap device and silicon then you will be able to see Rg(in) is much higher for silicon carbide device. For silicon carbide device Rg(in) is comparatively high. Okay, now for like gallium nitride device, gallium nitride this Vgs maximum in negative, so that will be comparatively higher than that of the silicon carbide. Okay and then Vgs(th) it is much lower in case of GaN. So you can just see the comparison part. So you can you will get the idea how each component is different with respect to different devices. Okay?

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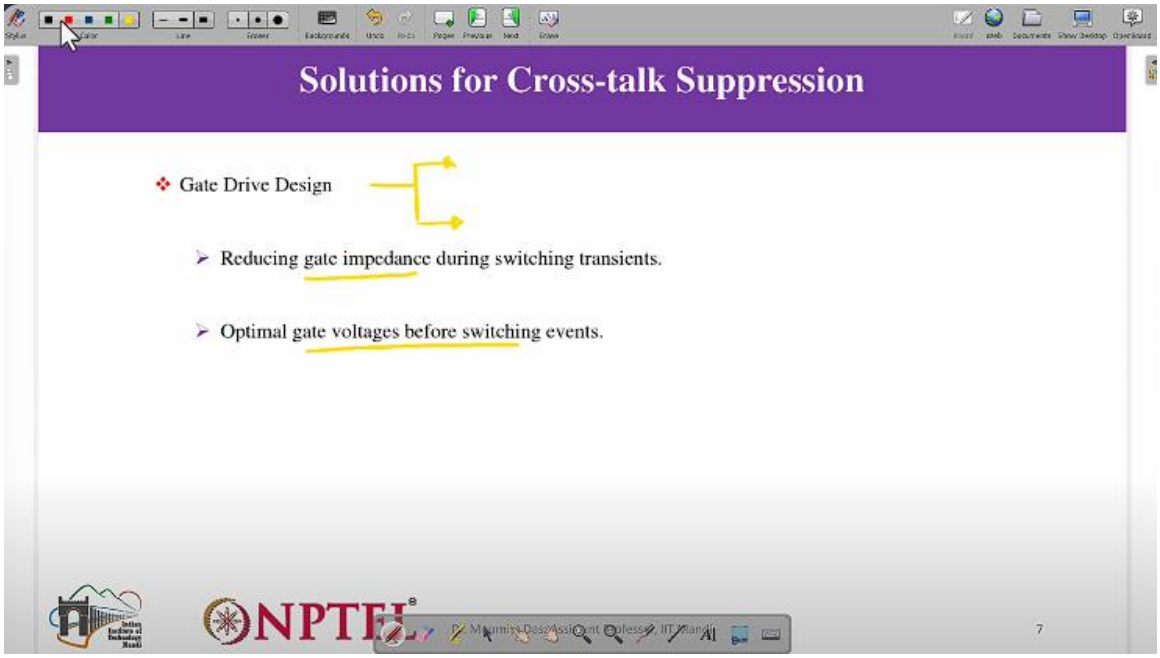

Now next is the, so then what can be the solution? So if this is the case that we have different problem during the switching, till now I haven't considered the parasitic inductance.

That anyway I will be considering later in the later stage. So now we have only considered the parasitic capacitances and that is causing this kind of problem and those capacitances are not external to the device, they are internal to the device. Now what we can do in order to reduce this problem, we can focus on the gate driver part. So similar thing which i have already discussed so like gate driver design we have to modify such a way that we can reduce this kind of problem. So what we have to reduce so we have to reduce gate impedance, so basically impedance whatever is coming in the gate loop so that we have to reduce, so that that false turn on condition will not happen. Now another thing comes into picture is that optimal gate voltages before switching events. So we can actually see that what should be the optimal voltage we can provide to the switches. It can be 0, negative or so whatever it is possible to provide so that we can provide. Okay. So this has two different solutions. So either by using passive mode or by using active mode. So now gate driver is also having two different like this design is having solution with respect to two different part. One is with respect to passive and one is with respect to active. So, we will see the differences of passive and active.

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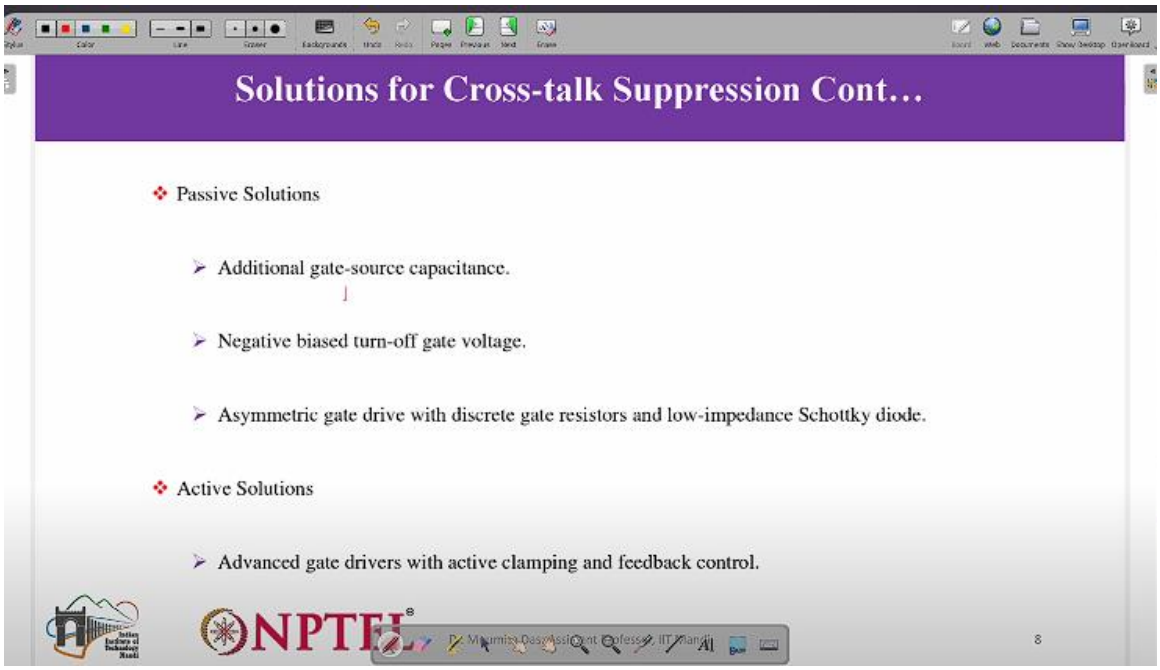

So, in passive solutions as you know there will be different passive components and with respect to that we can see how we can optimize the operation to reduce the crosstalk problem. So, there are actually three different methods we can consider in the passive solution. One is that by adding gate to source capacitance. There is already a gate source capacitance but we can add additional gate source capacitance that can actually reduce the problem somewhat, so basically it will reduce the impedance of that particular loop and then what will happen that will provide a path for current to flow. So, then the gate voltage will not increase during the turn on transient. But this has disadvantage, this also has disadvantage. I will tell you about disadvantage later when I will be discussing the detailed circuit. So, and second is the negative turn off voltage. So, negative turn off voltage we can apply instead of 0. So, that we can provide them like some gap gap between the threshold voltage and the turn off voltage. And the

asymmetric gate drive. Means we can provide two different resistances during the turn on and the turn off condition. Okay? So, these are the different solution which comes under the passive solution. Active solution what it gives? It provides the advanced gate drive kind of solution by using active component in the path. So in the passive solution whatever solution is provided that by using passive component. But active solution will have some active component. It can have some BJT in the path which can probably give some control by using feedback. So that will provide us optimum kind of solution for this kind of problem.

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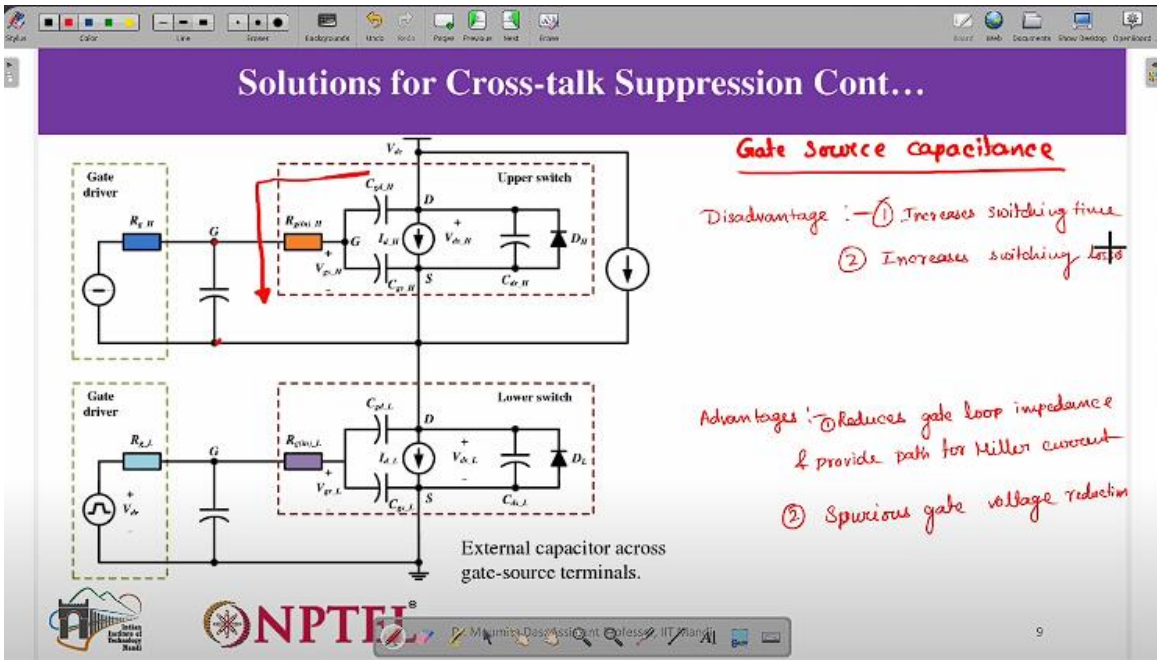

Okay, so let's start with the passive solutions. So passive solutions you can see so this the first thing I can discuss here so is the gate source by adding gate source capacitance. So you can see this is with respect to let's say gate source capacitance. Now you can already see there is a gate to source capacitance already connected here. But in addition to this there can be additional capacitance can be connected. So the additional capacitance since it is like Rg in H so then it will be connected between gate and source terminal. So then what will happen due to this connection, this current whatever current will be coming from the miller capacitance, this particular current will be having path through this capacitance. Then it will actually short the gate to source terminal. So there will be voltage drop will be equal to zero ideally. So then this will not turn on the device. In this case what will happen due to this capacitance, the additional capacitance in this path between the gate to source, it will increase the turn on time. So again like it will affect the switching operation of the converter. It will increase the time and it will increase the loss. So this is the disadvantage. So advantage is that it can provide path for the current. Disadvantage is that it can increase. So the disadvantage for this particular method is that, so, disadvantage is the, so let me write advantages also. So, the main advantage is that it reduces gate loop impedance. And provide path for Miller current. Okay? So whatever current will be coming through this Miller capacitance. And disadvantage in this particular case is that, so, this will reduce spurious gate voltage reduction. It is turn off time, turn on time or

the switching time increases. switching time and second is the increases switching losses. So, these are the advantages and disadvantages of this particular method. Now, let us go to the second one. So, this is with respect to the negative bias turn off gate voltage.

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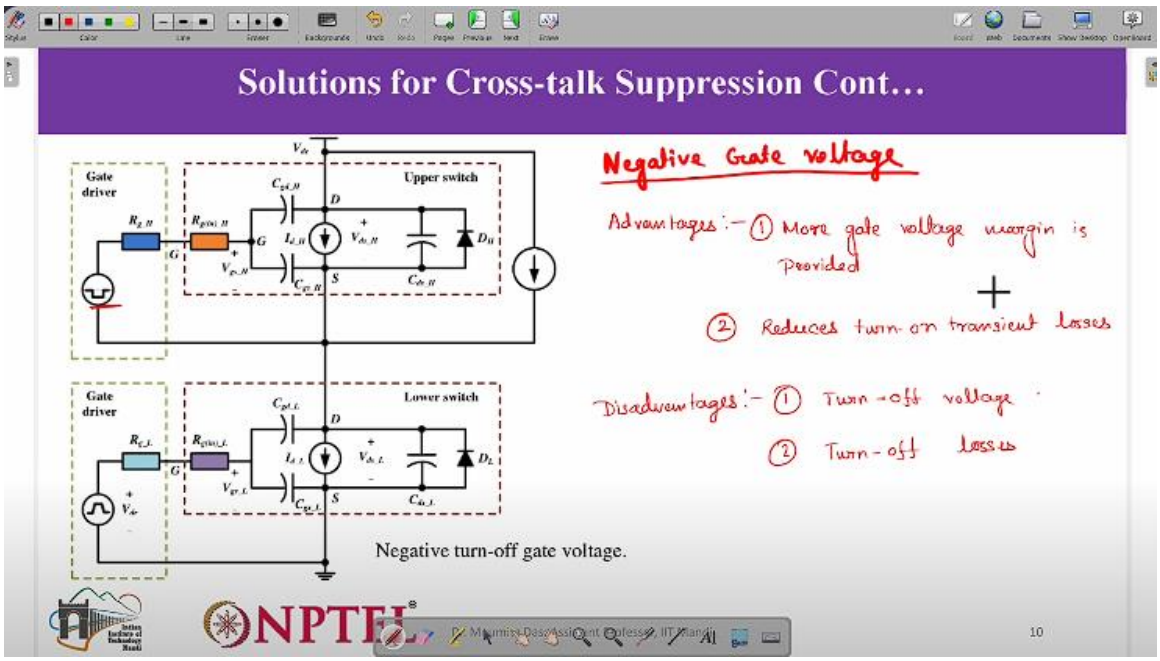

So, this we can consider with respect to, okay? So now, you can see here, so this particular voltage of the upper switch, it is kept here. In this particular case, here it is instead of 0, it is negative here. In the previous case, this was 0, right? So, instead of 0, in this solution, it is given as negative. So, now if the negative voltage is given, so what will happen? Let us say negative voltage is minus 2 volts. Now, voltage drop across this external resistance, is coming around 2 volts plus 2 volts. So, then what will happen minus 2 and plus 2 it will cancel each other then the voltage net voltage which will be coming across the gate to source terminal that will be 0. Now, if we keep only 0 then the plus 2 volts will be coming across the gate to source voltage and if the threshold voltage is less than plus 2 so then it will turn on the device. So that is why negative gate voltage will help to provide some safety margin it will actually help to reduce the false turn on kind of problem. So this is another solution it comes under passive type of solution. So let's see what are the advantages and disadvantages of this particular solution. So here I am writing advantages first so so the gate margin more gate margin is provided voltage, this reduces disadvantages. So, now what is happening? So, one advantages you know already the more gate voltage margin obviously the margin is provided and reduces turn on transient losses. Now, disadvantage is that it is having so basically negative gate voltage is provided. So, during the turn off time since this voltage level we have to see whether it is in the safety margin or not. So, that kind of problem can occur. So, one problem come from the turn off transient voltage can cause this negative gate voltage to go beyond the limit ok? This is one of the problems which can be actually found during the turn off condition, ok?. Now, also if the negative gate voltage is provided, so the losses, so turn on transient losses will be less, but the turn off transient losses will be more in this particular case, ok? Now, that is what

we have to optimize, how much voltage we can keep, so that we are not increasing the problem during the turn off condition. So, here we will have advantages, so turn off voltage and turn off loss, these two problem will be there here in this particular case we have advantage during the turn on conditio. Similarly in the previous previous case we have disadvantage during the switching time. So basically switching loss will increase here we can reduce that during the turn on condition but turn off condition we cannot optimize. So that is why we have to select the optimize negative gate voltage for this kind of solution.

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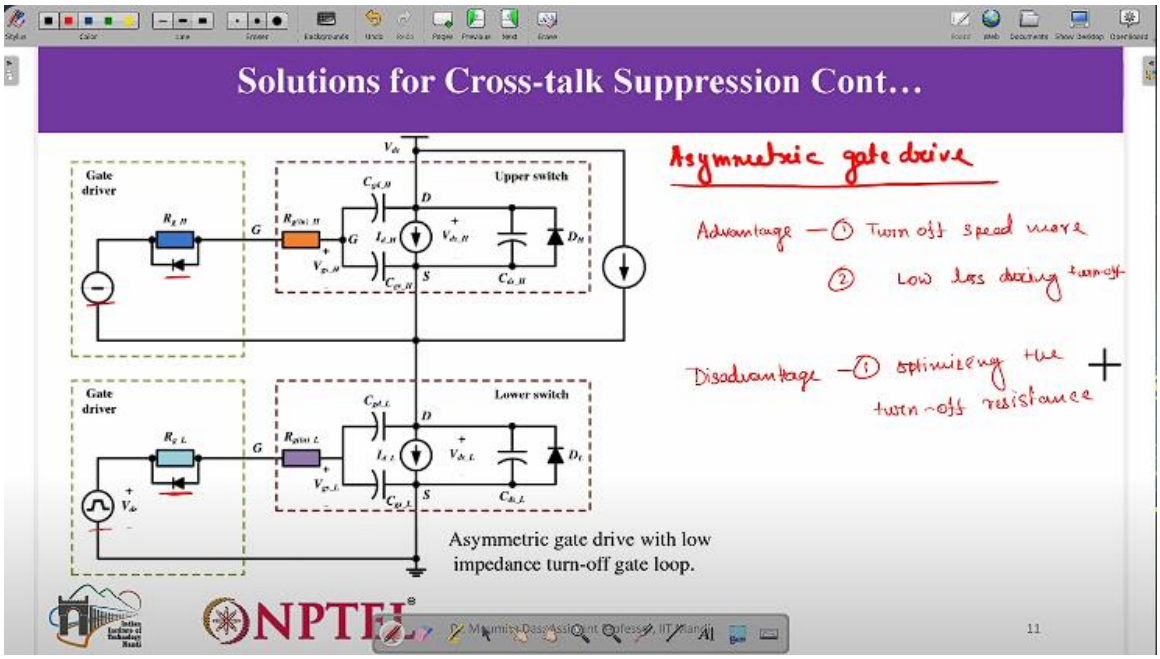

Now, the third problem is the with respect to asymmetric gate drive. So, asymmetric gate drive what does that mean? So, symmetric you understand, so basically both time, so some components which will be common for the turn on and turn off operation. But asymmetric means what? So, here you can see upper switch is having zero voltage, lower switch is having some gate voltage, positive gate voltage. Here one diode is connected, here in this case you can see both the cases upper and lower switch, one diode is connected across the external gate resistance. So if the diode is connected then what is happening during the turn off condition, so the direction of the diode you can see it is providing current path during the turn off condition. So during turn off condition it is actually bypassing this external resistance, means whatever internal resistance is there in the switch that we cannot do anything. So that internal resistance will remain same but external resistance we can optimize, so we can provide the diode so that it can bypass that so it can actually increase the turn off speed, and also it can reduces the losses during the turn off time. So that is what we can get from this asymmetric gate drive. So during turn on time the resistances which will be provided that will be more in in series with gate and during the turn off time the resistance which will be provided that will be less because we are bypassing using the diode. So in this case since we are bypassing, we cannot actually provide any optimum kind of resistance, means let's say during turn off condition instead of bypassing the complete resistance, if we want to provide some lower

resistance that we cannot provide. So the advantage in this particular case, so advantage will be there, turn off speed will be more. Low loss during turn off. Disadvantage will be there, we cannot optimize this turn off resistance. So this is the problem of this asymmetric type of gate drive and again like the kind of characteristics we will be getting during the turn on time it will be different than the in the turn off time. So these are the different solutions which is provided with respect to the passive solution and each is having disadvantage with respect to switching duration either during turn on some problem will be there or turn off some problem will be there. And during turn on and turn off operations will not be equal. So because you know either we are bypassing something during turn on or like adding something during turn off condition, So basically switching event in turn on and turn off event turn off durations will be different. So this kind of problem can be possible to give solution using active kind of gate driver.

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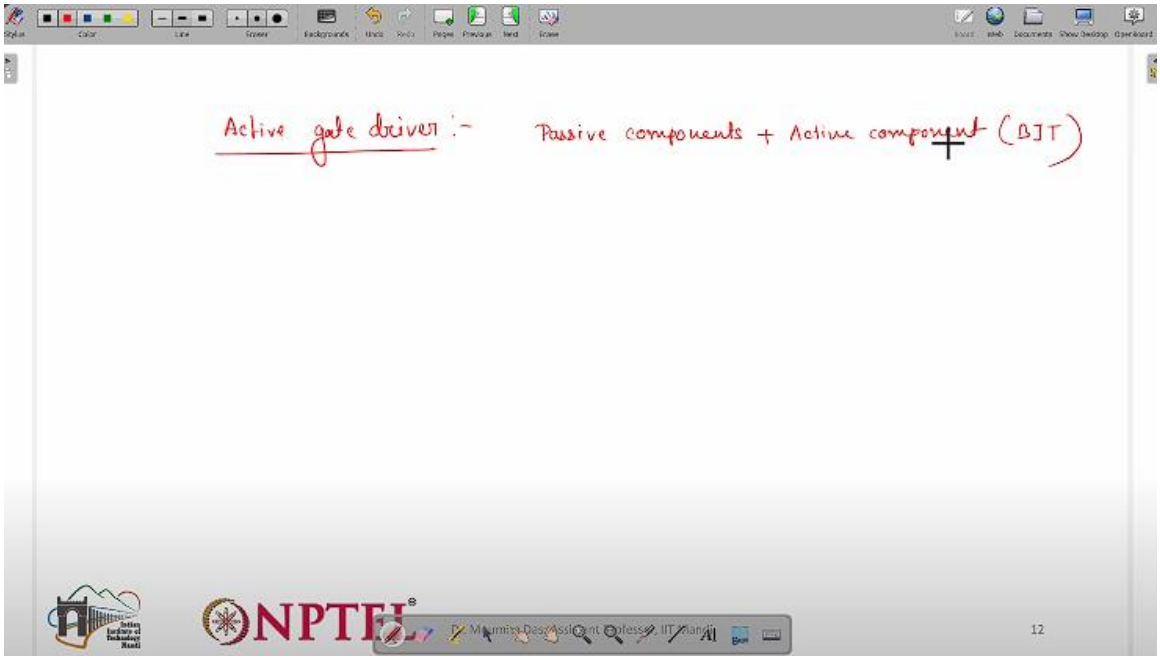
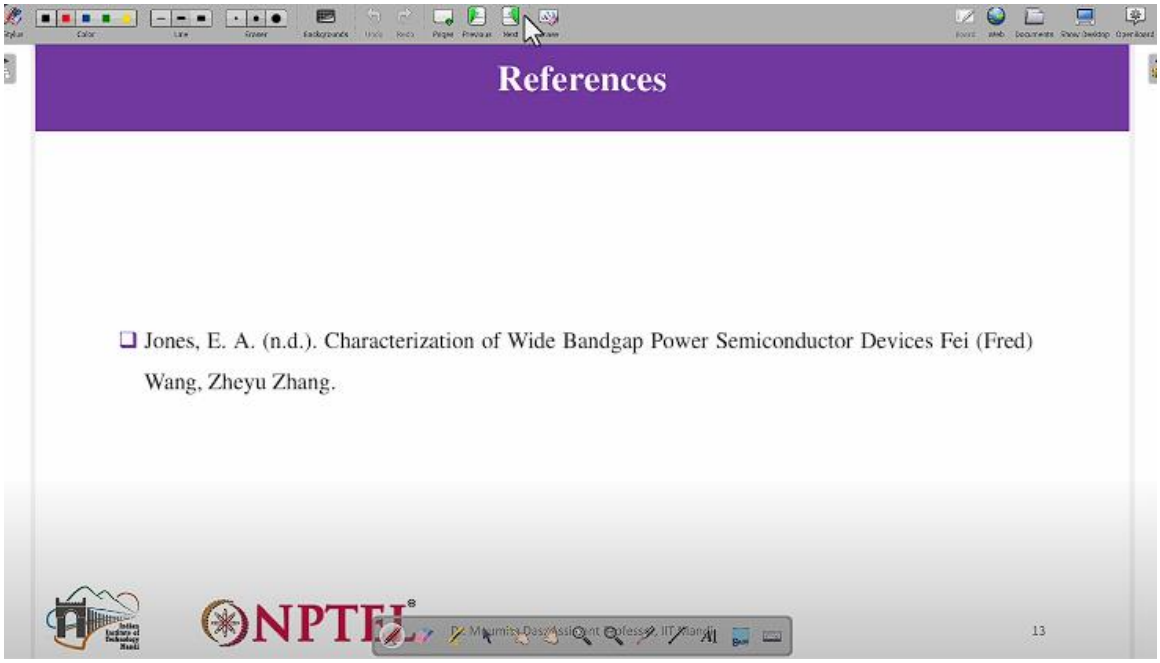


So active kind of gate driver, so whatever problem is coming during the crosstalk and whatever solutions we have provided the optimization we can do using active type of gate driver. So what will be there in active gate driver along with the passive components will be connected in series with some active component. So active component means it can be BJT. So let's say there is this capacitive type of solution is provided. In series of capacitance there can be one BJT connected. And BJT control will come from the feedback path. Now depending upon the operating condition, We can either change the value of the capacitance connected in that particular path or completely bypass that particular capacitance. So that will be up to us depending upon the operating condition that we can actually always monitor. So that is why this is known as active gate driver. So more about this active gate driver I will be discussing in the next class.



So you can refer this particular discussion in the same book which I have already told you. So, I will be discussing about active gate driver in the next lecture. Thank you.