

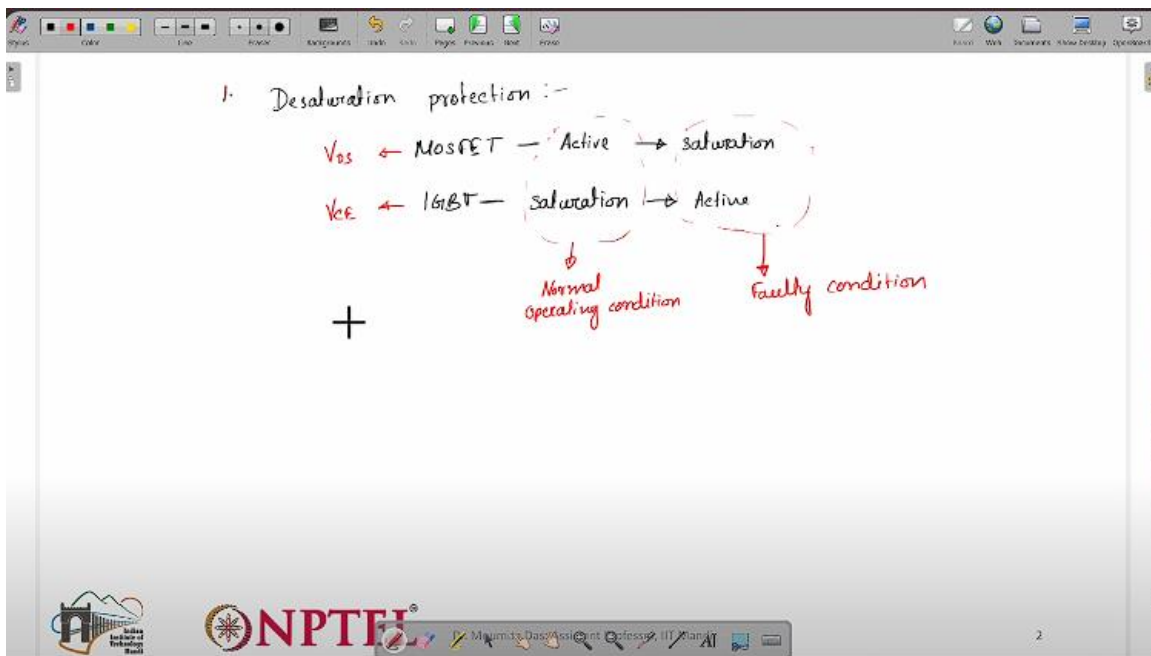
Power Electronics with Wide Bandgap Devices
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Lecture-11
DPT-PROTECTION

DPT-PROTECTION

Welcome back to the course on power electronics with wide band gap devices. Today I will be discussing about protection of DPTs. In the last lecture I have discussed about protection needed for the device under test. Today we will see what are the protection required for DPT circuit.

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So in the last lecture I have already told you so like different types of protection generally we use for DPTs are first is the desaturation protection. So now when I say desaturation protection then the things which is coming to our mind that is with respect to the device should not reach into the saturation or it should not leave the normal working region. So for that what is the important parameter? So we have to see what is the voltage drop in the device. For MOSFET it is V_{ds} and for IGBT it is V_{ce} . So, if we can sense this V_{ds} and V_{ce} , then we will have the information about this voltage whether the device is operating in normal condition. Normal condition is also different for MOSFET and

sensed and then what will happen, it will be compared in the comparator with respect to the desaturation voltage level and check whether the device is in normal condition or in the faulty condition. If the device is in faulty condition this comparator output will be given to the gate driver and then it will provide the required signal to the device so the device will turn off. So, now you can see here there are different components which are present in this desaturation protection. So, you can see here there are like two resistances R_{sat1} , R_{sat2} and then capacitor C , diode D and then this voltage here is the V_{desat} and then here the resistance and the MOSFET it is along with the comparator it is present here. So, in this case what is happening all the information we need to like provide if we know what is the device characteristics. So, that is one of the main disadvantages of this kind of protection, means we need to have prior information of the device until and unless, we know where the device is operating either it is in saturation or the active region, we cannot provide this kind of protection, so that is why for wide band gap kind of devices, where we probably don't have all the information, there this kind of protection implementation will become difficult because we need to have information of the devices. Okay? and also you can see here, so there are like different component involved, in this case so let me just write down.

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Disadvantages :-

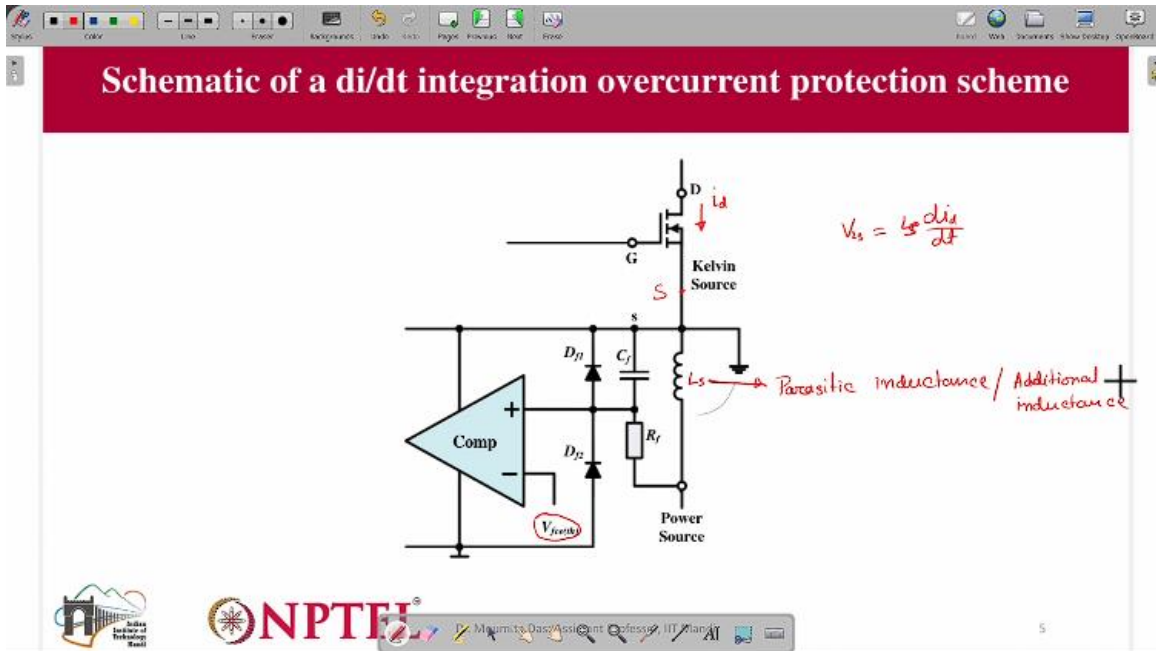
- ① Prior information of the device is required
- ① Diode must be used to protect sensing circuit
- ③ Over-current threshold is set by saturation current level
- ④ Saturation current is a function of junction temperature of the device

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So what are the disadvantages of this kind of protection? First is the prior information of the device is required. okay okay, now with respect, this is with respect to the device part and with respect to the implementation part, what are the other disadvantages? so this diode, so diode i will just show you this previous scale so diode you can see here D_{ss} which is represented here in this diode so this diode must be used to protect sensing

circuit. Okay? So that is why this diode is very important if there is any condition where it may happen that over current or anything which may destroy the sensing circuit, so that can be protected by using this diode. So that is why this diode connection is very important. Third is that over current threshold is set by saturation current level. Now, we need to have this information of saturation current level and this will vary case to case means device to device. So for some device, so let's say this desaturation block if we are implementing, so we cannot use the same block for all the devices, means depending upon the device type the current level will change and also the saturation level will also change and also you know that this saturation level depends upon the v_{gs} which we will be applying or the gate to source voltage, so control signal which we will be applying depending upon the voltage level the saturation current level will also change. So that is also something which we need to consider while implementing this desaturation block. So, whatever condition we will be using that will be device specific. If we are changing the condition or the device this saturation current level will change and based on that this implementation of the desaturation block should also change. The fourth one is the this saturation current, is a function of temperature, basically junction temperature of the device. Now if in any case due to some reason, let's say ambient temperature is changing or maybe during the operation the device junction temperature is changing, then what will happen? This saturation current will also change. Right? This if the saturation current is also change, so based on this current level the threshold whatever is set for the control block, so that will that should also change and if we are not changing that threshold then again there will be problem protection. Because you know with respect to temperature you have already seen in the datasheet current level of the device generally decreases. So if it is decreasing and how much it is decreasing that information, we need to have so that with respect to temperature this threshold value, we can change. If not then there again there will be problem in the protection so these are the disadvantages. which are involved with respect to this kind of protection.

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Then the next protection which I have already told you in the previous lecture that is di/dt integration over current protection scheme. So, di/dt integration protection where we need to have device and the protection is generally implemented between the Kelvin source and the power source ground. So you can see here so device ground it is shown here in Kelvin source right. So here DGS, so what you know as the source that point it is here. So, basically ground point of the device. So, that is represented in Kelvin source. And there is one inductance, let's say this inductance I am representing in terms of L_s . So, this inductance is in between this power source and the Kelvin source. So, source means the ground pin which we generally represent as source. So, Kelvin source is the ground pin of the device and power source ground means if it is connected to DC source this is like negative point of the DC source. So, basically power source ground, power ground basically that is what it is representing. So now there generally what happens in any device, so this kind of parasitic inductance will be present. So if we are considering silicon device, generally silicon device the connection it is such that there will be some parasitic inductance will be present between the device ground, device source and the power ground or the power source. Okay? Now this inductance, due to the presence of this inductance and as you know, there is a current which flows through drain to source that is generally we represent in terms of i_d or the drain current, that current will also be flowing through L_s and due to that, what will happen, so due to this presence of this L_s , if the current let's say I am representing this in terms of i_d So, due to this, the voltage across L_s will be di/dt . So, now if we have this voltage across L_s equals to $L_s di/dt$. So, then this we can actually sense and then we can actually compare this with respect to the voltage threshold voltage whatever is specified. Then we can see whether there is over current or not. If the current level is very high, this i_d due to some fault or any reason or

or inductance of the DPT circuit, it is getting saturated or load is sorted, so then what will happen this current will be tremendously high. So if this current is high then the voltage drop across L_s will also be very high? Then whenever we will see this voltage with respect to this threshold voltage, then we can understand that whether there is a fault or not. If there is a fault again, this block will send signal to the gate driver, as you know like the previous case the comparator after comparator block it is going to the logic control and it is going to the gate driver. So, similar after comparator so whatever you can see here before comparator, so this before comparator part here it is mainly sensing the voltage across the device, so basically this voltage right in case of desaturation and in the di/dt protection it is sensing basically the like current through the inductance so that is why you can see here this sensing block it is connected like this. Now it provides signal to the comparator and after comparator it goes to the gate drive and gate drive sends signal to the gate of the device and then if there is a faulty condition then the device will turn off. So that is how this device will be protected by this protection method. Now this method is also having some disadvantages.

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Disadvantages of di/dt protection :

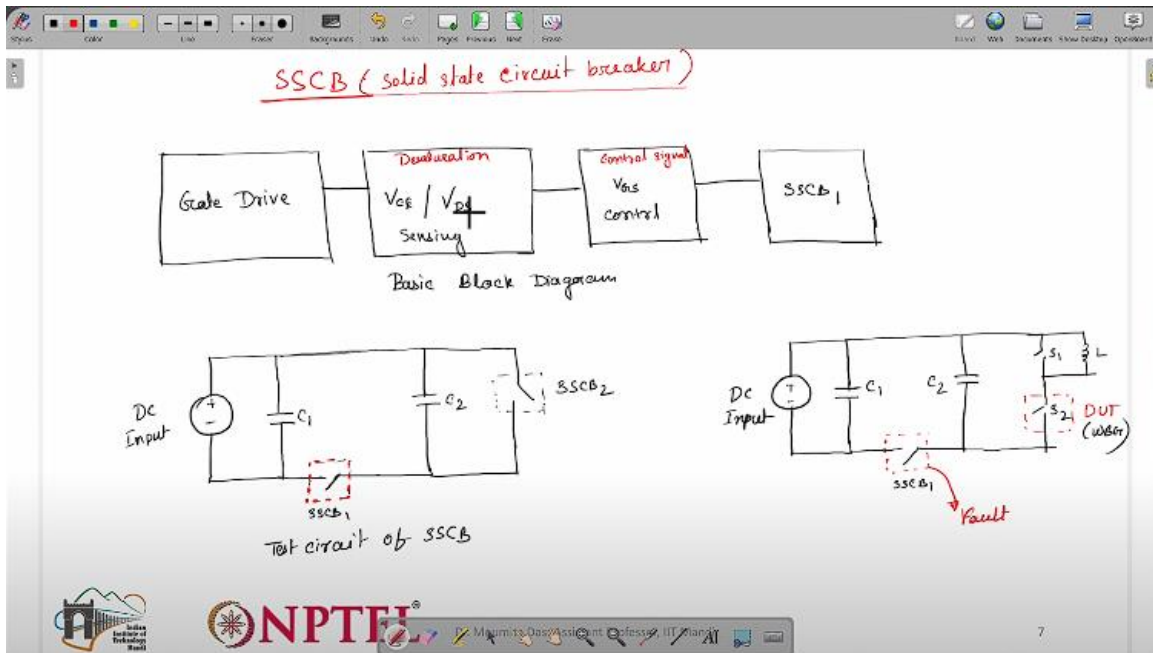
- ① WBG $\rightarrow$ less value L_s causes implementation of this protection difficult
- ② External inductance $\rightarrow$ Variable

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So what are the disadvantages of this particular method? So, the main disadvantage is this, so let me write down, disadvantages of di/dt protection. So first point I will just tell with respect to wide bandgap device. So wide bandgap device you have already seen the device size as compared to silicon device. So it is very small. so chip scale level, so basically where all the different points are connected drain shows gate, so there what

happens the chip size is very small with respect to silicon, so then what happens the L_s what I have represented here, generally, it is much higher in case of silicon device and also layout which we generally consider for silicon based converters so they are from the layout also this parasitic inductor so this is basically parasitic inductance either it can come from the chip or the device or it can come from the pcb layout so in both cases, so what will happen silicon has like much higher value of L_s due to this higher size of the device and also the pcb layout, the way we implement so that this gives sufficient amount of L_s and that is why implementation of this kind of protection for silicon device is much easier but in case of wide band gap devices what happened? so this parasitic inductance we try to minimize in both like device level and also in the pcb level. So this WBG devices that is why it is having less value of L_s , if it is having less value of L_s so then implementation of this kind of protection will be difficult. So then what we have to do? In any case if we want to implement this kind of protection, so then what so the less value of L_s causes implementation of difficult. Because you know like we need to have sufficient amount of voltage. So that comes from the inductance. If inductance is very less then L_s multiplied by di/dt will also be very less. So then the voltage which we will be getting that will be very less. So in any case, if you want to implement so then we need to connect one coil at the like between this device between, sorry between the device and the power source. So, here it is assumed that this will be parasitic inductance. But if this is not sufficient, we can also have additional inductance. added separately for this kind of protection. So, this can be added for WBG device. But again like there will be other kind of problem, if we are adding additional inductance that can cause problem in the operation of the converter. So that is why for wide band gap devices this kind of protection is not kind of advisable protection to be implemented. Now other associated problems are, so, the external coil or external inductance in case if we are adding this will be variable means with respect to different device what kind of inductance is required so that is not constant so it is device specific. So if we have let's say any protection circuit we cannot use it for any device we have to optimize the value based on the device rating. So that is another important point okay so these are the disadvantages of this di/dt protection. Now the third one you know this like current limiting in the dc source or any other source whatever you will be using. But again like that is not quite practical practical kind of solution, so if we have if we don't have any like source like in lab generally we have this dc source we can just provide current limit in that and then we can actually test the device in the control environment.

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So, this is for the testing purpose that is fine. But like otherwise it is not that much practical solution. Okay. Now, the fourth one which I have already told you in the last lecture that is S, SSCB or solid state circuit breaker. Now I told you this solid state circuit breaker is kind of universal solution, where we don't need device information in advance. So that is why this kind of protection is kind of protection which can be applied for any application for any devices, we don't need any like additional information about the devices or the circuit or device type it should not it will not change with respect to device type so like previous cases you have seen depending upon device type either like L_s will change or V_c V_{ds} all this will change and depending upon the device type also like MOSFET IGBT, so there we need to have the information of the characteristics so that is why this protection is like kind of more practical or or more useful protection for wide band devices. So how we can use this kind of protection? So first i'll just tell you what are the basic blocks involved in this protection. So the basic blocks are, first is the gate drive so that is there for all the protection, right? And then there is a block of V_{ce} or V_{ds} sensing or monitoring. So this is for desaturation implementation. I'll tell you like, if we don't have information about this then how to use this method. Then the third one is the providing V_{GS} control. And then this is what we provide to the device under test. Or it goes to the SSCB. So why I am saying it is device under test? So generally what this SSCB is nothing but a device. So solid state circuit breaker, so it is we can consider as device under test, so in place of wide band gap device we can like in order to implement this solid state circuit breaker what we need to do? We so this is the basic block diagram. Now test setup how it looks like. So it looks same as the DPT test setup. So only thing is that here we need to replace the device under test or DUT by using SSCB. So how that looks like. So the circuit diagram test circuit diagram it looks like. So same DC voltage

what we use for DPT test, we can use that. Then there are like two different capacitors generally we use for this kind of test. So then there will be one SSCB. So, SSCB is similar to like any kind of switch. And this we can represent as SSCB. Right. Now there is another capacitor. This is energy. First capacitor is the energy storage capacitor. And then second capacitor it is basically decoupling capacitor. Right? So these two capacitors already I have discussed what are their function and all. and now there will be another solid state circuit breaker, the same switch same what we are using in place of SSCB. Here so they we are using in place in this place as well. This second this is primary and this is the secondary one. So this the first one this is the one which we are testing means, the SSCB if we want to test this is the one which we are basically testing the SSCB, how it is operating and how to set different parameter this SSCB and now as you can see here so, this looks like switch and this actually this is the one SSCB 1 Okay, so here the control signal is coming from all this basic block diagram whatever I have shown. So I'll show you little diagram later. Like what are the different parameters are present in this VCE, VDS sensing and then VGS control block and gate drive block. So but at least you can understand. So basically this is providing the desaturation. So desaturation is provided by this one. This is the control signal and the drives, gate drives. Now whenever we are providing these two SSCB1, then we can test different parameters of SSCB1. But SSCB2 if there is any fault that cannot be handled by SSCB1 then this will provide the additional protection. So before use it in any device. So this is basically the test circuit. I will tell you about the test method also. Circuit of SSCB or here I can just write down the full form which is Solid state circuit breaker. So now this is the test circuit, once you have we have because initially we don't have information about about this SSCB. We are assuming that we are testing a new device and for that we have to use this SSCB. Then we can use this SSCB in place of DPT switches. Now what we need to do, we need to use this same SSCB, which i have shown in the dotted block, so that will be used in the DPT circuit to provide the protection of the device, which will be used in DPT so the test setup of DPT will look like It is having similar kind of capacitances which I have shown in this left diagram. So energy storage capacitor is C1 and this SSCB1 which we have tested now, so this will be placed here only. So this you can see here. So just let me use the red color. Then it will be highlighted. So this SSCB1 it will be placed here only. And then there will be decoupling capacitor. Right. C2. Then this is what is connected to the DPT. So how this DPT looks like? So DPT depending upon like what kind of switch you want to perform. So, let's say the device which you are testing, that is the lower device so S1 then L then S2. So, let's say this device which you are testing, so this is the device under test. Right? So now whenever there will be a fault, if any situation is happening there is a faulty condition, so then what will happen in that condition this SSCB1 will disconnect this input power source, so this is the input DC input. DC input. This input power source to be disconnected from the device which is under test. Let's say this is the WBG device. Then this device will be protected if there is a fault condition. And before this fault

condition, we have to actually before implement using this, we have to set the SSCB control and this control will come from the basic block diagram.

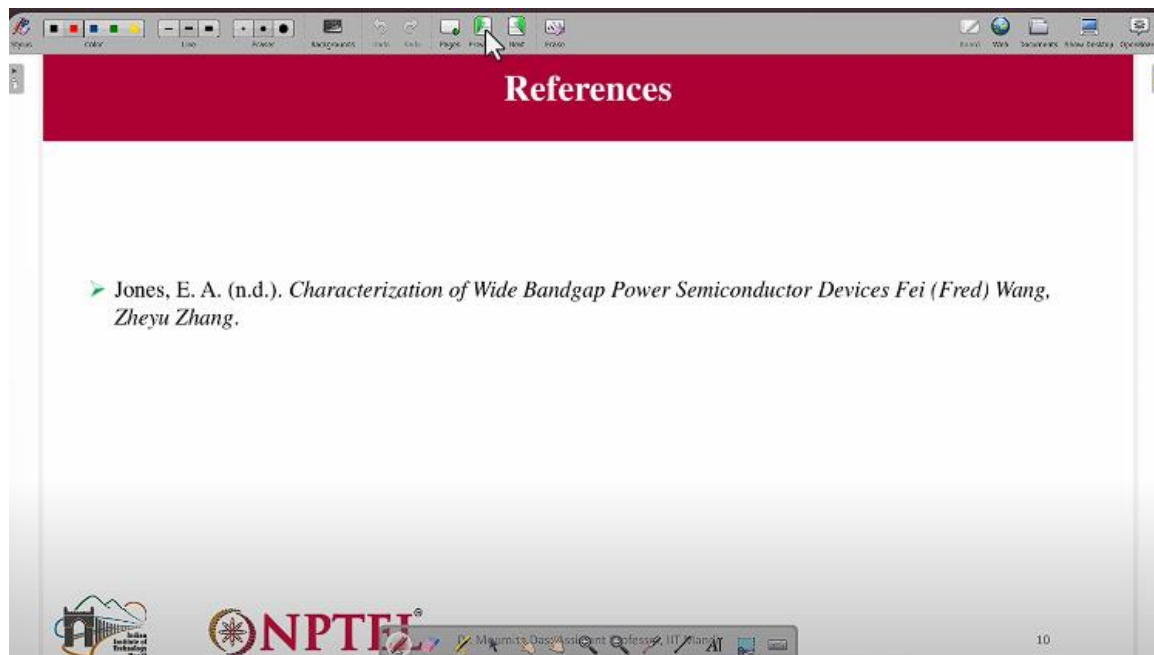
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The image shows a digital whiteboard with handwritten notes. At the top, 'Important parameters' are listed: 'Short circuit protection time ($< 500\text{ns}$)' and 'Overvoltage across the IGBT/MOSFET ($< 60\text{V}$)'. Below this, 'SSCB Test setup implementation steps:-' are listed in three steps: 'Step 1:- one short pulse is provided to SSCB₁ ($< 10\mu\text{s}$)', 'Step 2:- Desaturation block is disabled.', and 'Step 3:- V_{as} control unit $\rightarrow$ turn off signal during fault send to SSCB₁'. Under 'Disadvantage', there is a circuit diagram of a capacitor C₂ in series with a diode D_{UT} (labeled 'protected'). The whiteboard interface includes a toolbar at the top and logos for 'ONPTI' and 'Mamta Das' at the bottom.

So we can set the value the time basically two parameters we need to set for SSCB, so basically the important parameters important parameters for SSCB, Important parameters are, so it has to provide the information of the time. So basically short circuit protection time. So, now you know for silicon it can be 10 microsecond, but I told you in the last class for wide band gap devices it will be 200 to 400 nanosecond. So, that is why the protection should be implemented, this protection time should be implemented such that it should provide the protection less than 500 nanosecond, right? So, that we have to implement initially in the test circuit of the solid state circuit breaker. The second thing is the over voltage across the IGBT or MOSFET. So this like wide band gap devices can be there. If there is a over voltage condition is happening then immediately the device solid state circuit breaker will turn OFF and then it will disconnect the input from the output. Okay. So this is how this system is operating. So the step for the test is so basically SSCB test test setup implementation steps are so step 1 so basically one short pulse is provided from the so this is this is the DPT we are using right so DPT we provide two pulses but here only one short pulse is provided to the solid state circuit breaker under test to let's say SSCB₁ from this gate drive. Now this short circuit short pulse length should be slightly higher than the required short circuit protection time, so it should not be 10 microsecond it should be less than that but it should be slightly higher than that of like let's say if it is 200 nanosecond we can provide it for 500 nanosecond. Okay? then we can check check whether the device is responding or not. Obviously this should be much

much less than 10 microsecond which is given for silicon device. Okay? Now step two, so now this components related to desaturation block need to be selected. Now if we don't have information of the desaturation block or this VCE, VDS block, this desaturation block will be disabled initially. Right. Now step 3. It is with respect to the control unit VGS control unit. So this VGS control unit. Okay, so now if there is any over voltage, then what will happen? This will turn off, this will provide the turn off signal to to the SSCB if there is any faulty condition. Okay then the device is protected. These are the implementation step that you understand. Now device is also protected. Then everything is fine. You don't need to initial information or the pre-required information and your device is also protected. But there is a disadvantage in this method also. So what is the disadvantage of this method? you can see the diagram so you can see here if in case of fault what will happen this will be disconnected. So then the circuit will look like this is the energy storage capacitor, which will be disconnected from the decoupling capacitor which is connected to the devices which are under test Right? So this is how it looks like. So now this part is protected. This is protected. Now whenever we disconnect, so then this decoupling capacitor charge remains there. Device is protected but this decoupling capacitor it is disconnected from the input, So then it needs to discharge somewhere because you know capacitor charge it anyway like it has to discharge through some medium, eventually then it provide it it gets the discharging path through the devices which are connected here, so, basically it discharges through device under test. So through inductor and the device under test. So then what will happen again like obviously this discharging is not kind of thing which is desirable. So this is the disadvantage of this particular method.

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Okay, so you can actually look into the reference, this reference for this particular discussion. So, this is under DPT protection chapter. So, I will be discussing more in details about this different component in the next class and how to select the this component parameters with respect to the desaturation block and then VGS control block. So, how it looks like. So, that I will be discussing in the next class. Thank you.