

Analog Electronic Circuits
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Lecture - 84
Basic Analysis of the 741

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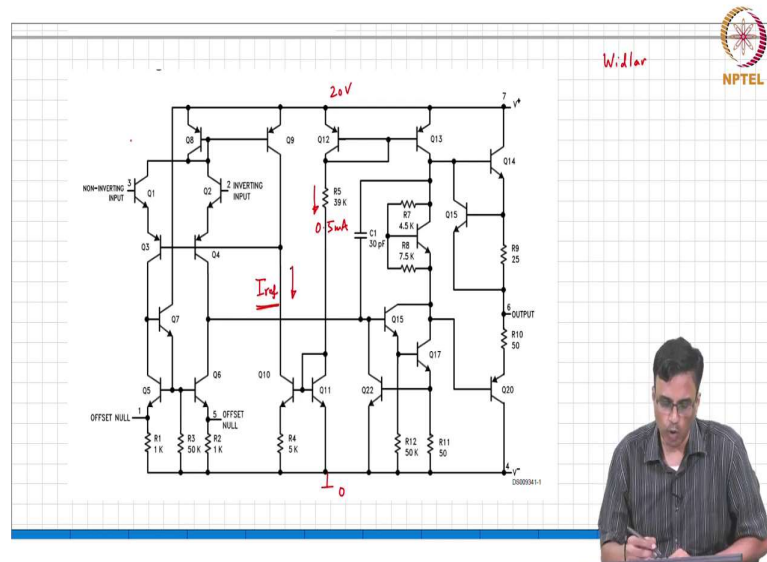
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And, so, now let us pull up the so, this is the beautiful 741, right. So, I believe you understood, what Q1, Q2, Q3, Q4, Q8, Q9 and this feedback loop, correct? Now, this is what I_{ref} we were talking about. Now, something clever, as with everyone of this, the designer of this circuit is a guy called Robert Widlar, right, and like you know, almost all of his circuits are incredibly clever, right? And, so, this is yet another example of a clever idea.

So, let us first assume that you know that these op-amps are all supposed to be intended for dual supply, right? I mean, people use plus or minus 15 volts and so on. So, but it does not matter; let us, just for our own simplicity, assume that this is 0 and this is, I do not know, some 20 volts, ok.

So, what comment can you make about the current situation through this R5? What is this voltage? 0.65. This voltage is going to be 19.35. So, basically, $20 - 1.3$ is the drop across the resistance. So, basically, I would say something like, "You know, 18 volts, 18 and a half volts across 39 K, and this basically causes roughly about 50 microamperes, is it?" Roughly, it is half a milliampere, ok.

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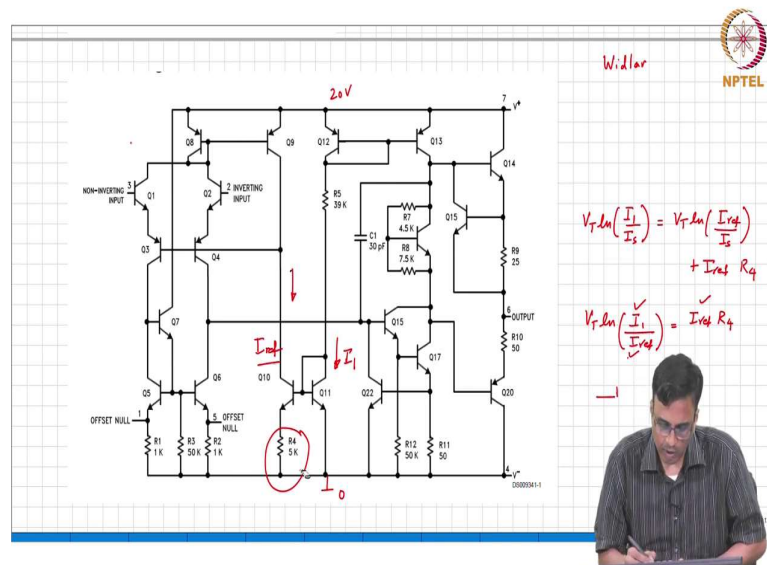


And, more importantly as you keep changing the supply voltage the current through this goes on changing because the current is simply $(V_{DD} - 1.3) / 39 K$, alright. So, and the design was such that, I mean, another thing that you have to be worried about is that you cannot have a current like this if you directly use a current like this to bias the input pair, right?

So, if this I_{ref} varies with V_{DD} a lot, correct? What problems do you foresee in the design? If I change the quiescent current changes what comment can we make about the current in the input pair? It will change. If g_{m1} if current changes, what comment can you make about g_{m1} ?

It changes. So, what happens to the dominant pole frequency, or what happens to the unity gain frequency? That also keeps changing, right? But what happens to the second pole? If the unity gain frequency keeps changing and the second pole does not move exactly the same way, what comment can you make about the phase margin? It will go on changing, right? So, you can potentially have a system that is nice and working for 10 volts, but the moment you move it to 12 volts, there is lots of ringing and all that stuff.

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So, you want this current to be, you know, largely independent of the supply voltage, ok. So, basically the idea is that if this current is let us call this I_1 and you know how do we get I_{ref} here? What do I mean? How do we find out what I_{ref} is? Well $V_T \ln(I_1/I_S)$ must be equal to $V_T \ln(I_{ref}/I_S) + I_{ref} R_4$, correct. So, basically this means that this $V_T \ln(I_1/I_{ref})$ must be equal to $I_{ref} R_4$, ok.

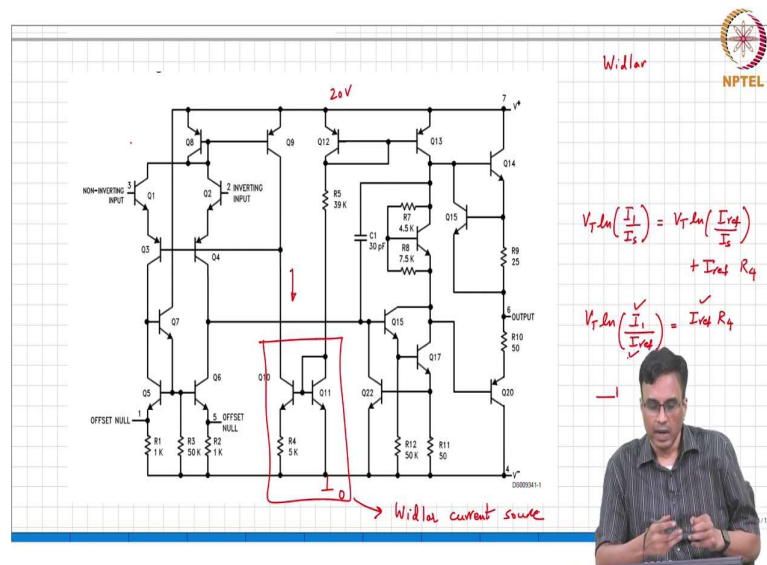
So, it is actually I mean to find I mean given I_1 and R_4 I mean and R_4 to find I_{ref} you would have to solve this equation numerically, correct. But, if you want I_{ref} to be something correct, then it is very straightforward to find if I_{ref} is known and I_1 is known approximately then it is very straightforward to figure out what R_4 is right.

So, in this case I mean you can more easily figure out R_4 . I think it will turn out to be a few micro amperes right, ok. And, the nice thing about this circuit is that you know what comment we can make about I_{ref} ? Is it going to be much smaller than I_1 or larger than I_1 ? It is going to be much smaller because there is going to be a drop e to the power of the drop across that resistor, right.

So, in other words the drop across this resistor has an exponential effect on reducing the current, correct. So, in other words you know for a small very small resistor R_4 you can get a very small current, right. So, nominally I mean normally if you have some voltage and want to generate a current you have to do V/R is the current.

So, if you want a very small current that resistance must be very large, it turns out that large resistors are difficult to make on an IC. So, basically you want to get a very small current, but with a small resistor.

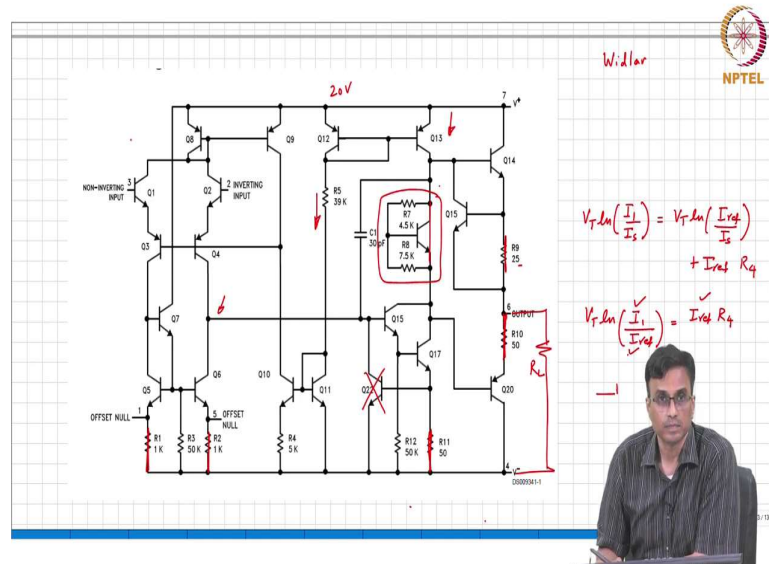
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So, this is one way, this is what this current source is called the Widlar current source ok. And, is a clever trick to get a small current while still using a small resistance ok. And, what comment can we make about the supply sensitivity of this current? This current is actually sensitive to supply, but the voltage across you know voltage across the base of between the base and emitter of Q11 is largely independent because it is logarithmically you know the base emitter voltage is $\ln(I)$.

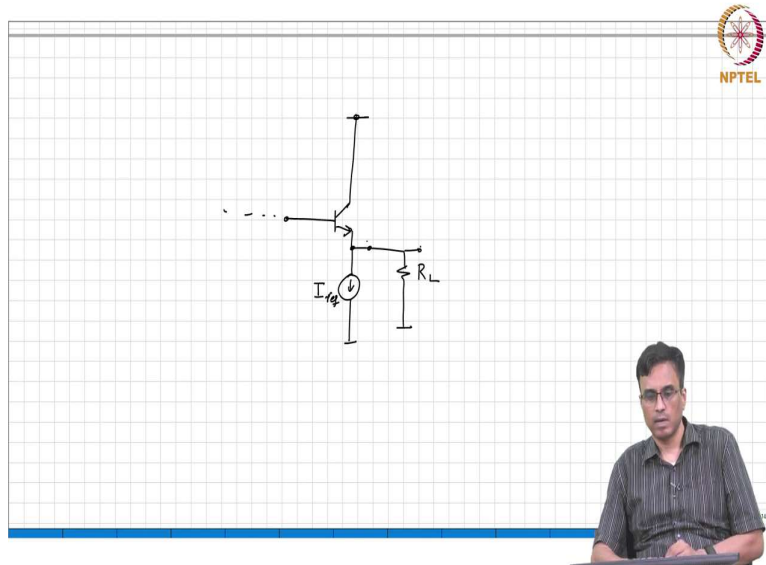
Now, see, there is the second stage you know goes into now, for the time being, let us assume that this is a short circuit, ok? What is Q13? It is simply a current; whatever current is flowing here is mirrored there. So, basically, that behaves like the current source load for the second stage.

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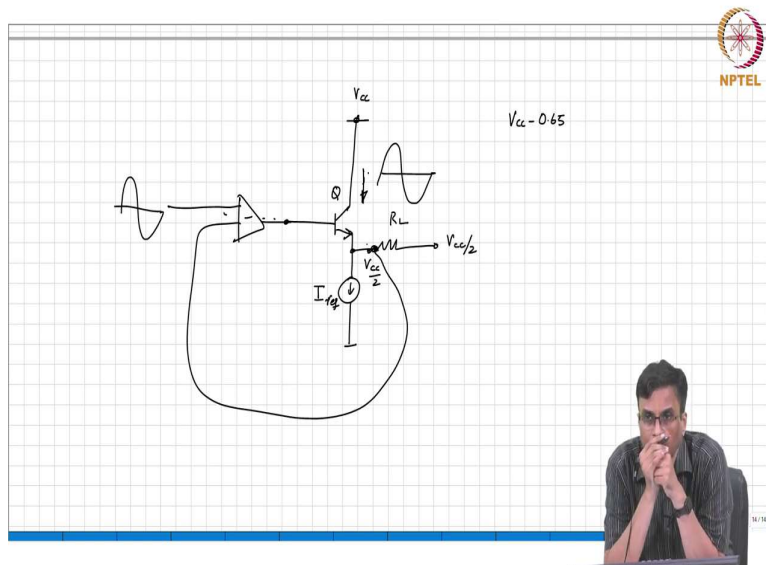
And, so, the output basically is you know through some load resistance is R_L which is outside the chip. So, you know again for the time being these resistors 25 ohms and all that you and 50 ohms lets neglect, ok. We will add we will figure out why they are needed, you know just a little bit. So, Q14 how does that behave? It is a common collector stage, right.

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So, the common collector stage, see normally as far as the output is concerned, I mean the output stage we so far have discovered we have discussed is basically a common collector stage, right. It could be an NPN common collector or a PNP. So, now let us see what the problem is with just having a common single common collector stage, ok. So, this is the internals of the op amp. So, what is the cut off limit for this transistor? Let us say some let us say this is the common collector. So, this is some I_{ref} . So, what is the; what is the voltage swing at the output which will cause the transistor to get cut off?

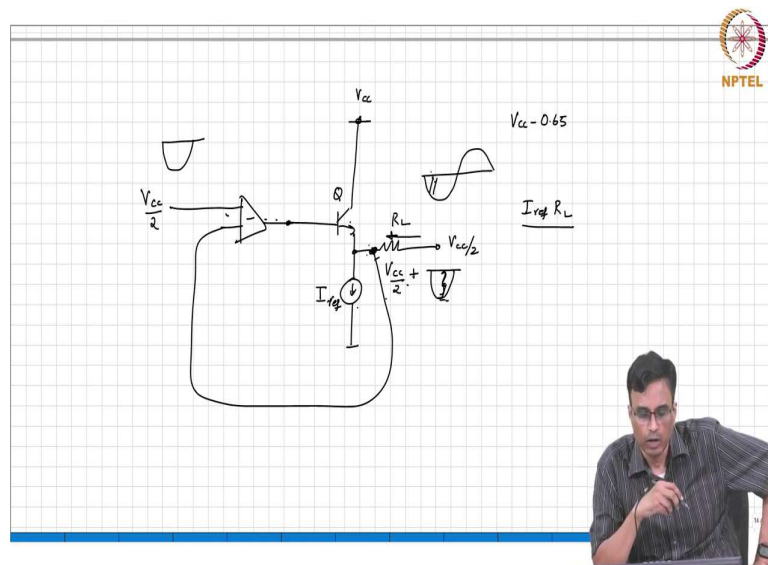
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Maybe ok let me remember the load is connected to analog ground which is $V_{CC}/2$ this is V_{CC} under quiescent circumstances this voltage is $V_{CC}/2$. This is R_L , correct? When you apply a signal, you know the output voltage is swinging like this. What is the maximum voltage that the output can go before something bad happens to the devices? If the output voltage keeps going high what happens eventually to the transistor?

So, V_{CE} no this is being driven by the feedback loop inside, correct? So, if this goes too high what happens to the transistor? It is moving towards the saturation region. So, what is the highest voltage the output can go before the transistor gets into the saturation region? $V_{CC} - 0.65$ is the upper limit. What about the lower limit? When the output is going low the transistor is going into the? I mean what comment can you make about the current in the transistor? So, under quiescent circumstances this is $V_{CC}/2$. So, this current is in the negative half of the input cycle where this output voltage is going below $V_{CC}/2$, right.

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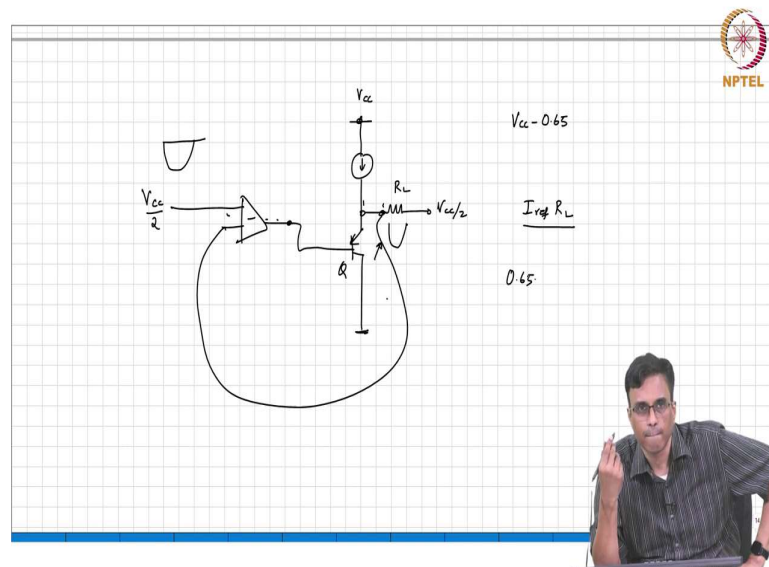
What comment can you make about the current in the load? Is it flowing in or flowing out? It is flowing like that. So, what comment can you make, but the sum of the load current plus the transistor current equals I_{ref} . So, what do you do; what do you think the transistor is going towards? So, what is the maximum output swing that is possible before the transistor goes into cut off? Yeah. So, basically the swing here around the quiescent operating point of $V_{CC}/2$ will be $I_{ref} R_L$, ok. So, let me repeat it again. So, this op amp is part of a negative feedback

loop. Under quiescent circumstances this is $V_{CC}/2$ which is analog ground. So, this voltage is going to be $V_{CC}/2$, correct.

Now, when the input is in the negative half of the input cycle, when in the negative half the input cycle what is happening? This is going to be also $V_{CC}/2$ plus some negative things there. We are trying to figure out what the maximum amplitude is before the transistor goes out or goes into the cut off free. So, the transistor is just cut off, the current flowing through the transistor is 0.

So, therefore, all this I_{ref} must be flowing through R_L . So, therefore, the voltage across R_L is going to be I_{ref} times R_L , ok. So, you can see that the positive half peak swing is independent of R_L whereas, the negative limit is dependent on R_L , alright. So, this is if you used an NPN common source common collector amplifier at the output. Now, if you use a PNP common collector what will happen? This is $V_{CC}/2$, this is R_L , ok.

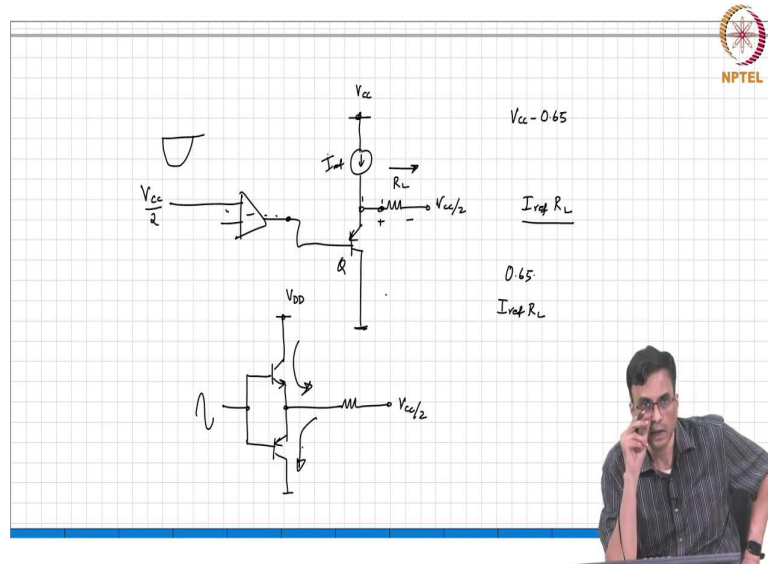
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So, if the input goes in the positive half of the in the negative half of the input cycle what happens to the transistor? When this voltage goes low, what is happening to the transistor? When the output voltage goes low, the collector is constant at ground, the emitter is going lower and lower is moving towards the saturation region, correct? So, what is the highest, what is the lowest voltage, what is the lowest you know potential there before the transistor goes into the is plus 0.65, right. Whereas on the high side now, what happens? High side what

happens? When in the positive half of the input cycle current is going that way. So, the transistor is in danger of going into the cut off region.

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So, what is the maximum swing? So, the voltage across the maximum positive voltage across the R_L is basically $I_{ref} R_L$, ok. So, what do we see? What is the model of the story? So, in the NPN case the upper limit is $V_{CC} - 0.65$ which is independent of R_L , the lower limit is dependent on R_L . In the PNP case, the lower limit is independent of R_L the upper limit is dependent on R_L , right. What do we want?

We want both to be independent of R_L . So, what should we do? You connect you connect both like this. So, this is $V_{CC}/2$, ok. So, when the input goes positive, this transistor will push current. When the input goes negative, this transistor will pull current ok.

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The diagram shows a differential pair of transistors. The top transistor's base is connected to an input terminal labeled $V_{cc}/2$. Its emitter is connected to a current source I_{ref} and a resistor R_L . The current source is connected to V_{cc} and the resistor is connected to ground. The output of the top transistor is labeled $V_{cc}/2$. The bottom transistor's base is connected to a diode-connected transistor circuit. This circuit consists of a diode-connected transistor with its base connected to $V_{cc}/2$ and its emitter connected to ground. The collector of this diode-connected transistor is connected to the base of the bottom transistor. The emitter of the bottom transistor is connected to a resistor R_L and ground. The output of the bottom transistor is labeled $V_{cc}/2$. Handwritten notes on the right side of the diagram include $V_{cc} - 0.65$, $I_{ref} R_L$, 0.65 , and $I_{ref} R_L$. The NPTEL logo is in the top right corner.

But, when the input is 0, what happens? I mean in other words when the input is $V_{CC}/2$ what happens? No current flows because basically the you know if this is $V_{CC}/2$ and this is $V_{CC}/2$, both the transistors are off because the V_{BE} is 0, correct?

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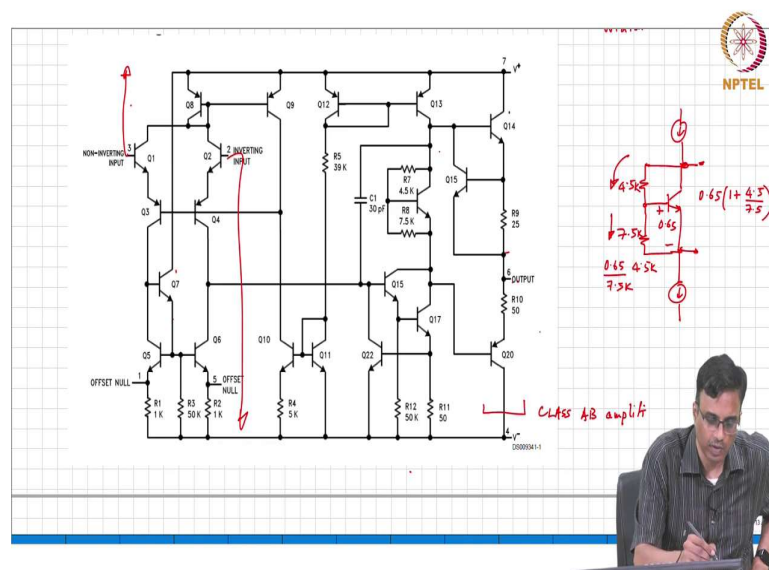
The diagram is similar to the previous one, but the diode-connected transistor's base is connected to a bias voltage V_{bc} instead of $V_{cc}/2$. The bias voltage V_{bc} is labeled as 1.3V. The rest of the circuit, including the differential pair, current source, and resistors, remains the same. Handwritten notes on the right side of the diagram include $V_{cc} - 0.65$, $I_{ref} R_L$, 0.65 , and $I_{ref} R_L$. The NPTEL logo is in the top right corner.

So, what do you know? What should be done is you have you know there are many ways of doing this you know one way is to put a battery off exactly 1.3 volts, ok. So, and you know perhaps put you know V in here. So, both the transistors are at the verge of conducting if the input goes slightly positive, then the NPN transistor will conduct immediately when the input

goes slightly negative the PNP transistor will conduct immediately and now because on the high side the your the NPN transistor goes into saturation and on the low side the PNP goes into saturation.

In either case, the swing is independent of the R. So, now with this background let us take a look at this. So, basically this is this is there is the NPN source followed that is the PNP you know emitter follower or common collector amplifier, right. Now, this is the battery, right and that is called the V_{BE} multiplier for a good reason I will tell you why.

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This is 7.5 K, this is 4 and a half K. So, what is this voltage? Some current is flowing. So, what is the voltage here base emitter voltage? 0.65. So, what is the current flowing here? $0.65/7.5\text{ K}$ what is the voltage across the 4.5 K? So, what is the voltage drop you see there? $0.65(1 + 4.5/7.5)$, right.

So, this is. So, as you can see this battery is not 1.3 volts which will cause both to conduct simultaneously, right. It is slightly smaller so that only one of them conducts at any one time. So, the input goes positive, the NMOS transistor is pushing current if the input goes low, the PMOS transistor is pulling current, ok. So, this is the equivalent of that battery, ok and what do you call the CC is what? Is that 30 pF is the Miller compensating capacity, ok. So, now the question is why do you need all you know what are these guys doing there? So, of course, I mean you know it is one thing to do a toy problem in a textbook and the other one is to have parts which basically go into you know go into reality.

They will short, they will short, they can potentially short the output correctly to ground, and then they will blow the I_C , and then they will come back and tell you that, hey, you gave me a bad I_C , right, ok. Or you know your part is that you know something is wrong with your design, right? I did a great job, okay?

So, you have to. So, basically, there has to be protection for short circuits, right? So, how do you protect against a short circuit when you short this to the negative rail? For instance, the current flowing here will be very large. You did detect when a large current is flowing. I mean, when you short the output to ground, what is happening?

A large current is trying to flow, and that is going to simply burn up the transistor, because most of the current and power are dissipated in the collector-base junction, which has a large voltage across it. So, it will simply burn up this transistor.

So, what they do is put a small resistor there. If a large current flows here, what will happen? The voltage across R_9 will keep increasing. Once it becomes very large, Q_{15} will conduct and then simply pull out all the base current that is necessary for Q_{14} to operate. So, this is short-circuit protection.

Likewise in this case also if I mean for the PMOS transistor you know first of all there is a resistance in series to prevent somebody from going and connecting this directly to V_{DD} I mean that would simply you know blow the device. So, there is some resistance to prevent the current to some degree and you know if the PMOS transistor I mean if this voltage. So, you can as well sense if there is a lot of current going to flow through the PMOS transistor that basically means that there will be a lot of current flowing here.

So, again, Q_{22} is going to sense that it is going to turn on the moment this voltage drop becomes very large and go and pull all that current down. So, basically, pretty much for all practical purposes, try stating this whole thing, right? So, making it high impedance means that, of course, your op-amp would not work right, but the moment you remove the shot, you will find that, well, you know nothing; no harm has been done, right?

So, now that we have seen all this, let me come to Q_7 and why it is there. So, under normal operation, Q_{22} will be off, and Q_{15} will be off, too. So, they do not have any role to play if everything is working fine; they are just like insurance, right? So, they do not; they do not

mess anything up. Now, the current is ideal in an op amp if you put the same input to both terminals. What must be the current flowing out here?

If the two inputs are exactly the same, if you shoot these two terminals, ideally this current is supposed to be exactly the same as that current. So, this current is supposed to be exactly the same as this current. So, no current must flow out, right? In reality, I mean, you know so, but on the other hand, if you let us say you did not have Q 7 and you just shot this transistor here, you can see that the current being drawn by Q 15 is not the same as the base current being drawn by, you know, Q 5. So, here, what will happen if you just simply short these two without Q 7 being there? Right, then what happens is that the current flowing here is going to be, as we discussed yesterday, going into Q 5 and Q 6.

So, this current will be smaller, and this current will be larger. So, net current will flow out even when there is zero input. So, that is basically like adding an offset to the op amp. So, what is done is, you know, basically, the bottom line is that you draw exactly the same current, whatever current you are drawing here in DC current, the same current has to be drawn here.

So, that is why if you notice Q 15 has 50 K in the emitter and likewise Q 7 has 50 K in the emitter, ok, and so on, this basically makes sure that the current is the same coming mean. So, at least nominally, the offset is 0.

and these two terminals. So, of course, in spite of all this, because of manufacturing variations, there will be mismatches between Q transistors, which will cause some offset, and you know, users might want to null that offset. So, you know you have these two terminals coming out, ok, and you know you can actually add a resistor, you know, a resistor to ground there or on this side to be able to, you know, turn a knob and nullify that offset, ok.

So, that is a quick overview of the 741, right? You know, as you can see, it incorporates a whole bunch of things that you have not learned, right? But, so, this is what is called a class AB stage, right? But otherwise, a lot of these things are, you know, even if you have not seen them, hopefully you can understand them.

The input stage is actually perhaps one of the nicest features of the 741, and you know it is done this way for a reason. It is not some awesome random thing that you know somebody

woke up and said, "You know, let me wear my jeans pants inside out. You know, it will look cool, and like, you know, this is not like fashion."

So, everything is done for a reason; there is a reason why every component is there, and this was done in the days before computers, spices, and CAD tools existed. So, this is almost a work of art, right? I mean, it's incredibly clever, and you know, as proven for more than 50 years, it basically works nicely in the field, right?

And, of course, there are some more Belgian visuals. For example, another common thing people do is, by mistake, connect what you call the reverse supply and ground. So, there must be some protection for that, or people will try to connect by mistake, connecting 3 to the input, this to V_{DD} , and this to ground. Okay, and you know you do not want your IC to blow. So, there are some protection diodes to, you know, make sure that eventuality is taken care of and so on, you understood?

So, some Belgian visuals around this, but this is a good skeleton, which explains a lot of things that you know we have seen in various parts of this course. It kind of puts many of these things together, alright. So, with that, we are done with this class.