Analog Electronic Circuits
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Lecture - 83
Input Stage of the 741 Op Amp

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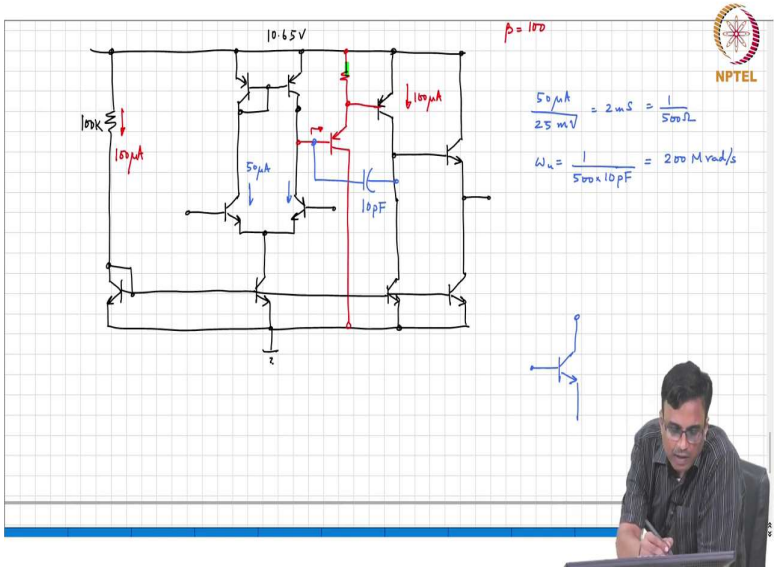

So, this is the basic idea, right? So, let us actually take a look at the very popular op-amp, which is perhaps the highest-selling chip in the history of electronics. It is the 741; let's see if I can download the picture rather than draw it. So, this seems like you know an op-amp, right? Early op-amps were indeed kind of designed based on this fundamental principle.

Unfortunately, it turned out that a lot of op-amps were people getting fed up with them in the field. So, they worked nicely in the lab, but once in a while, you knew the output of the op-amp would latch up, right? And, so, the problem was the following: The problem was that you all knew device physics. So, you will be able to understand this.

So, in a MOS transistor, let us say the transistor goes into the gate, which goes very high, and the drain goes low. Let us say we are building a common source amplifier. The gate goes very high, the drain goes low, and when the drain goes too low, the transistor goes into the linear region. In an NPN transistor, when the base goes very high and the collector goes low when the transistor goes into the saturation region, what actually happens inside the device?

So, in the active region, the base emitter junction must be forward biased and the collector base junction must be reverse biased. When the transistor is operating in saturation, the collector base junction is forward biased. So, basically, that means that whatever happens at the base will also reflect on the forward bias. What does that mean? That basically means that the collector-base junction is a short circuit.

So, if you yank the base up, if the transistor is in the active region, if you yank the base up, the collector is going down, whereas, you know, when the transistor is in saturation, if you yank the base up, the collector is also going up. This is a serious problem. Why do you think this could be a serious problem? Remember, when you put negative feedback around an op-amp, you are assuming that all the transistors are operating in the active regions.

So, now let's say by some mistake or by some transient. You know, many times what happens is that it takes time for the supply to come up right, but the input is already there. Under such circumstances, it is very easy to come up with scenarios where the common mode of the input or the common mode voltage of the op-amp inputs exceeds the supply.

Under such circumstances, the input pair transistors will only now be in the saturation region. See if the supply voltage is lower than you know the common mode voltage of the input. If the input common mode is greater than the supply, these transistors will become saturated.

So, basically, whatever happens here, you know the same thing will happen here. So, what is supposed to be negative feedback? You are going to arrange the signals of the op-amp so that there is overall negative feedback. Now, what happens is that the input transistors are saturated, the negative feedback has become positive feedback, and there is enough gain in these transistors to basically cause the loop gain to be greater than 1, but now with positive feedback.

So, what will happen? I mean, if you flip the signs of the op-amp in a negative feedback mode, look what will happen? The output will go to either plus VDD or ground; it will saturate, right? And, so, it will get stuck in that state and stay there, and the only way to fix the circuit would be to turn off the supply and turn it back on again.

And that, of course, is not a good thing because you have to. I mean, you know, I just imagine you are in a satellite on Mars and like to go into Mars, and suddenly, you know, something

like this happens. There is nobody to go and switch off the circuit in outer space and then switch it back on again.

So, imagine your phone, and you are talking in the middle of a very interesting conversation, and suddenly you know the whole thing just goes off. And, then, right at that time, you know, I am sure you are not thinking, "Well, you know, the guy should get marks for steps because, well, you know, it is almost working, you know, almost all the time."

Only once in a while does it do this weird thing, and I turn it off and turn it on, right? All of us know how annoying that is, right? right from a computer hanging in the middle of something to a phone, okay? So, you basically want this stuff to work right no matter what. So, this was clearly a big problem, right?

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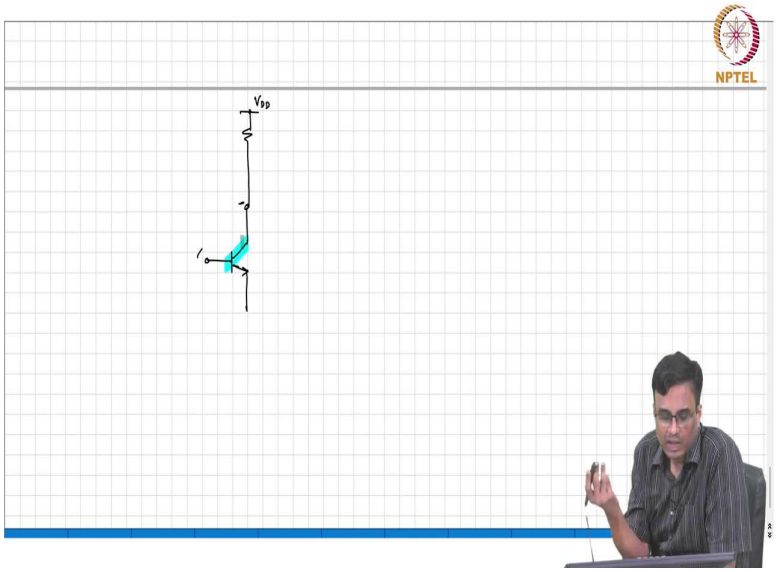

And, so, the root cause of the problem is that what is the root cause of the problem? The root cause of the problem is that you know in our common source amplifier whatever we build.

Let us assume that this is some resistive load, right? The root cause of the problem is that when the transistor is in the active region, the gain from here to here has one sign. When the transistor is in saturation because of the effective shot between the collector and the base, the sign of the gain is the opposite sign, correct?

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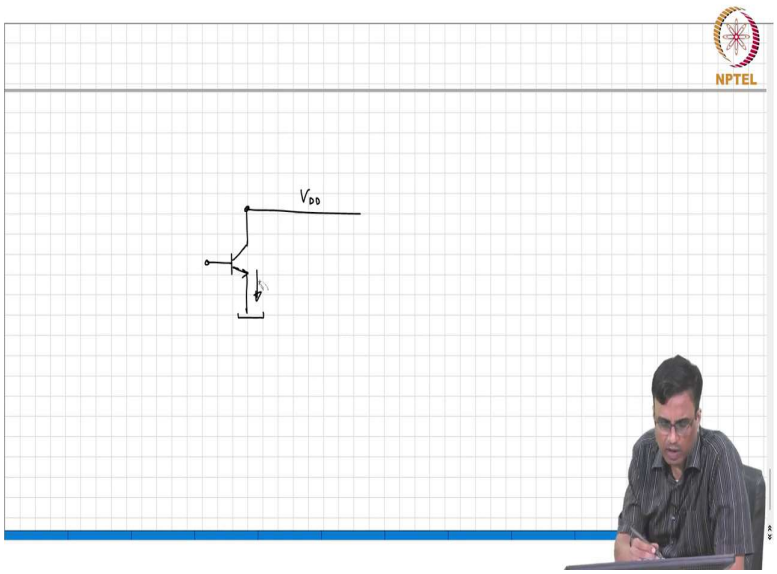

So, basically, the root cause is the fact that we are taking what the transistor is doing, which is basically converting this voltage to a current and pushing that current through a resistor, right? So, the root cause of the problem is the fact that we are taking the output at the collector, correct?

I mean, if we didn't look at the collector terminal at all, if we found some other way of taking that current in the transistor and passing it through a resistor, then you know the problem would be I mean, the root cause of the problem is that we are looking at the collector terminal as the output. So when the transistor saturates, we are in trouble. So, the thinking was, therefore, that this led to the thought that, well, the collector current and the emitter current are the same, correct?

So, if I, you know, tapped off the emitter current rather than the collector current and passed that current through a resistor, then I would be able to get there is no issue because I am not messing with the collector at all. So, I will actually ground, I mean increment, I mean collect, connect the collector to V_{DD}, and only look at the current through the emitter, but there is a problem, right? So, if you want a current, by which I mean a current source, what should the output resistance of the current source be?

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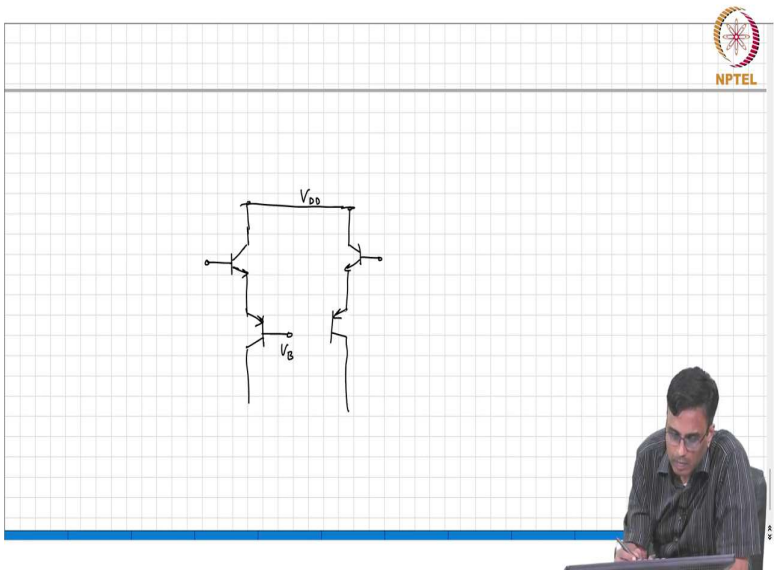

If you want a current source, In other words, when you are looking at the collector, what is the output resistance looking like here? When the source is grounded, what is the incremental impedance looking into the collector when the transistor is active? It behaves like a voltage-control current source because the output impedance is infinite, which is correct.

Now, if you say ok I am going to look for you know current in the emitter what comment can you make about the incremental output impedance here? $1/g_m$ is actually a very low impedance, right. So, you want a current source so that you can push that current through a resistor to get a lot of voltage gain. But, unfortunately, our so-called current has a very low output resistance. So, you know. So, if you want to take a current with a low output impedance and make it look like a current with a high output impedance, what kind of control source will be used? current control current source So, what kind of current control current source will you use? What is the simplest current control single transistor current source you know?

Student: Common base.

Common base. So, do you want to use an NPN common base or a PNP common base? If current is flowing like this, use a PNP common current common base amplifier, right?

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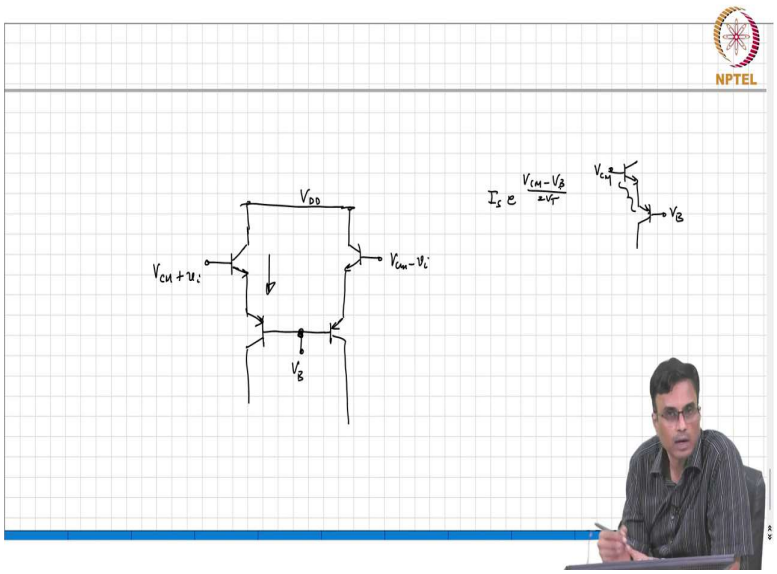

So, V_B. Yes, ok If you put NPN, what will happen? We will see that the advantage of using PNP is that the same quiescent current can flow through the PNP transistor as well. You can also fold. I mean, I think that is also possible, but does this make sense? Ok so, now this represents a current source, right. So, if I apply an incremental v_i here. So, let say this is V_{CM} + v_i, this is some bias voltage V_B this is V_{CM} - v_i. What comment can we make about the quiescent current here first? Let us assume all the transistors are the same saturation current I_s.

$$I_s e^{\frac{V_{CM}-V_B}{2V_T}}$$

Yeah, so, basically simply by symmetry this is V_{CM}, this is V_B, correct? So, by symmetry the voltage in the middle will be half. So, this is basically (V_{CM} - V_B)/2 V_T, correct?

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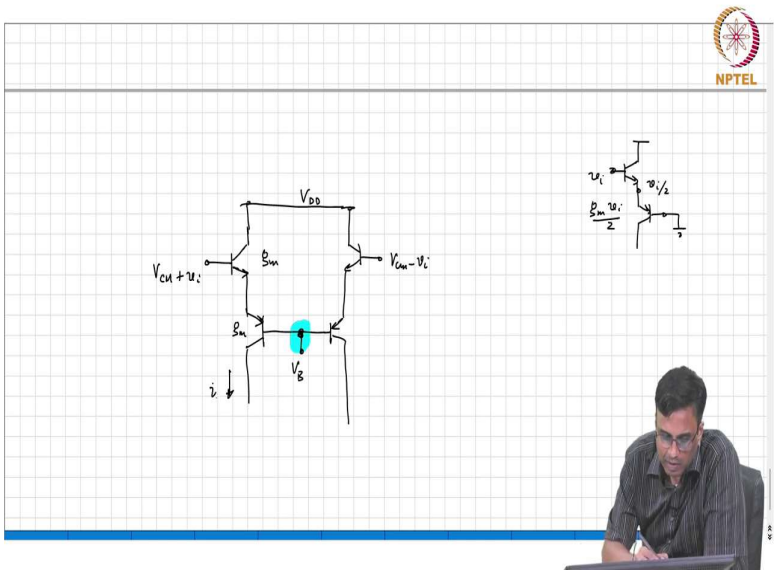

So, there is some quiescent current, and what comment if you assume that the gm of these transistors is denoted by gm? Now, what comment can you make about this incremental current? Let us assume beta is infinite. What is this voltage for incremental signals? It is ground. So, basically, what you have is something like this, ok? So, this is v_i, this is ground. I am interested in finding this current I, that is g_m $v_i/2$ correct. So, this is nothing but this voltage is $v_i/2$ by symmetry, correct?

So, this will be g_m $v_i/2$. So, that is the current that is flowing here, small signal current there is g_m $v_i/2$, ok. So, ok now I get a lot of gain. What kind of load do we want to use? Do we want to use a resistive load or do we want to use something else?

Student: Active load.

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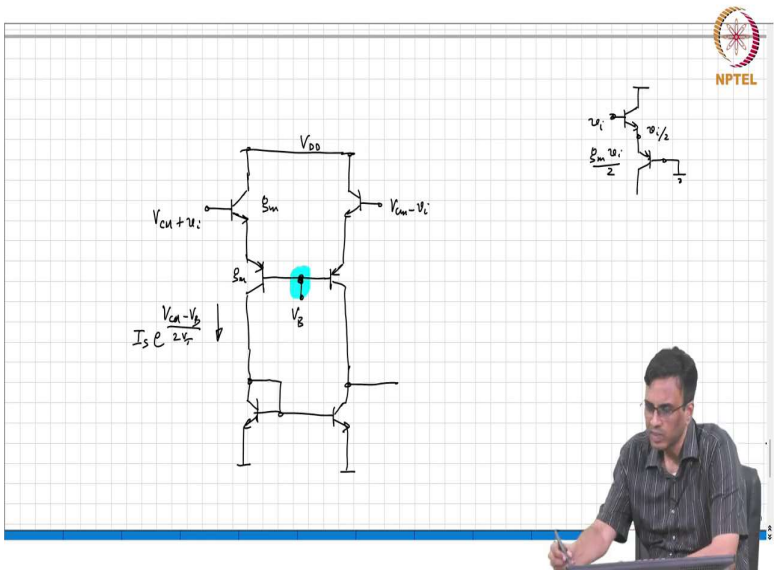

So, basically, you know, one way of doing this would be to just put an active load like this. But now there is a problem, and the problem is the following: So, as you can see, the quiescent current here is exponential.

$$I_S e^{\frac{V_{CM}-V_B}{2V_T}}$$

So, if the input common mode changes what comment can you make about what you know about the quiescent current flowing through the transistors. If V_B is fixed and the input common mode changes the quiescent current will change exponentially, right. I mean at a pinch if it goes up you may be happy, but if V_{CM} goes low a little bit then the current will know you basically you will have almost 0 current in the transistors, correct?

And, compare that with the conventional differential pair when we change the common mode voltage what comment can you make about the current in the transistors here? It does not change, correct? So, here therefore so, so, if we simply did this right why did we do this to avoid the problem of changing? What was this, what was this, why did we go to this in the first place?

So, basically the output would latch right because of the change of the sign of the feedback. So, we said we are going to take the current from the emitter rather than the collector. Now, we have a new problem, right? The problem is that the bias of the common base point right if

it is fixed then if the common mode varies well the current will also vary which is no good right, we want the quiescent current in the transistors to be constant, right so, ok.

So, how do we fix the problem? If V_{CM} changes and we want the quiescent current to remain the same, what do you think we should do? We should also change, so that the current flowing in the transistors is the same, correct? The quiescent current flowing in the transistors is the same alright. So, in principle what will we do? I mean we cannot measure the change in V_{CM} because it is coming from outside, we have no such thing, right? What do we want finally? We want the sum total of the currents in the two transistors of the input pair to be that is what this guy is doing, correct? What is happening here?

The sum total of the two currents in the quiescent currents in the input pair is always maintained to be a constant. So, we would like to do the same thing. The same thing has to be done here.

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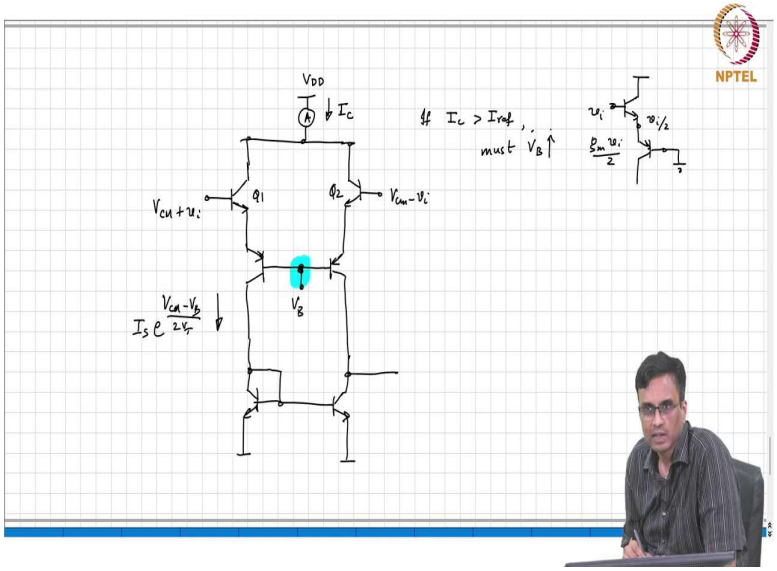

So, we want to find the sum of the currents quiescent currents in transistors Q1 and Q2 and tweak the base voltage, so that the sum of the currents always remains constant right equal to some reference current. So, where can we find the sum? Is there some way of finding where you can put an emitter to find the sum of the two currents in the transistor of, I mean the sum of $IQ_1 + IQ_2$? What do you think we can do? Where can we measure? Ok so, a good place to measure is the collector.

So, in principle what you would like to do is put an emitter here to measure the current I_C. If I_C is greater than I_{ref} right, which is the constant current you want to flow in the input pair. If I_C is greater than I_{ref}, what does it mean? It means that V_{CM} is too high, right? So, in other words you have no control over V_{CM}, it is only V_B. V_B is too low and what should you do? You increase V_B and vice versa. So, if I_C is greater than I_{ref} must increase V_B, ok. So, basically, we need to therefore, you know find I mean you know you need to compare I_C with I_{ref} what is comparison?

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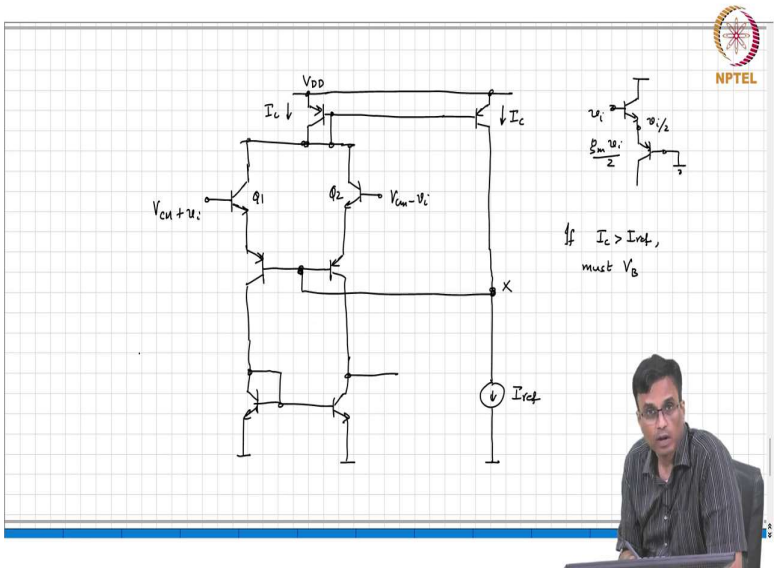

Use KCL to compare, but so, basically you make. So, one way of doing this is to make a copy of this current. How do you make a copy? Current mirror, right. So, this is the current mirror, ok and then you will compare this with I_{ref}. So, this is I_C, this is also I_C ok. So, this is I_{ref} if I_C is greater than I_{ref} we must increase V_B for what happens to this node x?

If I_C is greater than I_{ref} node x increases. So, what should we do? Well, the easy thing to do is simply connect I_C to the right. So, this is basically a feedback loop always comparing the total current in the input pair to I_{ref} and changing V_B in the right direction and the right amount, so that the current quiescent current is always equal to I_{ref}, ok. So, this basically solves the problem of the transistor going into saturation then causing the negative feedback loop to become positive feedback. Does it make sense? If you are able to see this, it is an incredibly clever idea and something that is not obvious at all.