Analog Electronic Circuits
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Lecture - 82
Bipolar Junction Transistor Circuits Swing Limits and Two-Stage Op amp

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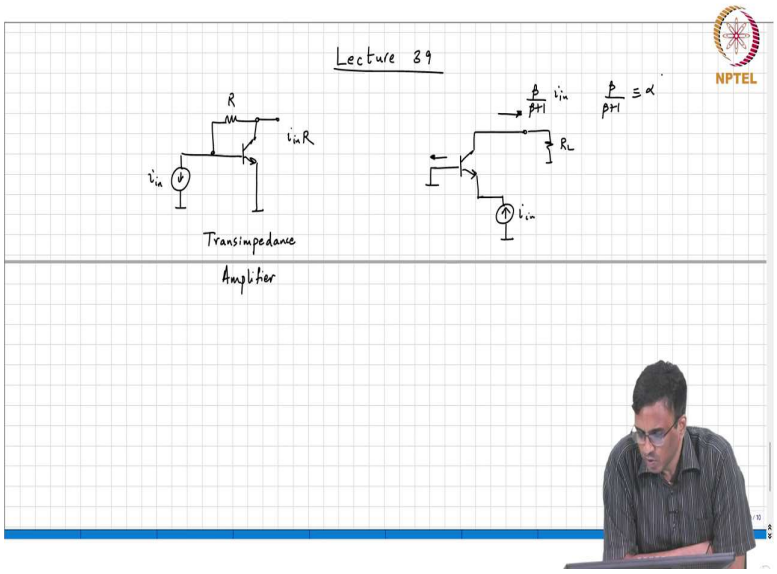

Good evening, everybody, and welcome to Analog Electronic Circuits. This is lecture 39. So, in the last class, we were looking at going over pretty much all that we did with MOS transistors, but we were doing it with bipolar transistors. And the first, I mean, we were looking at the voltage-controlled voltage source that is the common collector amplifier, and there is, you know, a small departure from the MOS transistor case because the input current in the base is not zero.

So, consequently, the input impedance of the common collector amplifier is not infinity, right? It has some large value, but it's not infinite. Likewise, if you do the voltage control of a current source, it's the same story: the input impedance should have been infinite, but in reality, it is not. Then, moving on, this is the small signal equivalent of the current-controlled voltage source.

So, the output voltage will be assuming that the g_m of the transistor is infinite or very large. What will be the incremental output voltage? It's simply i_{in} R ok and this is the trans

impedance amplifier, ok. And finally, we have the current-controlled current source, and analogous to the common gate amplifier, we now call it the common base amplifier. This is the input current source, right? And what would be the output current?

Yeah. So, I mean, if β was infinite, like in the MOS, you know, if β was infinite, then it would have exactly the same equivalent as the common gate amplifier, and therefore, the output current would simply be equal to i. Now, you know a small fraction of that input current goes out through the base, and that's basically it. So, what comes out is $\beta/(\beta + 1)\, i_{in}$ and remember that $\beta/(\beta + 1)$ is defined to be this quantity α.

So, α is understood. I mean you know one way of defining α is basically the current gain in the common base configuration. Now, like in the MOSFET case you know the two transistors.

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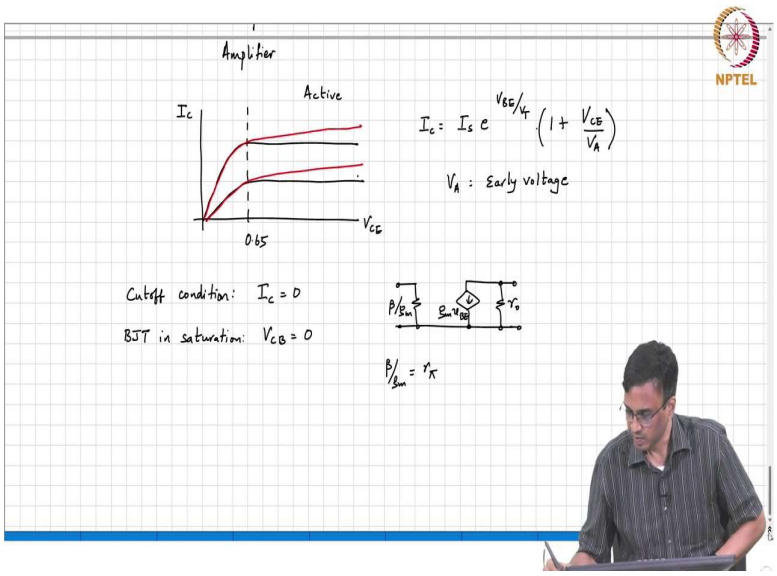

Ideally the output characteristics are I_C versus V_{CE} right for different values of V_{BE}. But remember that what you call the current is so sensitive to V_{BE} because exponential right. So, rather than you know control V_{BE} you know people find it easier to control I_B right. So, these are plotted for various values of I_B and so, this is the 0.65 volts V_{CE} minimum and so, ideally the curves must be flat right. So, the collector current in the active region is independent of V_{CE} right. But in reality, well they and this is grossly exaggerated, but I think you get the idea right. So, the current is like that. So, like in the MOSFET case the collector current is I_s $e^{(VBE/VT)}$.

We could have written $1 + \lambda V_{CE}$ right. But you know historically the fellow who first came up with this equation basically said it is V_{CE} by some V_A right and V_A is called the as called the early voltage after the person who came up with this first right and V_A is basically analogous to $1/\lambda$. λ units are per volt V_A units are volts.

So, therefore, the model for the transistor is actually this β over g_m and β over g_m is often called r_π this is $g_m V_{BE}$ this is r_o, ok. And it also turns out that there is actually very large resistance between the base and the collector right that also results in some y_{12} which is again undesired and actually is very small, but for most practical calculations we will just neglect that because the this becomes it say that resistance is very very large and it messes up calculations big time.

So, we just move with this, ok. So, this is the NMOS transistor and for as far as swings are concerned the cutoff condition is what is the cutoff condition in the MOS NMOS for the NMOS transistor? I_{DS} if the drain current was 0 now the collector current is 0 and likewise you know so, the BJT going into saturation, what is the condition?

I mean V_{CE} minimum is 0.65 and V_{BE} nominal is 0.65. So, what is that in English? What does that mean? The collector can go as not up to as low as the base right. So, in a MOS transistor the drain can go one threshold below the gate whereas, in a bipolar transistor the collector can go as low as the base. So, $V_{CB} = 0$, ok. So, I mean you know again as usual if you see big you know big circuit well the procedure is very straightforward you first find the; first find the operating point replace every transistor with its incremental equivalent and what do you call do the small signal analysis, then you know then you can find the total voltage everywhere the total current everywhere.

And then to find the cutoff condition for the for a given transistor you set you know I_C equal to 0 to set you know the stuff going into for the set to figure out the condition when the transistor goes into saturation you know you set V_{CB} you know figure out when the for what value of input amplitude the drain the collector will become equal to the base potential.

And therefore, you know that will give you 1 limit. So, for each transistor again you will have 1 limit and if you have 100 transistors you will have 100 limits you have to find the minimum of all the minima that you have found ok. Now, if you have an N NPN transistor you know we said that if you just had NMOS transistors only then the scope for design is limited, right.

So, in that respect the PMOS transistor was greatly helpful because its characteristic is complementary likewise, you know it's not surprising that you know if you had an NPN device there exists a complementary device that is the PNP and that is very fortunate because we can do things with NPN and PNP transistors put together which you could not do with any single time right.

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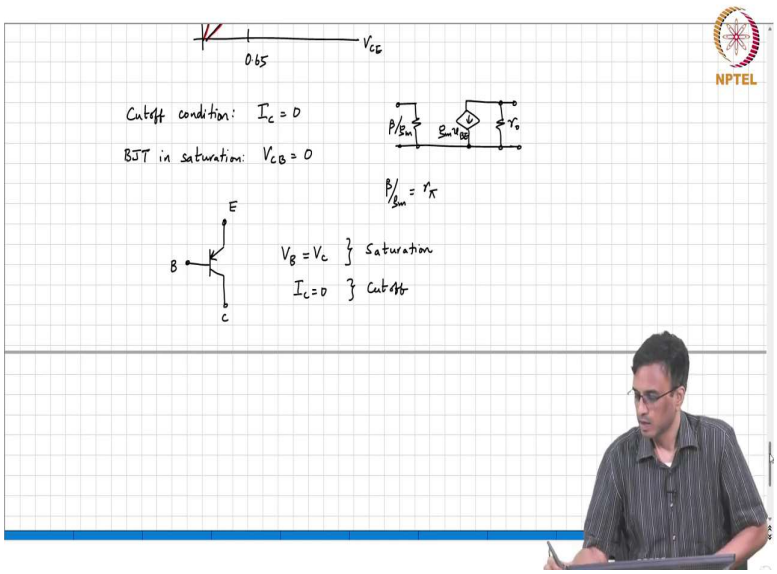

So, basically that the PNP also again you can see that I mean the logic behind drawing the symbols is also very clear the arrow is always drawn in the direction of flow of current of the total current not the incremental current. The incremental current could be flowing in the opposite direction, but the total current flows in this direction. So, this is the emitter, this is the base and this is the collector and just like how an N you know you know an NMOS circuit can be turned into a PMOS circuit and all we do is basically you know first set V_{DD} to - V_{DD}, right.

Then add V_{DD} to all nodes likewise you know to convert an PNP- NPN circuit into a PNP. Once you change V_{DD} to - V_{DD} and we do not like negative potential. So, we add V_{DD} to all nodes and of course, we do not like currents flowing from yeah you know the bottom of the page to the top of the page.

So, rather than turn the page or turn your head, you basically know you draw the emitters of the PMOS or the PMP transistors on the top and then they flow down, ok. So, now that all of

this is said you know very straightforward and. So, again the cut off condition for PNP I_C is 0 right, what about the saturation condition when the PNP transistor enters saturation. Yeah.

So, basically just like in the PMOS transistors where the drain can go one threshold above the gate in the PNP transistor the collector can go as high as the base, right. If it goes above the base then basically you can see that the emitter collector potential is getting crushed right if the potential becomes too small between the emitter and collector then you cannot have a constant current right. In the limit when V_{EC} is 0 no current can flow.

Because there is no potential difference. So, again the saturation condition is $V_B = V_C$ right and $I_C = 0$ is the cut off current. Now, after we are done with this the next thing to do is basically the differential pair right.

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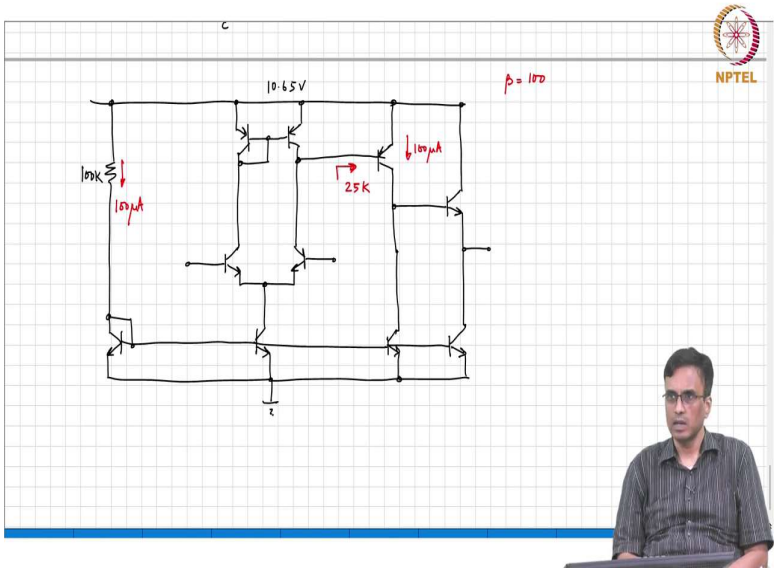

And the motivation for doing the differential pair in the two stages of the op-amp remains exactly the same. So, now let me take some simple examples. This is at 10.65 volts. Let us say this is 100 K and like before we use active load, ok.

So, this is an example of a two stage op-amp right a toy 1, but the basic principles are there and however, there is a; there is a difference between something done with MOS transistors and something done with bipolar transistors. What is the input impedance seen here? By the way, what is the current flowing here?

A 100 micro ampere and that basically if you assume all the transistors are identical this is also 100 micro amperes let us assume the βs are large, right. So, what is the input resistance looking in here? Let us assume β = 100 for instance. What is the g_m of the transistor? $1/g_m$ is 25 milli volts/0.1 milli amperes that is 250 ohms, and 100 ohms is the input impedance. So, that is basically 25 k ohms. So, if this was a MOS transistor what would be the input impedance?

Student: Infinite.

So, the now the you know a practical problem that comes about is that the second stage actually loads the first stage and therefore, the you know the gain of the first stage is going to get reduced because the output load now is now R_{ON} parallel R_{OP} parallel you know what do you call R_{OP} parallel R_{ON} =25K and in all likelihood the 25K is probably going to limit the gain. So, what do you suggest we can do? So, basically you want the input impedance to be higher, you want the same voltage, but the input impedance must be higher.

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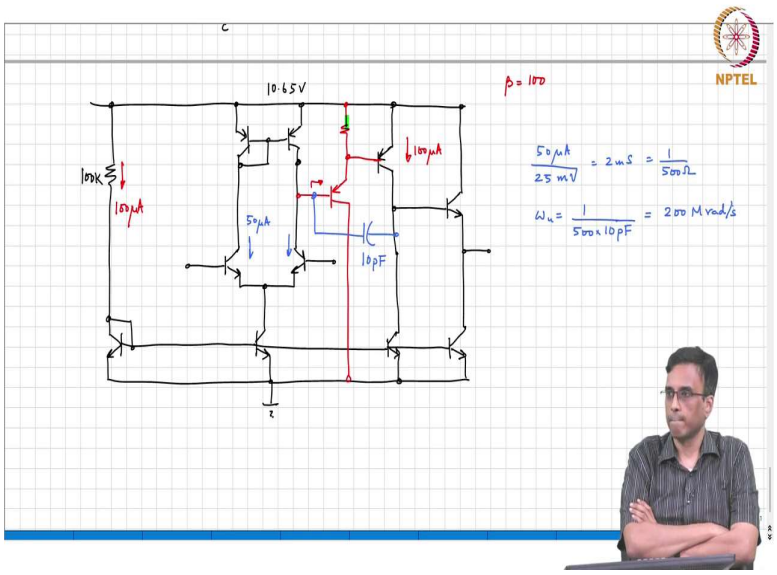

So, what controlled source will you put between these two terminals? Anyway, the problem is you want this voltage to come here, but you do not want any current to be drawn there. So, what do you want to put? In principle you want to put a voltage controlled voltage source. What is the simplest voltage controlled voltage source that you know?

Student: Common collector.

So, will you put an NPN common collector or PNP common collector? So, one way to do this is just do this ok, alright. So, basically the role of this is to increase the input impedance here. That input impedance will increase if this resistor is very large the input impedance will increase by a factor of β. So, that is one thing. And now if you want to make Miller compensate for the system, what do we do?

Basically you could add a CC here ok alright and that I mean. So, basically and this is the and it is very straightforward to. So, let us say this is you know 10 puffs. So, what is the unity gain frequency for bipolar transistors? This is very easy to do. What is the current flowing in each of these transistors? 50 micro amperes. So, what is the GM of the first stage? 50 micro amperes/25.

Basically it is 2 milli siemens. So, which is basically 1/500 ohms correct. So, the unity gain frequency omega u is nothing but g_m/CC which is 1/500 x 10 puff correct which is 200 mega radian per second, ok. So, that is you divide by 6 roughly to get the unity gain bandwidth in megahertz, ok. So, does that make sense to people? So, as you can see it's very straightforward to obtain by simply looking at the picture and just being able to compute what the unity gain bandwidth of the amplifiers is.