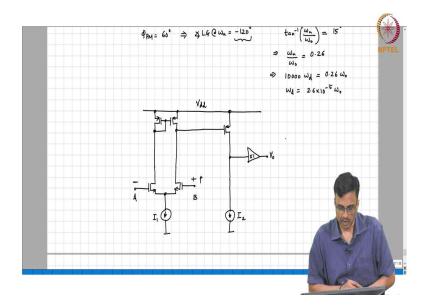
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Lecture - 75 The 2 -Stage Miller Compensated Amplifier

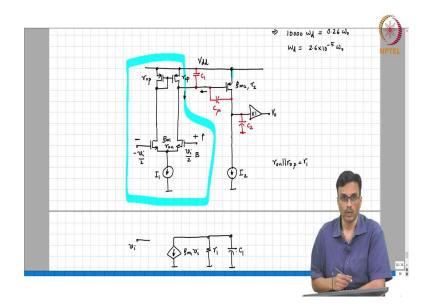
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So, remember long ago we did this 2-stage op amp. Now, all these current sources will be realized using MOS transistors. So, we do not mean at this time being we just assume that there are ideal current sources and here we said that we are going to have some kind of voltage control voltage source that can be either a NMOS or a PMOS common drain amplifier.

So, this is V_{DD} . So, which is the positive terminal of the op amp and which is a negative terminal of the op amp. let us call this A, let us call this B, A is negative B is positive and so, if you hang B up this is going to go down if this goes down this goes up this goes up that goes ok. So, remember and let us assume the output resistance of the NMOS transistor.

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So, let us call that the g_m of each of these NMOS transistors is g_{m1} and r_{on} and this is basically r_{op} is the output resistance of each of these PMOS transistors. And this is $g_{m2} r_2$. I am going to call this r_2 just for it because it is the second stage. So, now, assuming that everything I mean remember that you can never operate an op amp in an open loop it is part of some negative feedback loop.

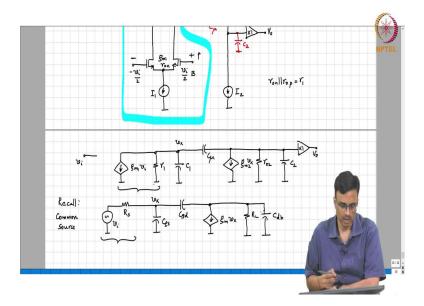
And therefore, the potentials at A and B will be the same and consequently all transistors are operating in saturation. Everybody is happy. So, now, the question is what is the; what is the what do you call this small signal equivalent as far as the what do you call this thing is concerned small signal operation is concerned. But remember that we said that every transistor every node is associated with some parasitic.

So, this is what I am going to call this C_1 and that includes what all parasitics C_1 include the drain parasitic of the input NMOS transistor, the drain parasitic of that PMOS transistor and the gate parasitic of or the second stage ok. So, all of them are in parallel. So, we can basically club every one of them together and so, that is C_1 . Similarly, C_2 is the input capacitance of the next stage and all that stuff.

So, that is basically C_2 ok and so, and there is going to be some small capacitor here which I will call C_{μ} ok. Now, what is the model for the first stage? Remember what we say was the DC gain. So, this is let us call this - $v_i/2$ this is $v_i/2$. So, the differential input is v_i . So, what is the effective current going in here? What is the effective current going in there? That is

nothing but g_{m1} v_i , and what is the output resistance of the first stage? $r_{on}//r_{op}$ which I will call $r_{on}//r_{op}$. I will call r_1 , that is basically r_1 , this is C_1 .

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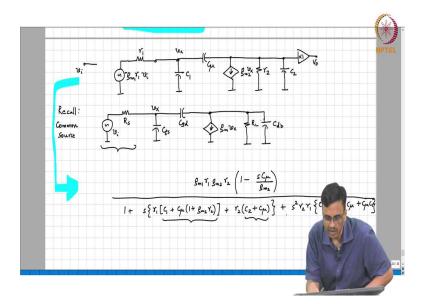


And this is g_{m2} r_{02} C_2 and then there is V_o . I have just kept that output buffer as an ideal VCVS simply. Because remember that the bandwidth of that common drain amplifier is actually very high and we do not have to really, I mean complicate our lives simply well that there will be some bandwidth, but that be so high that we do not worry about. So, this is the model of the whole two stage op amp. I think we have forgotten the g_m , ok. So, does this look familiar? Have we done this before?

Have we done this before? Where have we done it? Yeah, basically this picture is exactly the same as the common source amplifier, remember in a common source amplifier, we had a voltage source a source resistance then C_{gs} . So, this is a common source. So, this is v_i this is R_s this is C_{gs} C_{gd} this was g_m v_x and this was R_L I think and C_{db} .

What is the only difference between I mean apart from changing what we call each one of them this is g_{m2} v_x apart from minor changes the only other change is that here we had a voltage source in series with a resistance.

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Here you have the current source in parallel. So, what can we do? Yeah, well I mean if you want to just use the same formula this is simply r_1 and $g_m v_i g_{m1} r_1 v_i$, ok. So, ok so, what was the I mean can we just simply look at this and write down the formula. What is the DC gain?

So, what is the DC gain? Not this one we have already done. I am asking you for the one upper one. What is the point of redoing the one which you have already done? Before So, this is going to be r_1 g_{m1} g_{m2} r_2 (1-s C_{μ}/g_{m2})/(1 + s { r_1 [$C_1 + (C_{\mu}(1 + g_{m2} r_2)] + r_2 (C_2 + C_{\mu})$ } + $s^2 r_2 r_1$ { C_1 C_2 + C_2 C_{μ} + C_{μ} C_2 }). I mean this is just the same expression that we have done earlier except that we replace R_s with r_1 , r_2 with r_3 , r_4 with r_5 , ok.

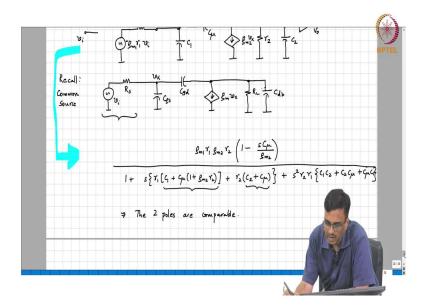
So, the DC gain of the op amp as expected is g_{m1} r_1 g_{m2} r_2 as right half plane 0 there are two poles correct. So, now the question I am going to ask you is obviously, there is a second order system. And there are two poles. What comment can we make about the locations of the two poles in other words are the two pole locations here I like comparable or are they like see r_1 C_1 r_2 C_2 etcetera will all be comparable because C_1 C_2 are parasitic of the transistors r_1 r_2 the output resistances they will not be the same, but they will be; they will be comparable.

So, with that what common can we make about the relative locations of these two poles of the two poles of the system. Why? But C_{μ} is also a small number. So, that is what the C basically all that this is saying is it this and this are comparable with are comparable to each other in other words means or in other words see if that C_{μ} was not there what common can we make

you have a first stage which is got a pole at r_1 C_1 second pole second system is got a pole at r_2 C_2 .

Because C_{μ} there is some small interaction, but the two poles are comparable there is no I mean it's not as if one is much faster than the other or one is much slower than the other there they can be expected to be roughly near each other, ok.

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So, in other words for all practical purposes therefore, two poles are comparable. So, the two poles are comparable. I mean we can use our earlier analysis where two poles are comparable basically means that they are somewhat close to each other.

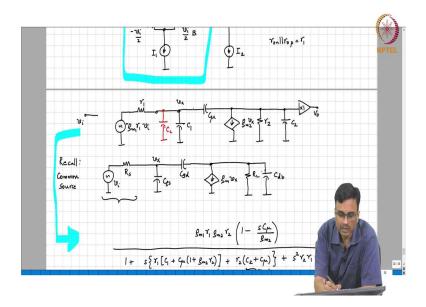
So, what happens if you enclose this op amp in a negative feedback loop is to get an idea of what happens. You can imagine that the two poles are the same. What will happen when you close the loop if the two poles are exactly the same. We have done this before. You have to have two pole systems where both the poles are at the same location. What comment can we make about the closed loop system? But what is the problem?

So, the quality factor is closed. So, if we just use the op amp as if the closed loop system might technically be stable, but in reality, the quality factor of the closed loop poles is A_o in this case is $g_{m1} \ r_1 \ g_{m2} \ r_2$. So, square root is basically of the order of $g_m \ r$ I mean $g_m \ r_o$ whatever is feedback factor there.

And therefore, what do you call the closed loop system is we will have a Q which is of the order of g_m r/2. If g_m r = 100, I mean some maybe 40 or 50, g_m r/2 will basically be something like 20 a closed loop system will have a Q of 20 that basically means it will ring 20 before it dies down does it make sense? So, for all practical purposes therefore, this op amp is unusable as it stands. So, what do we do to make it usable?

What is the principle? We introduce a dominant pole, ok. So, that these two poles can be widely separated does it make sense? Ok. In other words, the dominant pole is much lower than the other pole. So, as slowing something down is very easy, what do you think we can do? We can take a big fat capacitor and there are and we can place it in parallel with any one of the capacitors that are already there.

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For instance, we could place a big fat capacitor in parallel with let me call that C_c in parallel C_1 or parallel with C_2 or in parallel with either C_1 or C_μ or C_2 ok. There are three possible choices. Then somebody brightly came up with the idea that I will do both C_1 and C_2 . What is your opinion?

Both will shift close, which is no good. So, you only want to put it across either one of these. So, you have three choices correct ok. So, which do you think is the smartest thing to do? Well, by symmetry whether you do it to C_1 or C_2 it looks like it does not matter much. So, why do you say C_{μ} ?

So, basically as you can see if for a fixed amount of capacitance. So, if you add capacitance just in parallel with C_1 , C_1 will become $C_1 + C_x$. So, this term will become what you call the time constant and will increase by r_1 C_x that you add. Whereas, if you add it in parallel with C_μ you can see that capacitance is getting multiplied by the effect of C_μ is getting electronically multiplied due to the Miller. It's very easy to understand what this Miller effect is. So, let us say you have to say Usain Bolt is running at Bolt or Bolt or whatever he is running Buku fast.

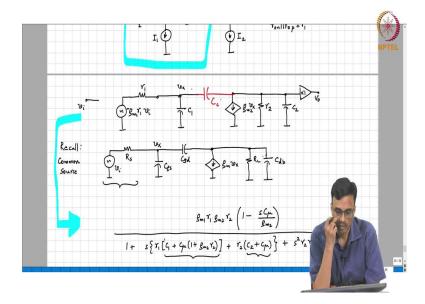
So, how can you slow him down? Well, you can say well it's very easy to take a bag of sand and you are tied up to one of his feet or you can tie to his foot or you can tie to his hands ok and then automatically it will slow down that is what capacitance does ok. But I do not know if you have watched the news, but sand is very expensive and sand is silicon. So, just like the silicon area, it's very expensive. So, you want to be able to slow him down to the same extent by using the least amount of sand correctly. So, what do you do? So, you watch the video in slow motion.

And then you recognize that every time Usain Bolt runs, his hand is running this way and his leg is kicking that way both of them and the opposite direction. So, you get the smart idea that I will try a thin string between his arm and his leg. So, he is basically slowing himself down. I do not have to really put too much sand that is basically what is happening with the Miller effect.

Why is this what is this big deal? What is the electronic multiplication of capacitance? Why is a small capacitor made to look big? Why? Because when the gate is going this way the drain is going the opposite way. So, if you put an elastic between the two then both of them are trying to pull towards each other. Therefore, slowing the whole system down.

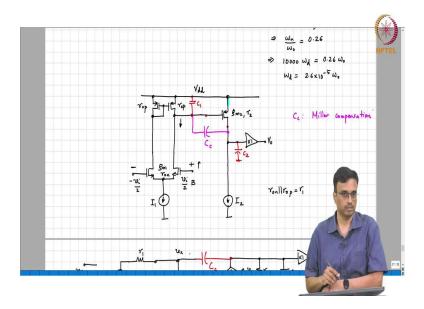
So, the basic principle behind a Miller effect is that if this goes up this is going down by a large factor and therefore, even though you are putting only a small capacitance the amount of current that is flowing through C_{μ} (1 + g_{m2} r_2) factor.

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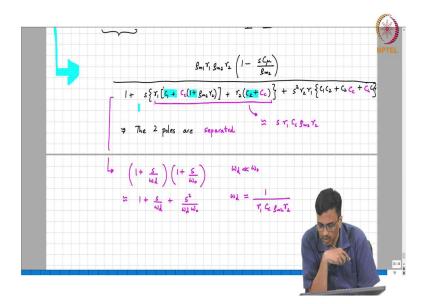
So, the smartest thing to do is basically say well neither C_1 or C_2 get anything we just simply take to replace. I mean you put a big fat capacitor and put it between the gate and the drain of the second stage.

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So, that is basically so, this is the C_c . So, C is the Miller compensating capacitor which introduces the dominant pole.

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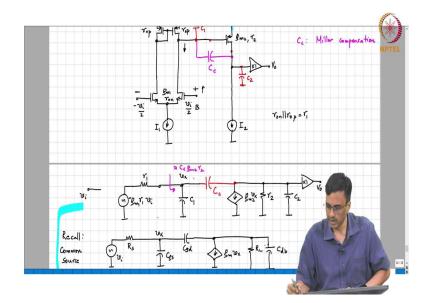


So, this becomes C_c this becomes C_c this becomes C_c . And by introducing C_c what have we done? We have shifted the poles apart. So, that the two poles are separated from each other. So, now, if the two poles are separated, they must be of the form. So, this is approximately therefore, equal to $1 + s/\omega_d + s^2/\omega_d\omega_o$ So, that basically that s/ω_o term can be neglected and basically you have $s^2/\omega_d\omega_o$. And so, what is ω_d ? What is ω_d ?

It is basically its 1 over all this entire term. So, which of these terms can be neglected? Well in the second term we can neglect C_2 and in the first term you can neglect C_1 you can neglect 1 and so, basically you have r_1 C_c C g_{m2} r_2 and you have r_2 C_c . But if the r_1 and r_2 are comparable, what can you neglect? I mean g_{m2} r_2 r_1 C_c and then r_2 C_c which is which can you neglect?

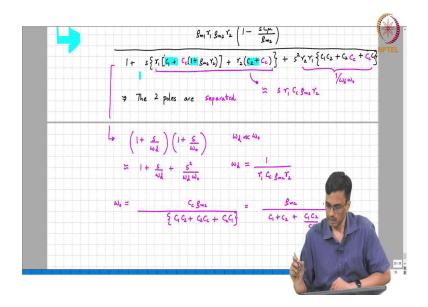
This is basically approximately equal to s r_1 C_c g_{m2} r_2 . So, what is the dominant pole? $1/r_1$ C_c g_{m2} r_2 . Does it make sense? Ok. I mean why does I mean of course, this comes out of the math, but is there an intuitive way simply looking at it and figuring out why it makes sense?

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What is the capacitance looking in here? C_1 in parallel with C_c . $(1 + C_c) (1 + g_{m2} r_2)$. So, if $g_{m2} r_2$ is very large, $1 + g_{m2} r_2$ is the same as $g_{m2} r_2$. So, the capacitance is approximately equal to $C_1 + C_c g_{m2} r_2$ which is approximately equal to $C_c g_{m2} r_2$ and the resistance is r_1 . So, the pole at that first node is going to be $1/r_1 C_c g_{m2} r_2$. So, it makes sense that the dominant pole being $1/r_1 r_2 C_c g_{m2}$ that makes sense. I mean the second pole, of course, is far away. So, if the dominant pole is concerned this is all that we need to worry about.

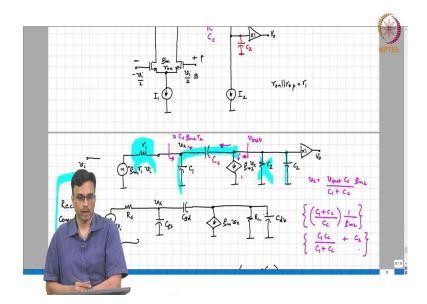
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So, what is the second pole therefore? What is ω_o ? So, basically, we know this is the product of the two poles. So, what should we do? This is nothing but ω_d ω_o . So, ω_o therefore, is nothing but sorry this is nothing but $1/\omega_d$ ω_o . So, what is ω_o ? It's $1/r_1$ r_2 C_1 $C_2 + C_2$ $C_c + C_c$ C_1 . This r_1 C_c g_{m2} r_2 . So, fortunately these two guys went away ok.

So, let me write it in a slightly different way. This is $g_{m2}/C_1 + C_2 + C_1 C_2/C_c$. So, why does this make sense? Ok. Let us take a look.

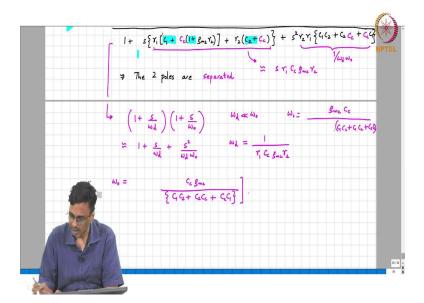
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So, basically at frequencies much beyond the dominant pole. Will which of these impedances dominate, which one will be higher? The resistance or the capacitor? The capacitor. So, at very high frequencies therefore, one need not worry about current through the resistors at all whether it is this resistor or that resistor.

So, the question is what is the pole frequency because of the rest of the circuit? Ok. So, what is the resistance looking in here? What is the impedance looking in there? What is v_x ? If I apply a test voltage here, what is v_x ? Yeah, that is nothing but $v_x = v_{test}(C_c/C_1 + C_c)$ g_{m2} . So, what is the current flowing here? So, what is the resistance looking in? It is nothing but $(C_1 + C_c)/(C_c)$ (1/g_m) that is the resistance looking in there. And in a part from this, there is also current flowing through that guy. What is that current? It is just C_c and C_1 in series. So, what is the effective capacitance looking in there? $C_1 C_c/(C_1 + C_c) + C_2$.

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So, what is the pole frequency? Therefore, ω_o , therefore, must be $1/r_c$, $=g_{m2}$ $C_c/(C_1$ $C_2 + C_2$ C_c + C_1C_c). So, basically this C_c comes here. This g_{m2} $C_c/(C_1$ $C_2 + C_2$ C_c + C_1C_c) C_c and that is basically that is that is basically what? The expression you get after running through the algebra is what you get.

But the intuition behind why you get this result is that at high frequency, the current flowing through r_1 and r_2 are all negligible. And the system you have is basically just C_1 C_c g_{m2} and C_2 and the time constant corresponding to the pole frequency corresponding to that system is now this expression over here. So, I will stop here and we will continue in the next class.