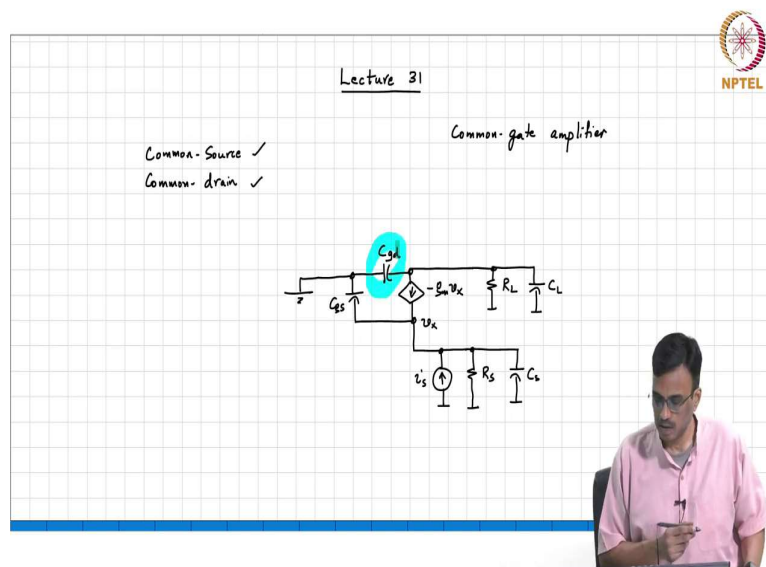


**Analog Electronic Circuits**  
**Prof. Shanthi Pavan**  
**Department of Electrical Engineering**  
**Indian Institute of Technology, Madras**

**Lecture - 65**  
**Frequency Response of the Common-gate Amplifier**

(Refer Slide Time: 00:18)



So, in the last class we were looking at the Frequency Response of some commonly used amplifier stages that we have dealt with. And so, we looked at the common source amplifier and then we also looked at the common drain amplifier. And, we concluded yesterday that the bandwidth of the common drain amplifier is expected to be much higher than that of the common source amplifier.

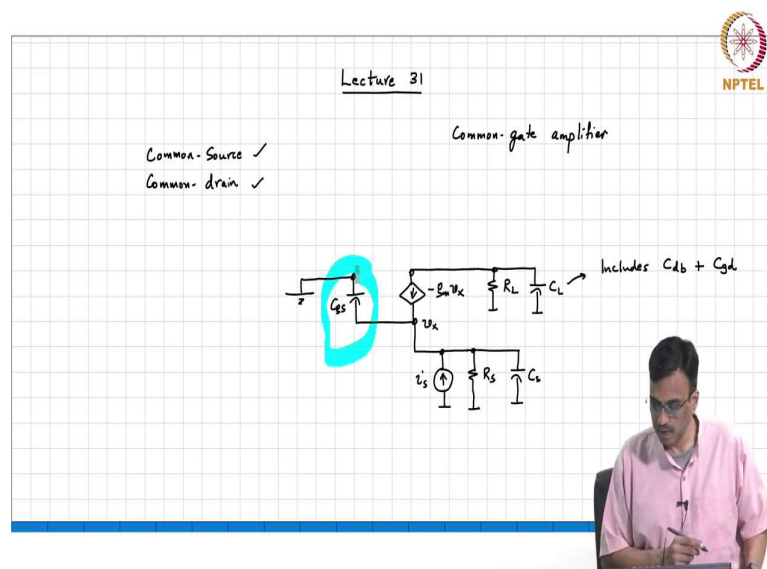
And, intuitively that makes sense because well none of the nodes in the common drain amplifier are swinging very much. So, the parasitic capacitances of those nodes need to be charged and discharged only to a much smaller degree. And as a consequence, the you I mean since the currents pumping into those nodes are roughly the same, it basically means that the capacitor current can be supported to a much higher frequency right without a loss of amplitude.

Because  $Cdv/dt$  is the current flowing through the capacitors, right. You only have some current, some  $g_m$  something you can push into those nodes, correct. So, if your voltage swings are small, that basically means that you can increase frequency and still be able to maintain

the same voltage you know for a given current. That is basically that is pretty much all that there is to it.

Now, let us look at the common gate amplifier and again, this is the small signal equivalent,  $C_{gs}$  and this is some  $R_L$ , this is  $v_x$ , this is  $-g_m v_x$ . And let us say that this is an input source and it has got some output resistance  $R_S$  and perhaps you know some capacitance  $C_S$ , alright and, some load capacitance say  $C_L$ . And  $C_{gd}$  and  $C$  drain to substrate as drain to bulk would be in parallel with  $C_L$ , right. So, what comment can we make about  $C_{gd}$ ? Can you club it with any of the other capacitances? It can be clubbed with  $C_L$ .

(Refer Slide Time: 03:50)



So, basically when I say  $C_L$  it includes  $C_{db}$  and  $C_{gd}$ , ok. And so, what comment can you make about  $v_x$ ? And likewise by the way, what comment can you make about  $C_{gs}$ ? Can we club it with something else?

Student: Yes.

Alright. So, basically this includes. So, therefore, you can club this and say this includes  $C_{gs}$ .

(Refer Slide Time: 04:25)

Common-Source ✓  
Common-drain ✓

Includes  $C_{db} + C_{gd}$

Includes  $C_{gs}$

$$\frac{V_x}{I_s} = \frac{\left(\frac{1}{g_m} \parallel R_S\right)}{1 + s C_S \left(\frac{1}{g_m} \parallel R_S\right)}$$

$$\frac{V_o(s)}{V_x(s)} = \frac{g_m R_L}{1 + s C_L R_L}$$

$$\frac{V_o}{I_s} = \frac{\frac{1}{g_m} R_S}{\frac{1}{g_m} + R_S} \cdot \frac{g_m R_L}{(1 + s C_L R_L) \left(1 + s C_S \left(\frac{1}{g_m} \parallel R_S\right)\right)}$$

So, what comment can you make about  $V_x$ ? What is  $V_x$ ? Ok, what is the impedance looking in there?

Student:  $1/g_m$ , ok.

So, what is  $V_x$ ? For DC, what is it? It is for DC it is nothing but  $1/g_m$  in parallel with  $R_S$ , alright. And as frequency varies, what will the voltage be?  $(1 + S) C_S(1/g_m \parallel R_S)$ , ok. So,  $V_o(s)/V_x(s)$ , therefore, is simply seen to be  $g_m R_L$ . So, what is the output voltage therefore?

Student:  $S C_L R_L$ .

Ok. So, what is the  $V_o/I_s$ , therefore? What is the DC gain? Basically  $1/g_m R_S / (1/g_m + R_S)$ . That is the formula of two parallel resistors, very nice. Ok, this  $g_m R_L / (1 + s C_L R_L) (1 + s C_S ((1/g_m) \parallel R_S))$  and you know first, ok. So, I will just write the whole expression then we can approximate, ok. So, what is this now? This and this go away and. So, you have  $R_S / (R_S + 1/g_m)$ . So, under the usual condition that if you want to build a good common gate amplifier, what comment can we make?

(Refer Slide Time: 08:12)

Common-Source ✓  
Common-drain ✓

$$\frac{V_o}{I_s} = \frac{\left(\frac{1}{g_m} \parallel R_S\right)}{1 + s C_L \left(\frac{1}{g_m} \parallel R_S\right)}$$

$$\frac{V_o(s)}{V_e(s)} = \frac{g_m R_L}{1 + s C_L R_L} \approx 1$$

$$\frac{V_o}{I_s} = \frac{R_S \parallel \left(\frac{1}{g_m}\right)}{\left(\frac{1}{g_m} + R_S\right) (1 + s C_L R_L) (1 + s C_S \left(\frac{1}{g_m} \parallel R_S\right))}$$

NPTEL

$g_m R_S$  is much much larger than 1 which basically means that  $R_S$  is much, much larger than  $1/g_m$ . So, in which case this quantity approximately equal to 1, alright, ok. And what comment can you make about that?  $1$  over  $g_m$  parallel  $R_S$ , what will dominate? So, if you have two large, they are two resistors in parallel and one is much larger than the other. So, what is this, how do you approximate this  $1/g_m // R_S$ ?

(Refer Slide Time: 09:01)

Common-Source ✓  
Common-drain ✓

$$\frac{V_o}{I_s} = \frac{\left(\frac{1}{g_m} \parallel R_S\right)}{1 + s C_L \left(\frac{1}{g_m} \parallel R_S\right)}$$

$$\frac{V_o(s)}{V_e(s)} = \frac{g_m R_L}{1 + s C_L R_L} \approx 1$$

$$\frac{V_o}{I_s} = \frac{R_S \parallel \left(\frac{1}{g_m}\right)}{\left(\frac{1}{g_m} + R_S\right) (1 + s C_L R_L) (1 + s C_S \left(\frac{1}{g_m} \parallel R_S\right))} \approx \frac{R_L}{(1 + s C_L R_L) (1 + \frac{s C_S}{g_m})}$$

NPTEL

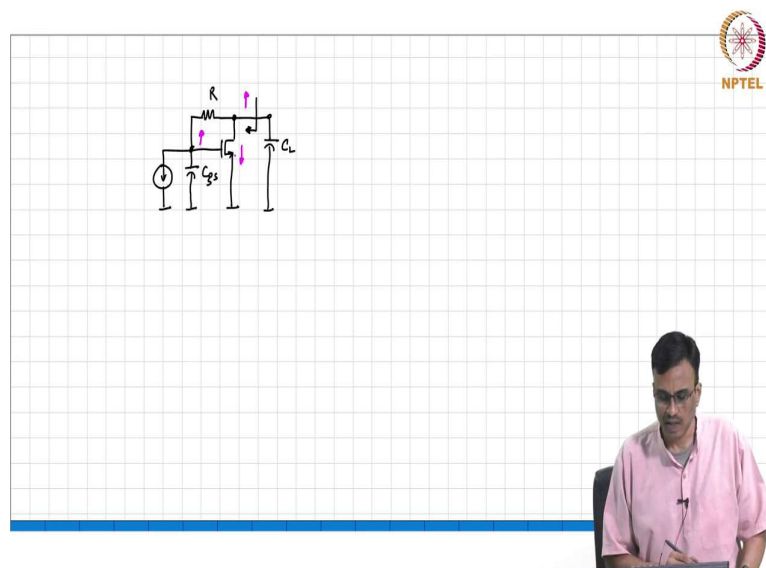
So, this approximately  $R_L / (1 + s C_L R_L) (1 + s C_S / g_m)$ , ok. So, in the special case that  $C_L$  is 0. So, you are like you are only pumping the output and feeding only a resistive load, right.

Then you will basically get the inherent speed of the common gate amplifier, right, in this way.

And, if  $C_S$  becomes 0, right, in other words  $C_S$  remember includes the contribution from the source as well as  $C_{gs}$ , right. So, if the contribution from the source itself becomes 0, then the only thing left in  $C_S$  is  $C_{gs}$ . So, you can see that just like in the common source, I mean common drain amplifier, this becomes  $C_{gs}/g_m$ , alright.

So, this basically is a, you know, this is typically going to be much larger, that time constant is going to be much smaller than  $C_L R$ , ok. And, again that makes sense, which of these nodes is charging up and down a lot, this one or this one? Yeah, basically I mean the swing at the source, the incremental swing at the source is very small, right. I mean ideally if  $g_m$  tends to infinity that swing is 0, correct. And, but that current is getting converted into voltage at the drain and therefore, that voltage is going to be swinging a lot and consequently, you know, the speed limitation is going to come from that node, you understand? Ok.

(Refer Slide Time: 11:00)



So, finally, let us take a quick look at the transimpedance amplifier, ok. I am not going to sit and do a full blown analysis, I leave it to you as an exercise, ok. Quick intuitive analysis, what is the time constant associated with  $C_{gs}$ ? You have a capacitor, what will be the time constant associated with that capacitor?

Yeah, you calculate the equivalent you know impedance, you know, resistance across that capacitor, what is the input impedance of the, you know, in the form that I have, we have drawn it, what comment can we make about the input resistance is  $1/g_m$ . So, what comment can we make about what you call, that the time constant is associated with the with  $C_{gs}$ ?  $C_{gs}/g_m$ , right? So, there will be, you should expect, if you do go and do the full blown math, you should expect to see a pole at  $C_{gs}/g_m$ , right. And you should also expect to see another pole at, corresponding to  $C_L$  and what will that time constant be? What is the output resistance looking here?

So, basically, if you yank this node up by delta, the same voltage appears here, because no current flows through the R, what is the current that will flow here?

Student:  $g_m V_{test}$ .

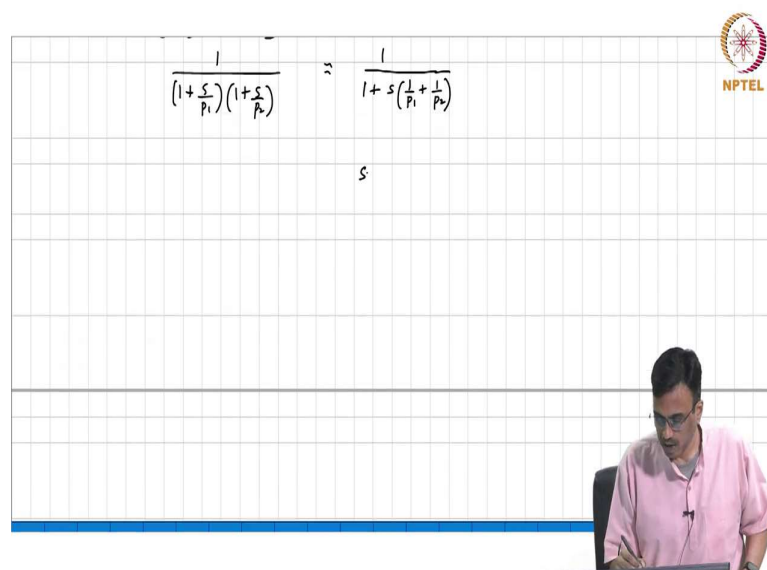
This output resistance is  $1/g_m$ . So, what comment can you make about the time constant associated with  $C_L/g_m$ .

(Refer Slide Time: 13:02)

So, you basically get a pole at  $g_m/C_{gs}$  another pole at  $g_m/C_L$ , ok. To summarize, therefore, the every gain stage basically is associated with at least one pole, right. So, for example, if you cascade a common source amplifier with a common drain amplifier, what comment can you make about the bandwidth? Which of these stages will limit the bandwidth of the common source amplifier, right. And, so, as a, you know, as a consequence, therefore, you should

expect to see that, you know, if you, when you try to cascade, you know, multiple amplifiers, each stage that gives you gain, right, voltage gain, I mean, why are you why are we cascading stages in the first place to get high gain, alright. And, you know, why are we getting, and when we have a high gain stage, each high gain stage has at least one pole, right. If you, I mean, you know, we saw that in reality, if you go and do the math for the common source amplifier, we see that we have two poles, right. And, but then, you know, if you try to have a first approximation, you can simply add the two poles.

(Refer Slide Time: 14:36)



$$\frac{1}{(1 + \frac{s}{P_1})(1 + \frac{s}{P_2})} \approx \frac{1}{1 + s(\frac{1}{P_1} + \frac{1}{P_2})}$$

$s$

Basically, simply because if you have, the intuition behind that is that basically if you have a system which is  $1/((1 + S/P_1)(1 + S/P_2))$ , right. At low frequencies, this is approximately equal to  $1/S (1/P_1 + 1/P_2)$ , ok. I mean, this is simply saying that if you have, I mean, you know, if you have two nodes and each node is associated with the time constant, right, then roughly the time constant of the entire system is some of the time constants of the individual nodes, ok.

So, this is basically. So, to first order, basically you can think of every high gain stage as having at least one pole, right. So, now, if you cascade, I do not know. I mean, if you say, well, it is so easy to get high gain, I can just go on cascading common source amplifiers, right? So, what comment can we make about the gain of a cascade? The gain of cascade of course the DC gain keeps increasing but each additional common source stage introduces a new pole and, you know, all these poles are roughly at the same, have the same order of

magnitude, right, ok. I mean, if you take two identical common source amplifiers and cascade them. If you make sure that the loading of the second one is the same as the first, then you will find that both of them have the same pole, alright. So, if you cascade the multiple stages, you will have multiple poles. So, now, the question is, and of course, you know that an op-amp, you know, is never intended to be operated without feedback, it has never been intended to operate in an open loop. So, when you take a high gain amplifier and you close the loop, we have to make sure that this system is actually stable, right, and that is what we are going to see.