**Analog Electronic Circuits**
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**Lecture - 61**
**Memory Effects in MOS Transistors**

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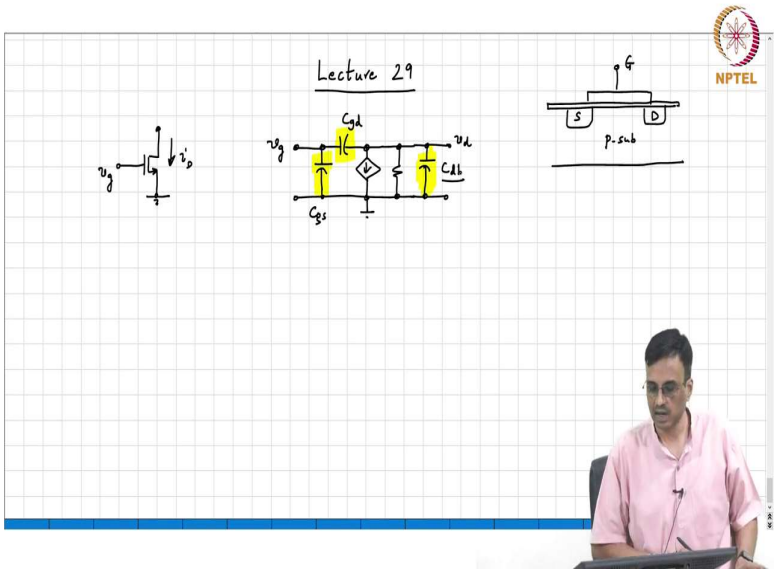


So, far in this course we have assumed that the MOS transistor works instantaneously. In other words you apply gate source voltage and immediately a drain source current incremental of course, develops. But it turns out that in reality and that is not quite correct as one might expect right, nothing in the world is instantaneous. The only thing that you can do as the technology progresses is that the device becomes faster and faster.

So, just like how you know we derive the low frequency small signal model, what did we say? Well, we write the non-linear I-V relationship between the drain current and the drain source voltage as well as the gate source voltage and likewise for the gate current we said the gate current was 0. So, there was really nothing to worry about and the drain current was some complicated nonlinear equation depending on $V_{GS}$ and $V_{DS}$ depending on the quiescent operating point.

And what we would do is basically increase the port voltages by small amounts and see what the changes in the port currents would be, alright. And consequently this is simply valid only

at very low frequencies. It turns out that the MOSFET is actually a much more complicated device and there is a lot of time varying. I mean if the voltages at the terminal change very suddenly then you have to actually solve the physics of the device and solve for the current in the transistor.

So, you will know if you account for memory effects the drain current is not merely governed by some non-linear equation of the gates the $V_{GS}$ and the $V_{DS}$. It now becomes a nonlinear differential equation, which governs $V_{DS}$, $i_D$ I mean $V_{DS}$ and $V_{GS}$ and $i_D$ and $i_G$ also. So, fortunately, however, even if you have a nonlinear differential equation right, if you only look for changes or the ratio I mean if you change the $V_{GS}$ by a small amount and $V_{DS}$ by a small amount. The change in the $V_{DS}$ and the change in the $V_{GS}$. In other words the incremental $V_{DS}$ and the incremental $V_{GS}$ can be related to the incremental drain current and the incremental gate current still by you know linear network it just so, happens as you might expect that now because the transistor is not instantaneous the linear the incremental linear network must consist of elements with memory.

And just like how the details of the small signal model for the low frequency case was derived by differentiating those equations you know which are based which are derived based on the physics of the device. Likewise we have to do that for the MOSFET, right. And that will take us into the realm of device physics which we are not interested in getting it to, right. So, all that we are interested in therefore, is basically you know go to the device folks and say I mean you know all the physics of the device, please go and calculate these extra elements for us right, which are basically these elements with memory which are the which are capacitors and potentially could be inductors also.

But it so turns out that for over large regions of operation the model for the MOSFET which includes the which models the memory of the transistor is basically this one, right. And so, this is so, if the source is grounded then grounded. So, this is basically the model for the MOS transistor when one of its when the source terminal is incrementally grounded. So, this is $v_g$ this is $v_d$ right, and this is all these elements are all the memory elements, right.

And so this is $C_{gs}$ this is $C_{gd}$ as $C_d$, I am going to call it $C_{db}$. It turns out as you all know that how the MOSFET is made is that N-MOSFET is made for instance, that you have some oxide and that is the source, that is the drain and that is the gate, right. And this drain for N-MOSFET what kind of subset substrate do we use?

P substrate. So, the drain and n are made with n plus. So, basically you can see that between the drain and the substrate there is going to be a reverse bias diode. So, this is basically that $C_{db}$ stands for C drain to bulk ok, if the source is grounded then the bulk and the resource are shorted, right. And therefore you basically have it go from drain to source. But strictly speaking I mean the parasitic capacitance is between the drain and if the source is floating I mean is independently controlled.

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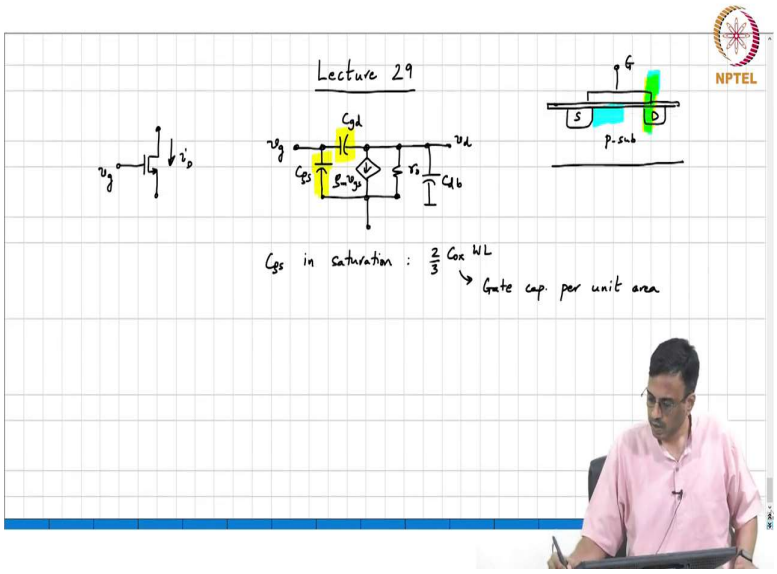


Then this is source, this is the usual $r_o$ and this $i_s$ $g_m$ $v_{gs}$ and there is a capacitance from drain to bulk, ok, alright. The $C_{gd}$ physically is coming because of the or the overlap between the source and the drain, I do not know if you are able to see this in that is the overlap between the gate and the drain, right. The $C_{gs}$ basically are a lot more complicated. It is coming not merely because of the overlap between the gate and the source, but also because there is a channel here, right.

And the channel basically there is the channel is connected to the source and therefore, it seems reasonable that there is some capacitance between the gate and the there is obviously, there is parallel plate capacitance between the gate and the channel right, but the channel is connected to the source electrically.

So, therefore, it seems reasonable that there is some capacitance between the gate and the source. What that capacitance is again you know I remember that this channel is actually

pinched off at one end. So, clearly you know all the field lines from the gate are not you know basically it is not a uniform channel.

And therefore, it is kind of wrong to expect that the gate source capacitance will be simply the parallel plate capacitance between the gate and the channel to actually get a to do this properly you actually have to get into the device physics. And it just so turns out that after all that the $C_{gs}$ in saturation, I mean clearly these are incremental parameters.

So, what comment can you make like all incremental parameters? They must all incremental parameters depend on what? Depend on the operating point, right. And so, all these capacitances also in principle must depend on the operating point. It so, turns out that in saturation $C_{gs}$ happens to be two thirds C ox times W times L, right. C ox is the gate capacitance per unit area and W and L are of course, the width and the length of the, alright. Similarly, $C_{db}$ right, is simply the reverse bias capacitance between the drain and the bulk, right.

And clearly if you have done a basic device physics class you know that a reverse bias junction has a capacitance which changes with the voltage, but for all practical purposes you basically assume that it is constant, right? And $C_{gd}$ again in saturation is basically due to the overlap between the gate and the drain terminal and is expected to be somewhat smaller than $C_{gs}$.

So, ah, but to get exact values of this basically you have to know the device geometry carefully and then do the device physics properly. So, fortunately as a circuit designer you know all these things are modelled. So, when you run a computer simulation you know these things are properly accounted for if the modelling is done, right.

So, again as usual we use this as a black box and then and then move on correct, alright. So, with this background now we need to go back to all the circuits that we have done, right. And see the effect of these parasitic capacitance on the performance.